Carrier Board Design Guide

for COM Express Modules (COM.0 R2.0)

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Revision History

Revision	Date	Description
0.10	8/11/2011	Initial internal draft release.
0.20	10/27/2011	Added note on section 4.3. Updated figure 17 and figure 18 captions.
0.21	2/8/2012	Updated legal page: Copyright year. Added HDMI registered trademark.
0.30	8/2/2013	Removed VCP interface section. Updated pinlists table of Connector C-D. Updated differential trace width, spacing, impedance and accumulated trace length of PCIe in tables 4-4, 4-6, 4-9 and 4-11. Changed PCIe rev. 1.0 and rev. 2.0 to PCIe Gen1 and Gen2 in table 4-6. Updated differential trace width, spacing, and impedance of SATA in table 4-48. Updated accumulated trace length of USB 2.0 and 3.0 in tables 4-53 and 4-56. Updated differential trace width, spacing, and impedance of USB 3.0 in table 4-57. Updated Note on pages 17, 24, 28, 66 and 73 Added COMe-9X90 information and COMEDB4 schematics. Updated the naming of COME8X80 and COME8X90 to COMe-8X80 and COMe-8X90 respectively. Updated copyright year and disclaimer notice.
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1. Introduction

This document provides layout and routing design guidelines to developers of COM Express carrier boards that support the features of VIA COMe-8X80, COMe-8X90 and COMe-9X90 COM Express modules. This guideline provides all the major underlying interfaces related to COM.0 R2.0. While, there are a total of seven different Type of COM Express defined in the COM.0 R2.0, this document discusses only Type 10, Type 2 and Type 6 implementations

This document is not intended to be a specification. All information in the document is believed to be accurate as of the publication date. However, no guarantees are given regarding the accuracy of this document.

1.1. Document Overview

A brief description of each chapter is given below.

Chapter 1: Introduction

Chapter 1 briefly introduces the structure of the design guide document.

Chapter 2: General carrier board recommendations

General design schemes and recommended layout rules are shown in chapter 2. This chapter contains board descriptions and general layout and routing guidelines for a COM Express Carrier Board. These design recommendations should be used when designing a system.

Chapter 3: COM Express Mechanical Specification

Detailed information about the COM Express connector placement and dimensions are described in chapter 3.

Chapter 4: Interface layout and routing recommendations

Detailed layout and routing guidelines for each interface are described in chapter 4.

Appendix A: Video combinations and display device support

Appendix A contains the combination of video and display device support using COM.0 R1.0 module.

Appendix B: COMEDB4, COMEDB2 and COMEDB1 reference schematics

Appendix B contains the schematics for the carrier board reference design. These schematics (COMEDB4, COMEDB2 and COMEDB1) can be used as one example on how to design a COM Express carrier board that provides optimal performance when used with VIA COM Express COMe-9X90 module (COM.0 R2.0), COMe-8X90 module (COM.0 R2.0) and COMe-8X80 module (COM.0 R1.0). The reference designs are only for reference and not to be copied.

1.2. Acronyms and Definitions

Term	Description
AC'97	Audio Codec '97
CF card	CompactFlash card
DMA	Direct Memory Access
DAC	Digital Analog Converter
DDC	Display Data Channel
DDI	Digital Display Interface
DVI	Digital Visual Interface
DVP	Digital Video Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
GBE	Gigabit Ethernet
HDA	High Definition Audio
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IDE	Integrated Drive Electronics
IEEE	Institute of Electrical and Electronics Engineers
LAN	Local Area Network
LCD	Liquid Crystal Display
LPC	Low Pin Count
LVDS	Low-Voltage Differential Signaling
NC	No Connection
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PEGx4	PCI Express Graphics x4 Lane
RGB	Red, Green and Blue analog signals
RJ-45	Registered Jack-45
ROM	Read-Only Memory
SATA	Serial Advanced Technology Attachment
SMBus	System Management Bus
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
VGA	Video Graphics Array

Table 1: Acronyms and Definitions

1.3. Illustrations and Schematics

Illustrations and schematics depicted in this document may show the directional flow of signals. Directional flow is indicated by the pointed ends of the polygonal shapes. See Figure 1.

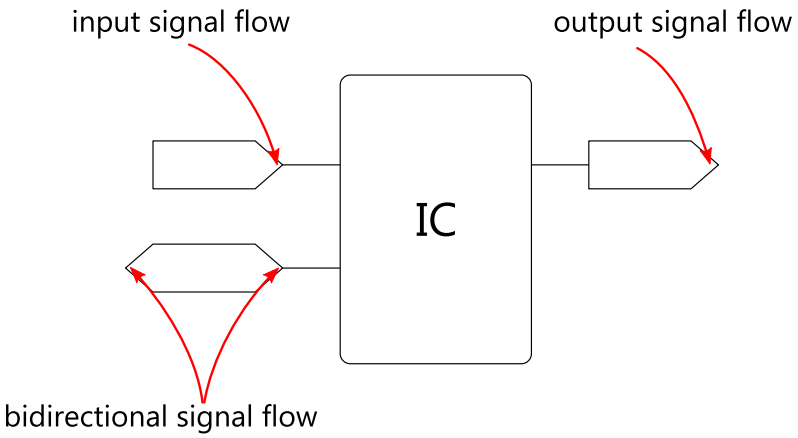


Figure 1: Conventions pertaining to illustration and schematics

2. General Carrier Board Recommendations

This section contains general guidelines for the printed circuit board (PCB) stackup and the layout of traces. General guidelines for routing style, topology, and trace attribute recommendations are also discussed.

2.1. PCB Stackup example

Figure 2 illustrates an example of a PCB with a six-layer stackup. The stackup consists of three signal layers and three reference (power and ground) layers. The three signal layers are referred to as the component layer, inner layer and solder layer. The example below also shows the PCB stackup in a microstrip design.

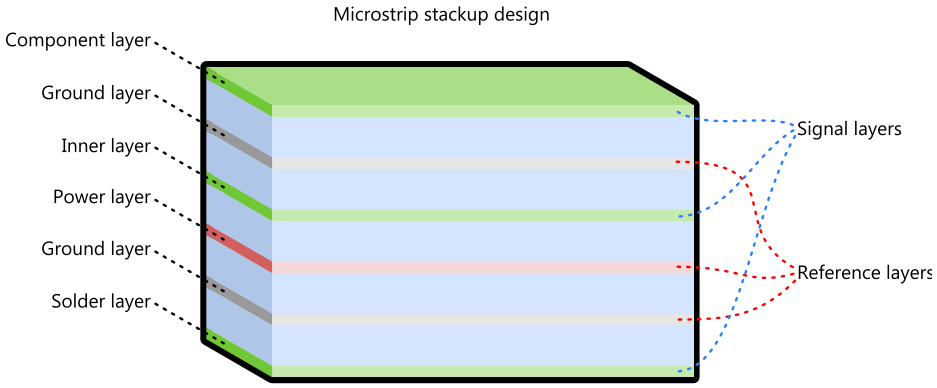


Figure 2: Six-layer microstrip PCB stackup example

2.1.1. Microstrip versus Stripline designs

Carrier board designers can choose between two basic categories of PCB design: microstrip and stripline. Microstrip designs have the outer signal layers exposed. Stripline designs have the outermost signal layers shielded by reference layers.

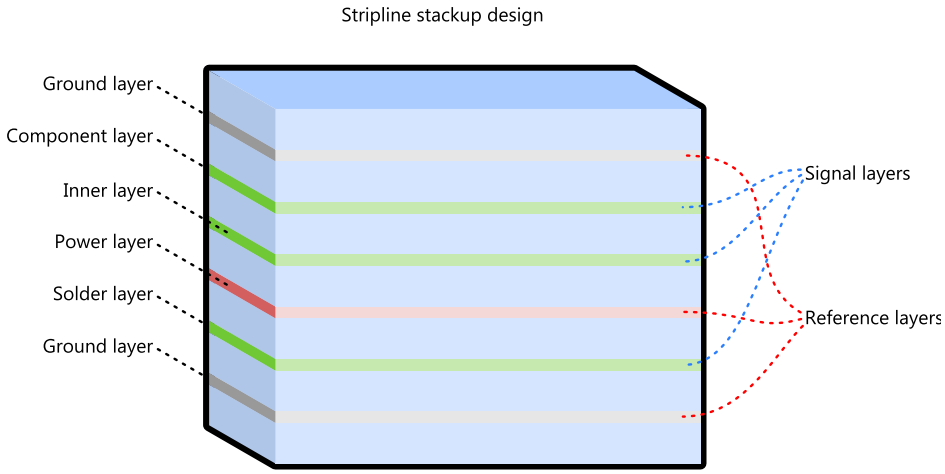


Figure 3: Six-layer stripline PCB stackup example

The choice of microstrip or stripline design depends on the application for which the carrier board is being designed. If the carrier board is being designed for locations where sensitivity to electromagnetic interference (EMI) is an issue, a stripline design is recommended for reducing EMI and noise coupling. For applications where the tolerance for EMI levels is greater, a microstrip design is recommended to reduce costs. Due to the inherent nature of stripline PCB stacks, broad-side coupling is possible.

Layer Description	Thickness Value	Spacing (mil)
Component Layer	0.5 oz. Copper + Planting	
Prepeg	2.4 ~3.5 mil thickness	
Ground Layer	1.0 oz. Copper	
Prepeg	2.4 ~3.5 mil thickness	
Inner Layer	~52.3 mil thickness	
Prepeg	2.4 ~3.5 mil thickness	~62 mil
Power Layer	1.0 oz. Copper	
Prepeg	2.4 ~3.5 mil thickness	
Ground Layer	1.0 oz. Copper	
Prepeg	2.4 ~ 3.5 mil thickness	
Solder Layer	0.5 oz. Copper + Planting	

Table 2: General Six layer microstrip PCB stackup

Description	Value	Notes
Dielectric constant (Er) of Prepeg	3.6 ~ 4.2	@ 1 GHz
Board Impedance	55Ω ± 10%	For all signal layers

Table 3: PCB Stack-Up Detail

Notes:

1. It is not recommended to have any signal routings on either power layer or the ground layer. If a signal must be routed on the power layer, then it should be routed as short as possible.
2. Signal routing on the ground layer is not allowed.
3. Lower trace impedance providing better signal quality is preferred over higher trace impedance for clock signals.

2.2. General Layout and Routing Rules

This section provides general layout rules and routing guidelines for designing COM Express Carrier Boards.

2.2.1. Routing Styles and Topology

Topology is the physical connectivity of a net or a group of nets. There are two types of topologies for a motherboard layout: point-to-point and multi-drop. An example of these topologies is shown in Figure 4.

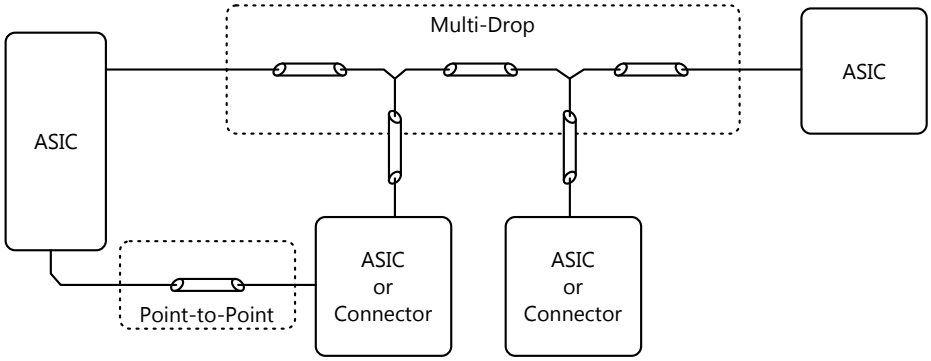


Figure 4: Point-to-point and multi-drop examples

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept as short as possible (less than 1.5"). Therefore, daisy chain style routing is strongly recommended for these signals. Figure 5 below shows an example of daisy chain routing.

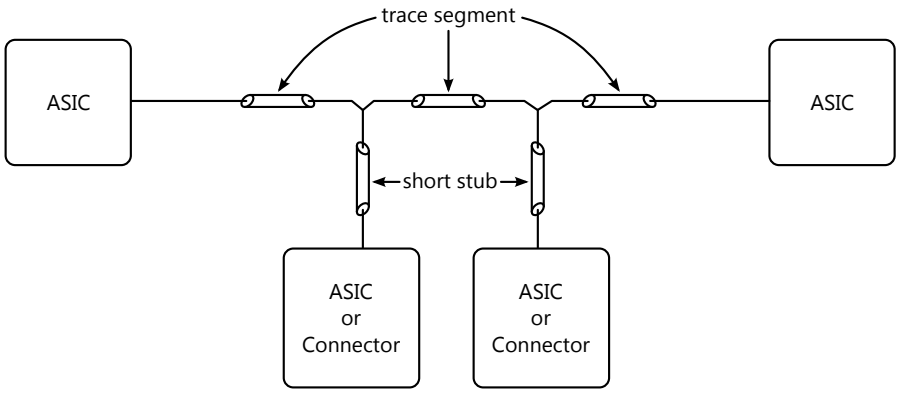


Figure 5: Daisy-chain example

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 6. In this case, the branch point is somewhere between both ends. It may be near the source or near the loads. Being close to the load side is best. The separated traces should be equal in length.

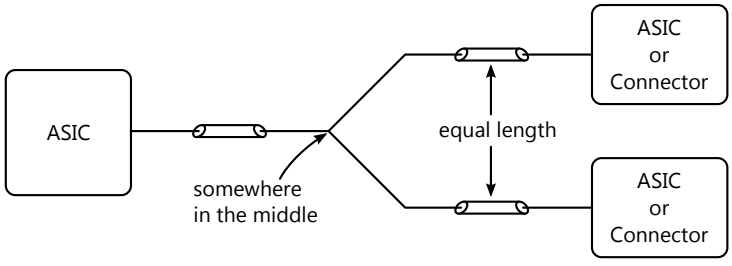


Figure 6: Alternate multi-drop example

2.2.2. General Trace Attribute Recommendations

A 5 mil trace width and 10 mil spacing are generally advised for most signal traces on a COM Express carrier board layout. To reduce trace inductance the minimum power trace width is recommended to be 30 mil.

As a quick reference, the overall recommended trace width and spacing for different trace types are listed in Table 4, and the recommended trace width and spacing for each signal group is shown in Chapter 4.

Trace Type	Trace Width (mil)	Spacing (mil)
Regular Signal	5 or wider	10 or wider
Interface or Bus Reference Voltage Signal	20 or wider	20 or wider
Power	30 or wider	20 or wider

Table 4: Recommended Trace Width and Spacing

General rules for minimizing crosstalk in high-speed bus designs are listed below:

- Maximize the distance between traces. Maintain 10 mil minimum spaces between traces wherever possible.
- Maximize the distance (30 mil minimum) between two adjacent routing areas of different signal groups wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Select a board stack-up that minimizes coupling between adjacent traces.

2.2.3. General Clock Routing Considerations

Clock routing guidelines are listed below:

- The recommended clock trace width is 5 mil.
- The minimum space between one clock trace and adjacent clock traces is 20 mil. The minimum space from one segment of a clock trace to other segments of the same clock trace is at least two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 7).
- Clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 8).
- Series terminations (damping resistors) are needed for all clock signals (typically 0 Ω to 47 Ω). When two loads are driven by one clock signal, the series termination layout is shown in Figure 9. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20 mil to 50 mil wide) is preferred.
- No clock traces on the internal layer if a six-layer board is used.

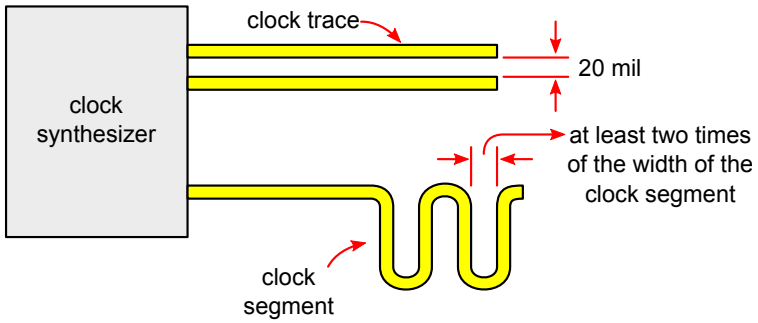


Figure 7: Suggested clock trace spacing

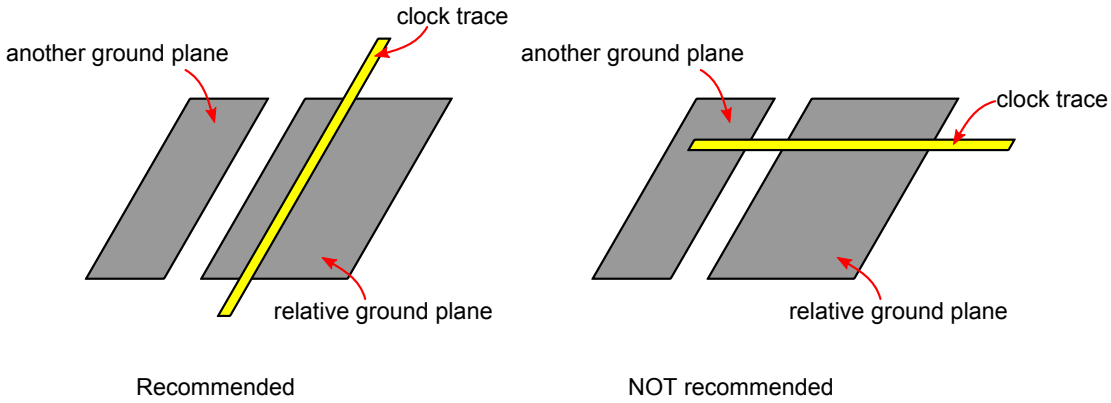


Figure 8: Clock trace layout in relation to the ground plane

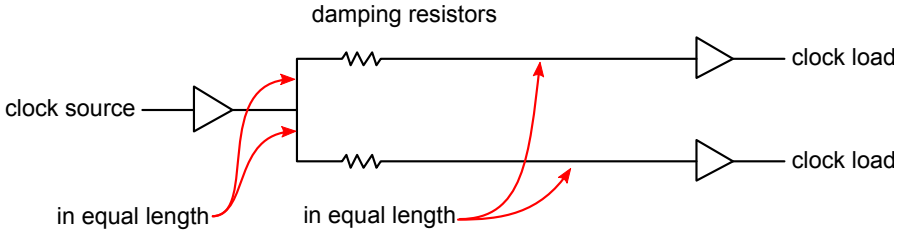


Figure 9: Series termination for multiple clock loads

3. COM Express Mechanical Specification

Carrier boards for VIA COM Express modules must follow the placement defined in the COM Express specification. Figure 10 is a depiction of the top view of a carrier board PCB with an appropriate amount of space reserved for the COM Express module. The placement of the COM Express connectors must be exact to ensure that COM Express modules can be properly fitted.

To increase the thermal performance, a buffer of 5 mm around the perimeter of the area designated for the COM Express module is recommended as a keepout zone.

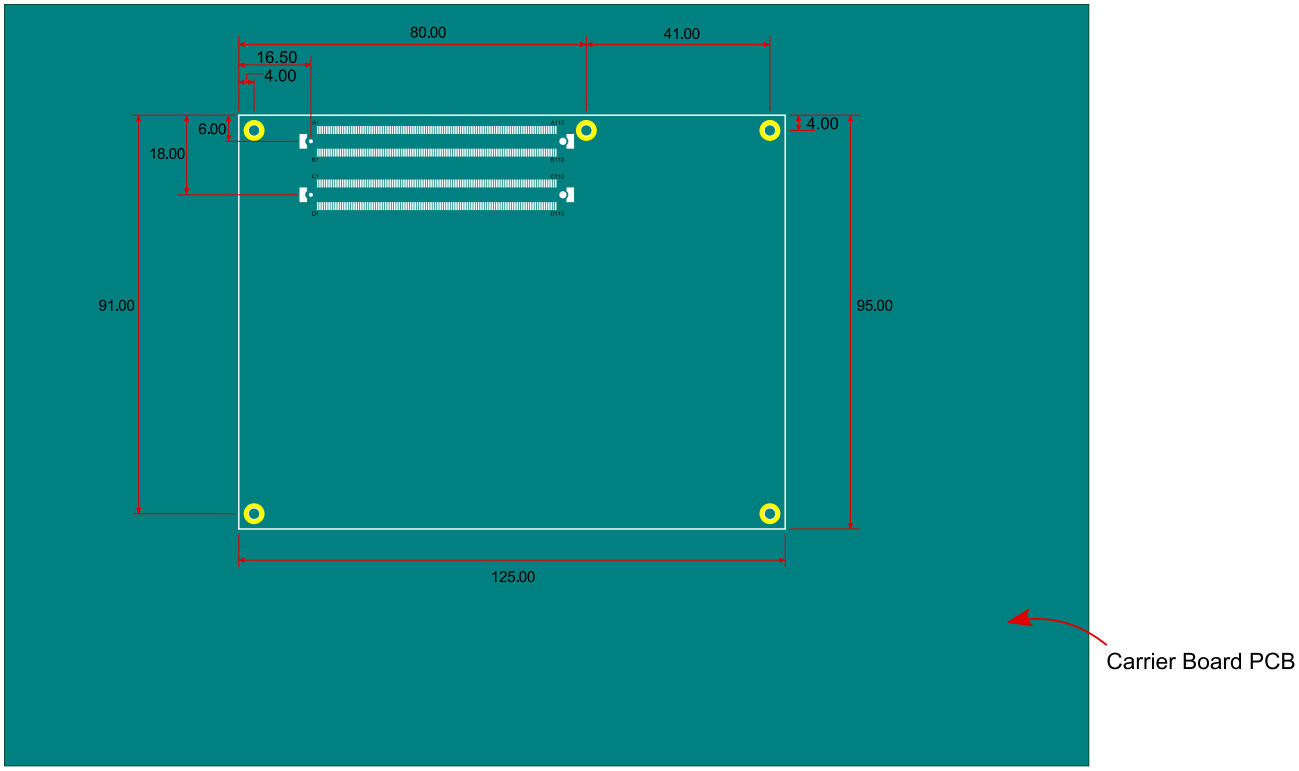


Figure 10: COM Express connector placement on Carrier Board PCB

3.1. COM Express Module Form Factors

The VIA COM Express Module specifies three different types of form factors are shown below.

- **Compact module:** 95 mm x 95 mm
- **Basic module:** 95 mm x 125 mm
- **Extended module:** 110 mm x 155 mm

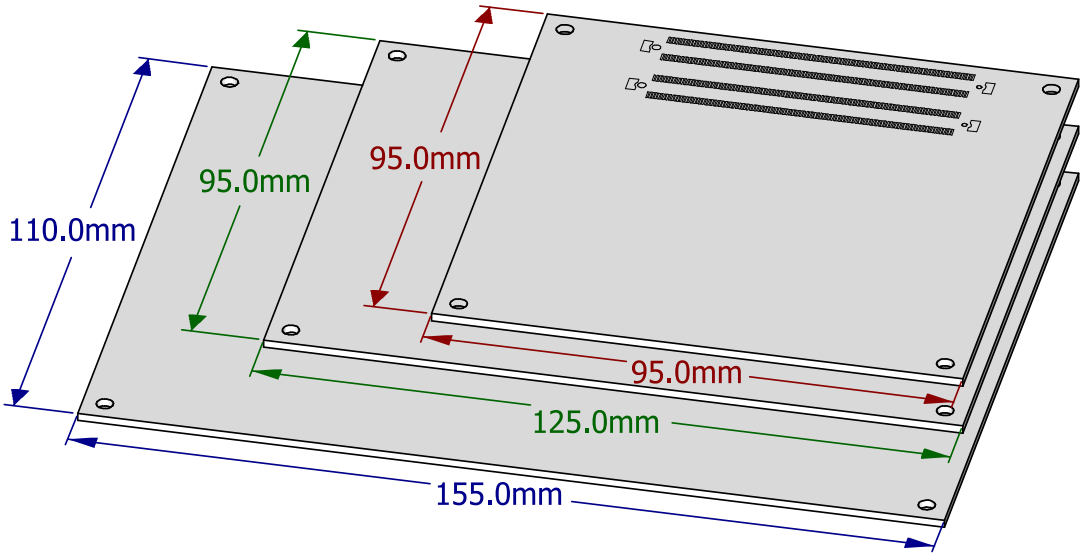


Figure 11: COM Express Form Factors comparisons

3.2. Dimensions of the COM Express Connectors

The COM Express connectors comprises of up to two 220-pin connectors. Each connector is said to have two rows.

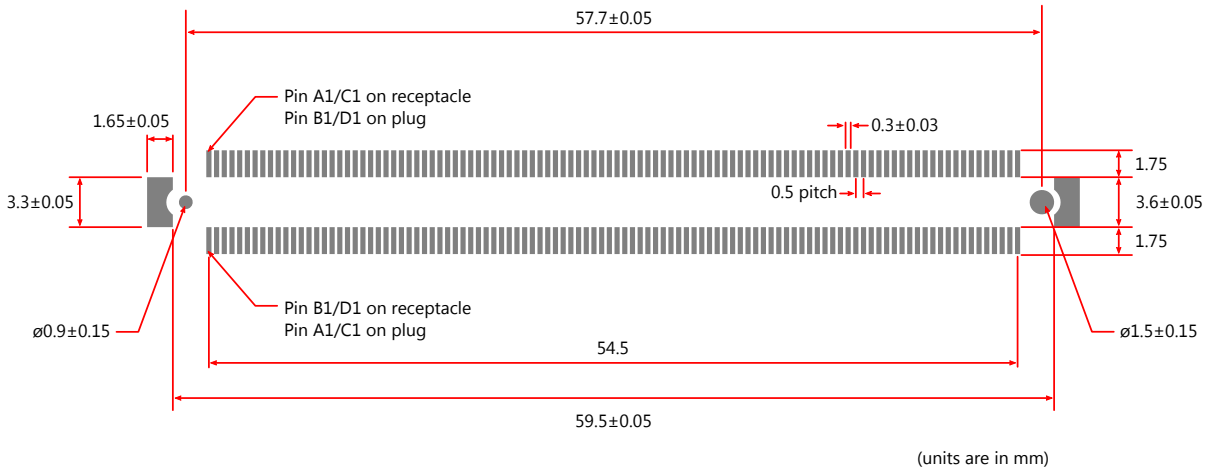


Figure 12: COM Express connector dimensions

The connectors on the bottom of the COM Express module should have the rows in the reverse order of the rows on the carrier board. Figure 13 shows an example of how the rows should be oriented on the COM Express module.

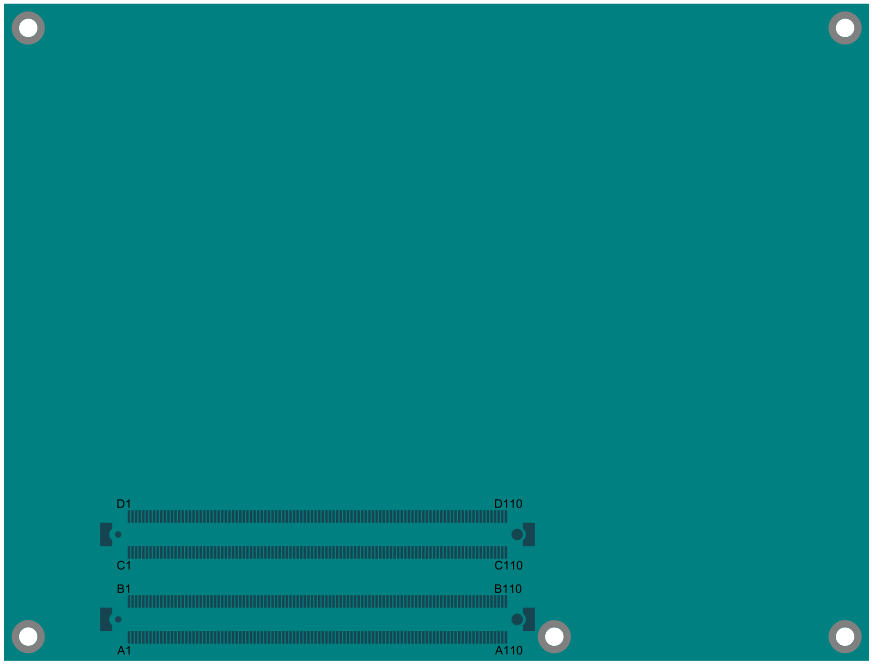


Figure 13: Orientation of COM Express connectors on a COM Express module

3.3. Pinout of COM Express Interface

The pinout tables show the pinout of the COM Express interface as implemented in VIA COM Express modules. The pinout table in section 3.3.1.1 is intended for Type 10 only while the pinout table in section 3.3.2.1 is meant for Type 6 and Type 2.

3.3.1. Type 10 Pinout Connector

3.3.1.1. Connector A-B

Pin	Pinout Name (Row A)	Pin	Pinout Name (Row B)
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	NC	B8	LPC_DRQ0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	NC
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	RSVD	B22	RSVD
A23	RSVD	B23	RSVD
A24	SUS_S5#	B24	PWR_OK
A25	RSVD	B25	RSVD
A26	RSVD	B26	RSVD
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	AC/HAD_SDIN2
A29	AC/HDA_SYNC	B29	AC/HAD_SDIN1
A30	AC/HDA_RST#	B30	AC/HAD_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC/HDA_BITCLK	B32	SPKR
A33	AC/HDA_SDOUT	B33	I2C_CK
A34	-BIOS_DIS0	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#

A48	EXCD0_PERST#	B48	NC
A49	NC	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	RSVD	B52	RSVD
A53	RSVD	B53	RSVD
A54	GPI0	B54	GPO1
A55	RSVD	B55	RSVD
A56	RSVD	B56	RSVD
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	DDI0_PAIR0+
A72	LVDS_A0-	B72	DDI0_PAIR0-
A73	LVDS_A1+	B73	DDI0_PAIR1+
A74	LVDS_A1-	B74	DDI0_PAIR1-
A75	LVDS_A2+	B75	DDI0_PAIR2+
A76	LVDS_A2-	B76	DDI0_PAIR2-
A77	LVDS_VDD_EN	B77	DDI0_PAIR4+
A78	LVDS_A3+	B78	DDI0_PAIR4-
A79	LVDS_A3-	B79	LVDS_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	DDI0_PAIR3+
A82	LVDS_A_CK-	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	RSVD	B87	VCC_5V_SBY
A88	PCIE_CK_REF+	B88	BIOS_DIS1#
A89	PCIE_CK_REF-	B89	DDI0_HPD
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	DDI0_PAIR5+
A92	SPI_MISO	B92	DDI0_PAIR5-
A93	GPO0	B93	DDI0_PAIR6+
A94	SPI_CLK	B94	DDI0_PAIR6-
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	NC	B96	RSVD
A97	NC	B97	SPI_CS#
A98	SER0_TX	B98	DDI0_CTRLCLK_AUX+
A99	SER0_RX	B99	DDI0_CTRLCLK_AUX+
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWNOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	NC	B103	NC
A104	VCC_12V	B104	VCC_12V

A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

3.3.2. Type 6 Pinout Connector

The signal names in gray indicate signals that are relevant to Type 2.

3.3.2.1. Connector A-B

Pin	Pinout Name (Row A)	Pin	Pinout Name (Row B)
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	NC	B8	LPC_DRQ0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4# / NC	B18	NC
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	NC / SATA2_TX+	B22	NC / SATA3_TX+
A23	NC / SATA2_TX-	B23	NC / SATA3_TX-
A24	SUS_S5#	B24	PWR_OK
A25	NC / SATA2_RX+	B25	NC / SATA3_RX+
A26	NC / SATA2_RX-	B26	NC / SATA3_RX-
A27	BATLOW# / NC	B27	WDT
A28	(S)ATA_ACT# / ATA_ACT#	B28	AC/HAD_SDIN2 / NC
A29	AC/HDA_SYNC / AC_SYNC	B29	AC/HAD_SDIN1 / NC
A30	AC/HDA_RST# / AC_RST#	B30	AC/HAD_SDIN0 / AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC/HDA_BITCLK / AC_BITCLK	B32	SPKR
A33	AC/HDA_SDOUT / AC_SDOUT	B33	I2C_CK
A34	-BIOS_DIS0	B34	I2C_DAT
A35	THRMTRIP# / NC	B35	THRM# / NC
A36	USB6- / NC	B36	USB7- / NC
A37	USB6+ / NC	B37	USB7+ / NC
A38	USB_6_7_OC# / NC	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	NC
A49	NC	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#

A51	GND (FIXED)	B51	GND (FIXED)
A52	NC	B52	NC
A53	NC	B53	NC
A54	GPI0	B54	GPO1
A55	NC	B55	NC
A56	NC	B56	NC
A57	GND	B57	GPO2
A58	NC	B58	NC
A59	NC	B59	NC
A60	GND (FIXED)	B60	GND (FIXED)
A61	NC	B61	NC
A62	NC	B62	NC
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	NC / LVDS_B0+
A72	LVDS_A0-	B72	NC / LVDS_B0-
A73	LVDS_A1+	B73	NC / LVDS_B1+
A74	LVDS_A1-	B74	NC / LVDS_B1-
A75	LVDS_A2+	B75	NC / LVDS_B2+
A76	LVDS_A2-	B76	NC / LVDS_B2-
A77	LVDS_VDD_EN	B77	NC / LVDS_B3+
A78	LVDS_A3+	B78	NC / LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	NC / LVDS_B_CK+
A82	LVDS_A_CK-	B82	NC / LVDS_B_CK-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD / KBD_RST#	B86	VCC_5V_SBY
A87	RSVD / KBD_A20GATE	B87	VCC_5V_SBY
A88	PCIE_CK_REF+	B88	BIOS_DIS1#
A89	PCIE_CK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER / SPI_VCC	B91	VGA_GRN
A92	SPI_MISO / SPI_DI	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI / SPI_DO	B95	VGA_I2C_CK
A96	NC / GND	B96	VGA_I2C_DAT
A97	NC	B97	SPI_CS# / -SPI_SS0
A98	SER0_TX / RSVD	B98	RSVD
A99	SER0_RX / RSVD	B99	RSVD
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX / RSVD	B101	FAN_PWNOUT / RSVD
A102	SER1_RX / RSVD	B102	FAN_TACHIN / RSVD
A103	NC / RSVD	B103	NC / RSVD
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V

A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

3.3.2.2. Connector C-D

The signal names in red are meant for DVP pins which are defined and proprietary of VIA Technologies.

Pin	Pinout Name (Row C)	Pin	Pinout Name (Row D)
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND / IDE_D7	D2	GND / IDE_D5
C3	USB_SSRX0- / IDE_D6	D3	USB_SSTX0- / IDE_D10
C4	USB_SSRX0+ / IDE_D3	D4	USB_SSTX0+ / IDE_D11
C5	GND / IDE_D15	D5	GND / IDE_D12
C6	USB_SSRX1- / IDE_D8	D6	USB_SSTX1- / IDE_D4
C7	USB_SSRX1+ / IDE_D9	D7	USB_SSTX1+ / IDE_D0
C8	GND / IDE_D2	D8	GND / IDE_REQ
C9	USB_SSRX2- / IDE_D13	D9	USB_SSTX2- / IDE_IOW#
C10	USB_SSRX2+ / IDE_D1	D10	USB_SSTX2+ / IDE_ACK#
C11	GND (FIXED)	D11	GND (FIXED)
C12	USB_SSRX3- / IDE_D14	D12	USB_SSTX3- / IDE_IRQ
C13	USB_SSRX3+ / IDE_IORDY	D13	USB_SSTX3+ / IDE_A0
C14	GND / IDE_IOR#	D14	GND / IDE_A1
C15	NC / PCI_PME#	D15	NC / IDE_A2
C16	NC / PCI_GNT2#	D16	NC / IDE_CS1#
C17	RSVD / PCI_REQ2#	D17	RSVD / IDE_CS3#
C18	RSVD / PCI_GNT1#	D18	RSVD / IDE_RESET#
C19	NC / PCI_REQ1#	D19	NC / PCI_GNT3#
C20	NC / PCI_GNT0#	D20	NC / IDE_REQ3#
C21	GND (FIXED)	D21	GND (FIXED)
C22	NC / PCI_REQ0#	D22	NC / PCI_AD1
C23	NC / PCI RESET#	D23	NC / PCI_AD3
C24	NC / PCI_AD0	D24	RSVD / PCI_AD5
C25	NC / PCI_AD2	D25	RSVD / PCI_AD7
C26	NC / PCI_AD4	D26	NC / PCI_C/BE0#
C27	RSVD / PCI_AD6	D27	NC / PCI_AD9
C28	RSVD / PCI_AD8	D28	RSVD / PCI_AD11
C29	NC / PCI_AD10	D29	NC / PCI_AD13
C30	NC / PCI_AD12	D30	NC / PCI_AD15
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLCLK_AUX+ / PCI_AD14	D32	NC / PCI_PAR
C33	DDI2_CTRLDATA_AUX- / PCI_C/BE1#	D33	NC / PCI_SERR#
C34	DDI2_DDC_AUX_SEL / PCI_PERR#	D34	NC / PCI_STOP#
C35	RSVD / NC	D35	RSVD / PCI_TRDY#
C36	DDI3_CTRLCLK_AUX+ / PCI_DEVSEL#	D36	NC / PCI_FRAME#
C37	DDI3_CTRLDATA_AUX- / PCI_IRDY#	D37	NC / AD16
C38	NC / PCI_C/BE2#	D38	RSVD / PCI_AD18
C39	DDI3_PAIR0+ / PCI_AD17	D39	DDI2_PAIR0+ / PCI_AD20
C40	DDI3_PAIR0- / PCI_AD19	D40	DDI2_PAIR0- / AD22
C41	GND (FIXED)	D41	GND (FIXED)
C42	DDI3_PAIR1+ / PCI_AD21	D42	DDI2_PAIR1+ / PCI_AD24
C43	DDI3_PAIR1- / PCI_AD23	D43	DDI2_PAIR1- / PCI_AD26
C44	DDI3_HPD / PCI_C/BE3#	D44	DDI2_HPD / PCI_AD28
C45	RSVD / PCI_AD25	D45	RSVD / PCI_AD30
C46	DDI3_PAIR2+ / PCI_AD27	D46	DDI2_PAIR2+ / PCI_IRQC#
C47	DDI3_PAIR2- / PCI_AD29	D47	DDI2_PAIR2- / PCI_IRQD#
C48	RSVD / PCI_AD31	D48	RSVD / NC
C49	DDI3_PAIR3+ / PCI_IRQA#	D49	DDI2_PAIR3+ / NC
C50	DDI3_PAIR3- / PCI_IRQB#	D50	DDI2_PAIR3- / PCI_CLK
C51	GND (FIXED)	D51	GND (FIXED)

C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	NC	D54	NC
C55	PEG_RX1+	D55	PEG_TX1+
C56	PEG_RX1-	D56	PEG_TX1-
C57	NC	D57	TYPE2#
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	NC	D65	NC
C66	NC	D66	NC
C67	RSVD	D67	GND
C68	NC	D68	NC
C69	NC	D69	NC
C70	GND (FIXED)	D70	GND (FIXED)
C71	NC	D71	NC
C72	NC	D72	NC
C73	GND / NC	D73	GND / NC
C74	NC	D74	NC
C75	NC	D75	NC
C76	GND	D76	GND
C77	RSVD	D77	IDE_CBLID#
C78	DVP1_D0	D78	DVP1_D1
C79	DVP1_D2	D79	DVP1_D3
C80	GND (FIXED)	D80	GND (FIXED)
C81	DVP1_D4	D81	DVP1_D5
C82	DVP1_D6	D82	DVP1_D7
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	DVP1_D8	D85	DVP1_D9
C86	DVP1_D10	D86	DVP1_D11
C87	GND	D87	GND
C88	DVP1_D12	D88	DVP1_D13
C89	DVP1_D14	D89	DVP1_D15
C90	GND (FIXED)	D90	GND (FIXED)
C91	DVP1_DE	D91	DVP1_TVCLKR
C92	DVP1_VS	D92	NC
C93	GND	D93	GND
C94	DVP1_HS	D94	DVP1_CLK
C95	DVP1_TVFLD	D95	NC
C96	GND	D96	GND
C97	RSVD	D97	RSVD / DVP1_DET
C98	DVP1_SPD	D98	DVP1_VDD_EN
C99	DVP1_SPCLK	D99	DVP1_BKLT_EN
C100	GND (FIXED)	D100	GND (FIXED)
C101	NC	D101	BLT_CK
C102	NC	D102	NC
C103	GND	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V

C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

Notes:

1. The DVP is VIA's defined interface and not specified in the COM Express standard specification.
2. The VIA COMe-9X90 COM Express module does not support DVP interface.

4. Interface Layout and Routing Recommendations

The information presented in this chapter includes the signal descriptions, reference schematic examples, topology examples, and detailed layout and routing guidelines for each bus interface. The information provided is intended for designing COM Express carrier boards that are compliant with VIA COM Express modules.

4.1. PCI Express x1 Interface

VIA COM Express (COM.0 R2.0) modules can support up to four PCI Express lanes. The four lanes can be grouped into four x1 mode configurations. Each of these modes consists of two differential signal pairs: the *receive data pair* and the *transmit data pair*.

This section will help the developer to create a robust PCI Express x1 interface design on the carrier board. However, the carrier board designer should do an appropriate analysis and simulation to verify that the design fulfills PCI Express specification requirements.

4.1.1. PCIe x1 Signal Definition

The general purpose PCI Express interfaces are defined by the PICMG COM Express specification on connector A-B.

Signal Name	Pin #	I/O	Description	Type
PCIE_RX0+	B68	I	Receive input differential pair. Channel 0	10, 6 and 2
PCIE_RX0-	B69			
PCIE_TX0+	A68	O	Transmit output differential pair. Channel 0	
PCIE_TX0-	A69			
PCIE_RX1+	B64	I	Receive input differential pair. Channel 1	10, 6 and 2
PCIE_RX1-	B65			
PCIE_TX1+	A64	O	Transmit output differential pair. Channel 1	
PCIE_TX1-	A65			
PCIE_RX2+	B61	I	Receive input differential pair. Channel 2	10
PCIE_RX2-	B62			
PCIE_TX2+	A61	O	Transmit output differential pair. Channel 2	
PCIE_TX2-	A62			
PCIE_RX3+	B58	I	Receive input differential pair. Channel 3	10
PCIE_RX3-	B59			
PCIE_TX3+	A58	O	Transmit output differential pair. Channel 3	
PCIE_TX3-	A59			
PCIE_CK_REF+	A88	O	PCIe and PEG lanes reference Clock	10, 6 and 2
PCIE_CK_REF-	A89			
EXCD0_PERST#	A48	O	PCIe Card0: Reset, Active Low	10, 6 and 2
EXCD1_PERST#	B47	I	PCIe Card1: Reset, Active Low	10, 6 and 2
CB_RESET#	B50	O	Reset output from Module to Carrier Board	10, 6 and 2
WAKE0#	B66	I	PCIe wake up signal	10, 6 and 2
PCI_RESET#	C23	O	PCI reset output	2

Table 5: Four x1 Lane PCI Express Signal Descriptions

4.1.2. PCIe x1 Reference Schematics

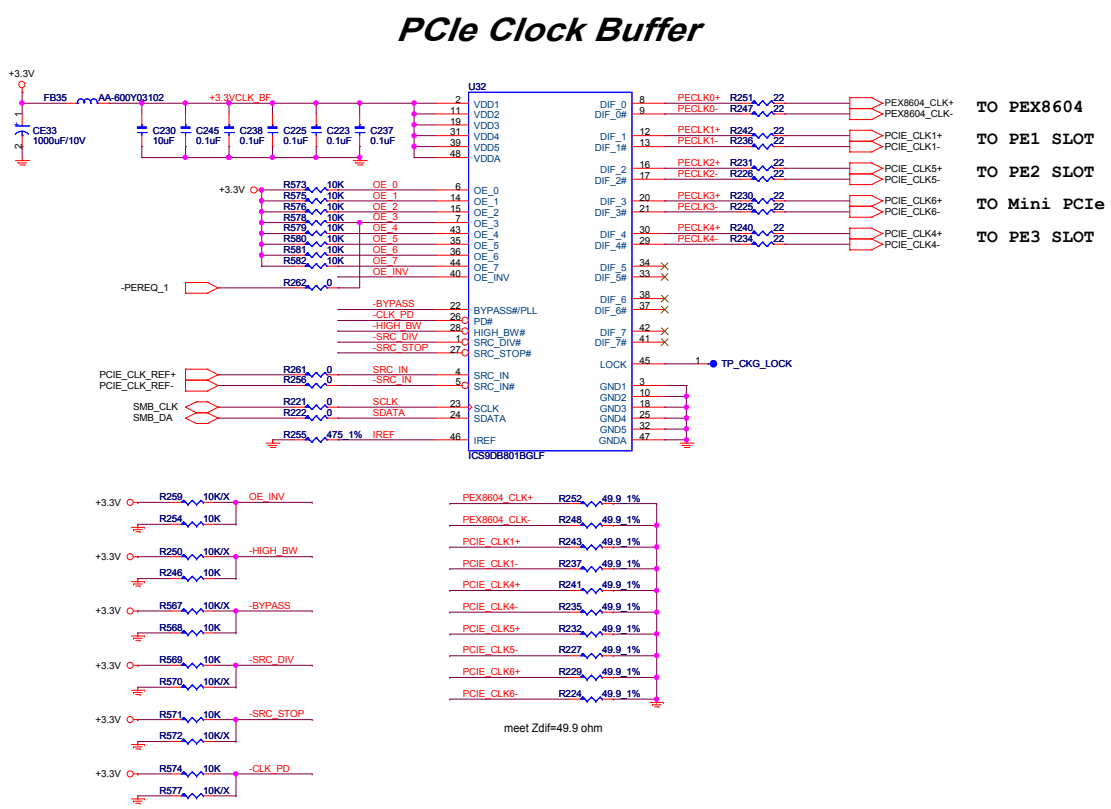


Figure 14: PCI Express Clock Buffer

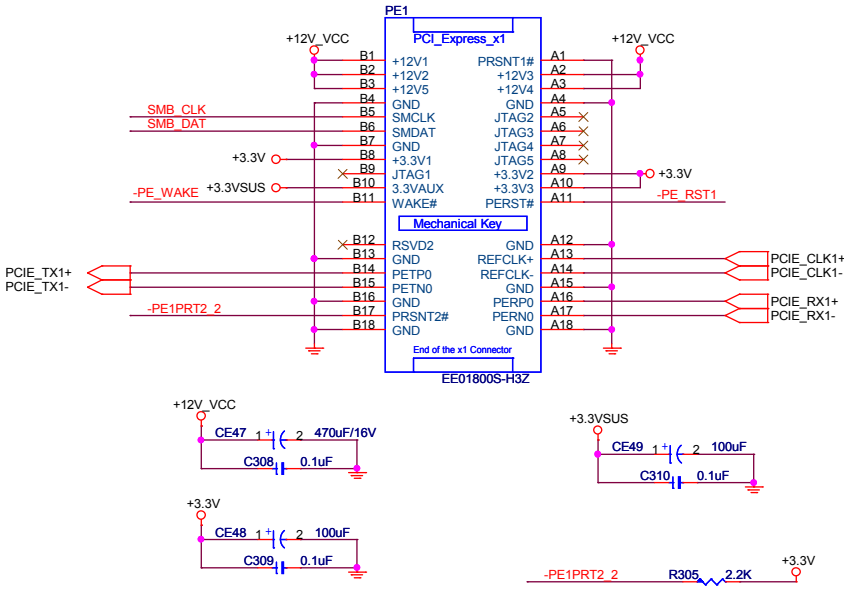


Figure 15: PCI Express x1 Mode Slot

4.1.2.1. PCIe x1 Interface Topology

Each PCI Express slot (PE1 to PE4) contains one signal group that represents the PCI Express x1 mode. These signal groups are listed in Table 6, and grouped in the example below. The PCI Express signal has a point-to-point topology.

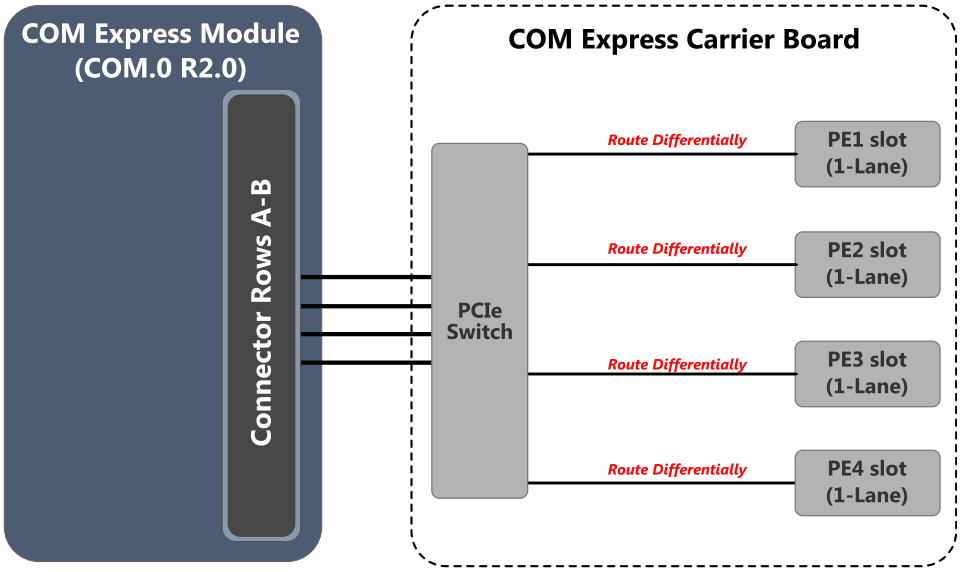


Figure 16: PCI Express x1 Mode Topology Example

Signal Groups	Signal Name	
PE1 slot (1-Lane)	Lane 0	PCIE_RX0+
		PCIE_RX0-
		PCIE_TX0+
		PCIE_TX0-
PE2 slot (1-Lane)	Lane 1	PCIE_RX1+
		PCIE_RX1-
		PCIE_TX1+
		PCIE_TX1-
PE3 slot (1-Lane)	Lane 2	PCIE_RX2+
		PCIE_RX2-
		PCIE_TX2+
		PCIE_TX2-
PE4 slot (1-Lane)	Lane 3	PCIE_RX3+
		PCIE_RX3-
		PCIE_TX3+
		PCIE_TX3-

Table 6: PCI Express Signal Groups PE1 to PE4 slot

4.1.2.2. Mini PCI Express socket

The Mini PCI Express socket is a 52-pin socket that is designed for modular PCI Express Mini Cards. Applying the Mini PCIe socket enables the COM Express carrier board to have a flexible upgrade path. The Mini PCI Express socket consists of a single PCIe x1 lane and single USB 2.0 channel wherein the PCI Express Mini Card host can use either (PCIe x1 or USB 2.0 link) interfaces.

Signal	Pin #	Description	Type
WAKE#	1	Request to return to full operation and respond to PCIe	
+3.3VAUX	2	Primary source voltage, 3.3V	
NC	3	No Connection	
GND	4	Ground	
NC	5	No Connection	
+1.5V	6	Secondary source voltage, 1.5V	
CLKREQ#	7	Clock request signal	
UIM_PWR	8	User Identity Modules power source	
GND	9	Ground	
UIM_DATA	10	Data signal for User Identity Module	
REFCLK-	11	Negative reference clock differential pair	
UIM_CLK	12	Clock signal for User Identity Module	
REFCLK+	13	Positive reference clock differential pair	
UIM_RESET	14	Reset signal for User Identity Module	
GND	15	Ground	
UIM_VPP	16	Variable supply voltage for User Identity Module	
RSVD	17	Reserved	
GND	18	Ground	
RSVD	19	Reserved	
W_DISABLE#	20	Used to disable radio operation on add-in cards	
GND	21	Ground	
PERST#	22	PCI Express reset	
PERn0	23	Receiver differential pair negative signal, Lane 0	
3.3VAUX	24	Auxiliary voltage source, 3.3V	
PERp0	25	Receiver differential pair positive signal, Lane 0	10, 6 and 2
GND	26	Ground	
GND	27	Ground	
+1.5V	28	Secondary source voltage, 1.5V	
GND	29	Ground	
SMB_CLK	30	SMBus clock	
PETn0	31	Transmit differential pair negative signal, Lane 0	
SMB_DATA	32	SMBus data	
PETp0	33	Transmit differential pair positive signal, Lane 0	
GND	34	Ground	
GND	35	Ground	
USB_D-	36	USB data interface differential pair, negative signal	
GND	37	Ground	
USB_D+	38	USB data interface differential pair, positive signal	
+3.3VAUX	39	Primary source voltage, 3.3V	
GND	40	Ground	
+3.3VAUX	41	Primary source voltage, 3.3V	
LED_WWAN#	42	LED status indicator signal	
GND	43	Ground	
LED_WLAN#	44	LED status indicator signal	
RSVD	45	Reserved	
LED_WPAN#	46	LED status indicator signal	
RSVD	47	Reserved	
+1.5V	48	Secondary source voltage, 1.5V	
RSVD	49	Reserved	

GND	50	Ground	10, 6 and 2
RSVD	51	Reserved	
+3.3VAUX	52	Primary source voltage, 3.3V	

Table 7: Mini-PCI Express socket pinout definition

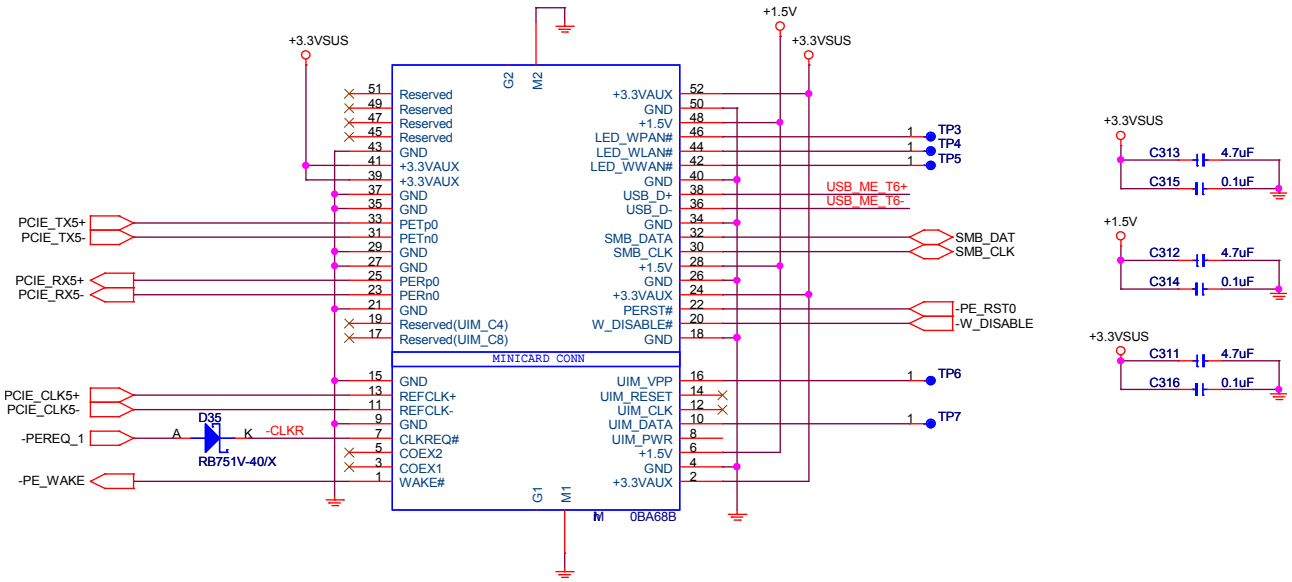


Figure 17: Mini PCI Express Card Socket

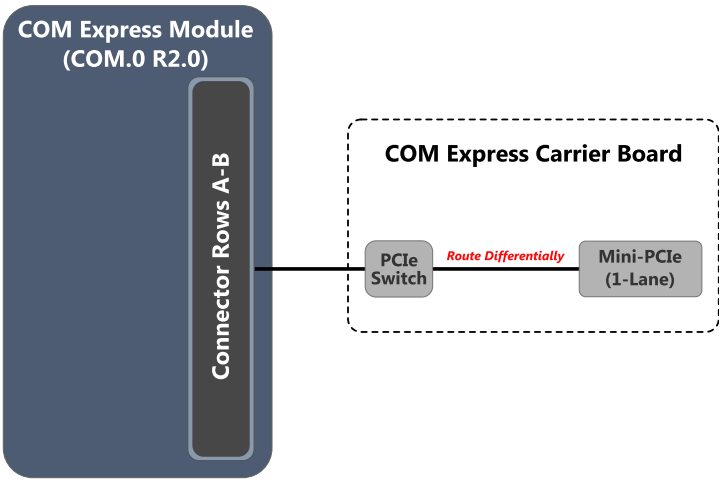


Figure 18: Mini PCI Express x1 Mode Topology Example

4.1.2.3. PCIe x1 Mode Layout and Routing Recommendations

- All the PCI Express signals should be referenced to the ground plane at all times.
- Each trace of differential pairs should route to parallel to each other with the same trace length.
- The spacing between differential pairs must be equal at all times (in parallel), even during trace bending and serpentine topology.
- Differential pairs must be routed on the same layer with maximum of one signal layer change allowed. The differential pairs must always move to the same layer with the same reference plane.
- Transmit differential pairs are recommended to be routed on the top layer and receive differential pairs are recommended to be routed on the bottom layer.
- Do not route PCI Express traces under magnetic devices or IC's, oscillators and clock synthesizers.
- To minimize signal crosstalk, wider spacing is recommended wherever possible between traces.
- It is always best to reduce the line mismatch to add to the timing margin. In other words, a balanced topology can match the trace lengths within the groups to minimize skew.

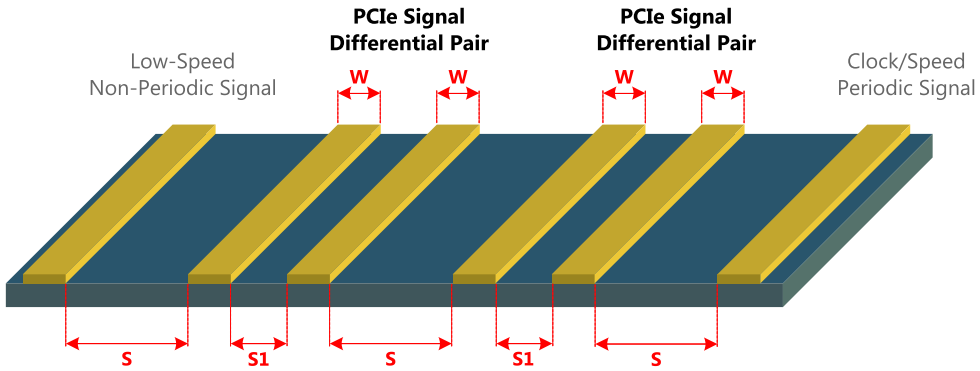


Figure 19: PCI Express (x1 mode) Trace Spacing

Signal Group		Trace & Spacing (S : W : S1 : W : S)	Differential Trace Impedance	Spacing to Other Signals
PE1	Receive	20 : 5 : 5 : 5 : 20 Differential	85Ω ± 10%	20 mil
	Transmit			
PE2	Receive			
	Transmit			
PE3	Receive			
	Transmit			
PE4	Receive			
	Transmit			

Table 8: PCI Express Trace Properties

Signal Group		Routing Topology	Signal Type	Note
PE1	Receive	Point to Point	Source Synchronous I/O Signals	Do not cross power plane division line
	Transmit			
PE2	Receive			
	Transmit			
PE3	Receive			
	Transmit			
PE4	Receive			
	Transmit			

Table 9: PCI Express Interface Routing Topology and Signal Type

Signal Group	Routing Layer	Accumulated Trace Length	Differential Trace Length Mismatch
PE1	Top or Bottom	< 8" (for PCIe Gen1) < 5" (for PCIe Gen2)	< 0.005"
PE2			
PE3			
PE4			

Table 10: PCI Express Interface Layout Guidelines

Note:
The PCIe Gen1 and PCIe Gen2 mode trace length in VIA COM Express module is approximately 3", therefore the PCIe Gen1 and PCIe Gen2 mode trace length in the carrier board should not be longer than 5" and 2" respectively.

4.2. PCI Express Graphics (PEG x4) Interface

This section describes the layout and routing guidelines that ensure a robust PEG x4 interface design. The PCI Express Graphics interface is defined by the PICMG COM Express specification on connector C-D. The VIA COM Express modules (specifically the Type 6 and Type 2) can support one PCI Express Graphics (PEG) x4 lane.

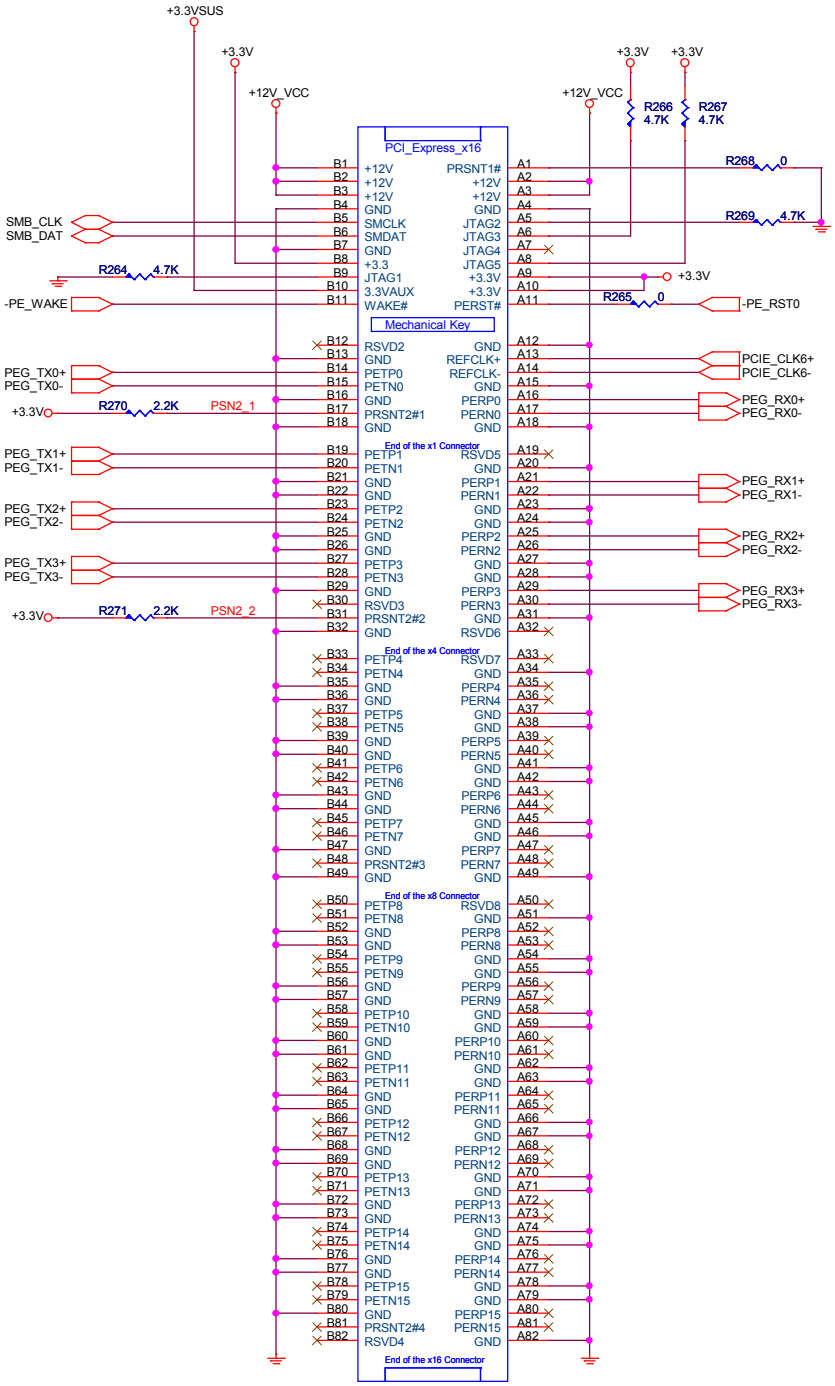
4.2.1. PEG x4 Signal Definition

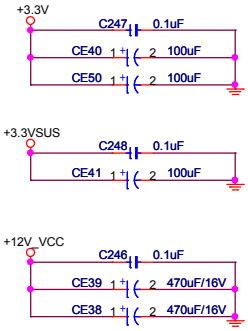
The PEG x4 lane uses differential signaling on each lane (consisting of a receive data and transmit data signal pair) that results in a high-bandwidth interface. The PEG x4 lane signals on VIA COM Express modules (COM.0 R2.0) are intended for handling an external video graphics card. However, if the PEG x4 lane signal is not used for an external video graphics interface, it can be used by other PCI Express devices.

Signal Name	Pin #	I/O	Description	Type
PEG_RX0+	C52	I	Receive input differential pair. Channel 0	6 and 2
PEG_RX0-	C53	I	Receive input differential pair. Channel 0	
PEG_TX0+	D52	O	Transmit input differential pair. Channel 0	
PEG_TX0-	D53	O	Transmit input differential pair. Channel 0	
PEG_RX1+	C55	I	Receive input differential pair. Channel 1	6 and 2
PEG_RX1-	C56	I	Receive input differential pair. Channel 1	
PEG_TX1+	D55	O	Transmit input differential pair. Channel 1	
PEG_TX1-	D56	O	Transmit input differential pair. Channel 1	
PEG_RX2+	C58	I	Receive input differential pair. Channel 2	6 and 2
PEG_RX2-	C59	I	Receive input differential pair. Channel 2	
PEG_TX2+	D58	O	Transmit input differential pair. Channel 2	
PEG_TX2-	D59	O	Transmit input differential pair. Channel 2	
PEG_RX3+	C61	I	Receive input differential pair. Channel 3	6 and 2
PEG_RX3-	C62	I	Receive input differential pair. Channel 3	
PEG_TX3+	D61	O	Transmit input differential pair. Channel 3	
PEG_TX3-	D62	O	Transmit input differential pair. Channel 3	
PCIE_CK_REF+	A88	O	PCI Express reference clock, positive signal	10, 6 and 2
PCIE_CK_REF-	A89	O	PCI Express reference clock, negative signal	

Table 11: PEG x4 Signal Descriptions

4.2.2. PEG x4 Reference Schematics





Close PCI Express x16 Slot

Figure 20: PEG x4 Slot (PE16) Example

4.2.2.1. PEG x4 Interface Topology

The PE16 slot contains signal groups that represent 4-lane PCI Express (PEG x4) interfaces. These signal groups are listed in Table 12.

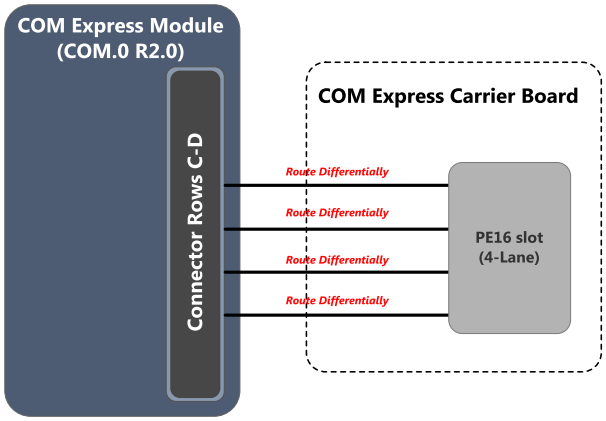


Figure 21: PEG x4 Topology Example

Signal Groups	PEG x4 Signal Name	
PE16 slot (4-Lane)	Lane 0	PEG_RX0+
		PEG_RX0-
		PEG_TX0+
		PEG_TX0-
	Lane 1	PEG_RX1+
		PEG_RX1-
		PEG_TX1+
		PEG_TX1-
	Lane 2	PEG_RX2+
		PEG_RX2-
		PEG_TX2+
		PEG_TX2-
	Lane 3	PEG_RX3+
		PEG_RX3-
		PEG_TX3+
		PEG_TX3-

Table 12: PEG x4 Signal Group

4.2.2.2. PEG x4 Layout and Routing Recommendations

The layout and routing recommendations for the PEG x4 signals in COM Express carrier board are listed below:

- Each trace of differential pairs should route to parallel to each other with the same trace length.
- All the PCI Express signals should be referenced to the ground plane at all times.
- The spacing between differential pairs must be equal at all times (in parallel), even during trace bending and serpentine topology.
- Differential pairs must be routed on the same layer with maximum of one signal layer change allowed. The differential pairs must always move to the same layer with the same reference plane.
- Transmit differential pairs are recommended to be routed on the top layer and receive differential pairs are recommended to be routed on the bottom layer.
- Do not route PCI Express traces under magnetic devices or IC's, oscillators and clock synthesizers.
- To minimize signal crosstalk, wider spacing is recommended wherever possible between traces.
- It is always best to reduce the line mismatch to add to the timing margin. In other words, a balanced topology can match the trace lengths within the groups to minimize skew.

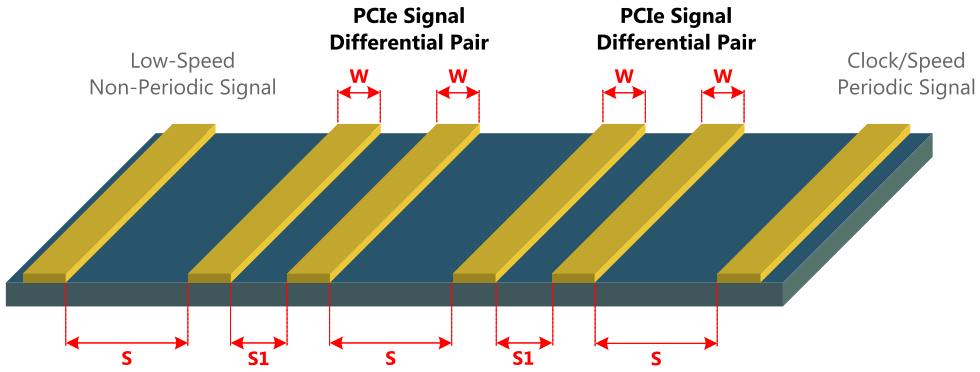


Figure 22: PEG x4 Trace Spacing

Signal Group		Trace & Spacing (S : W : S1 : W : S)	Differential Trace Impedance	Spacing to Other Signal
PE16 (4-Lane)	Transmit Receive	15 : 5 : 5 : 5 : 15 Differential	85Ω ± 10%	20 mil

Table 13: PEG x4 Interface Trace Properties

Signal Group		Routing Topology	Signal Type	Note
PE16 (4-Lane)	Transmit Receive	Point to Point	Source Synchronous I/O Signals	Don't cross power plane division line

Table 14: PEG x4 Interface Routing Topology and Signal Type

Signal Group	Routing Layer	Accumulated Trace Length	Trace Length Mismatch
PE16 (4-Lane)	Top or Bottom	< 5" (for PCIe Gen1) < 2" (for PCIe Gen2)	< 0.005"

Table 15: PEG x4 Interface Layout Guidelines

4.3. Digital Display Interface

The DDI interface is one of the newly added interfaces in COM Express (COM.0 R2.0). The VIA COM Express (COM.0 R2.0 compliant) modules provide Digital Display Interface (DDI) pin-out signals designed for interfacing the HDMI® (High Definition Multimedia Interface) or DisplayPort connection.

The Type 10 module supports one DDI interface for DDI port 1. Its pin-out locations are implemented only on connector row B. Previously on Type 1 modules, the pin-out were used for the LVDS channel B and VGA interfaces. The Type 6 module can support up to two DDI interface for DDI port 2 and DDI port 3 on connector C-D. The carrier board developer can use the DDI port 2 to configure it to either HDMI® or DiplayPort connection. The DDI port 3 is intended only for DisplayPort interface connection. The HDMI® and DisplayPort connectors both use differential signaling, however, the auxiliary channel is required when DDI port 2 is going to be configured as a DisplayPort connection.

4.3.1. Digital Display Interface Signal Definition

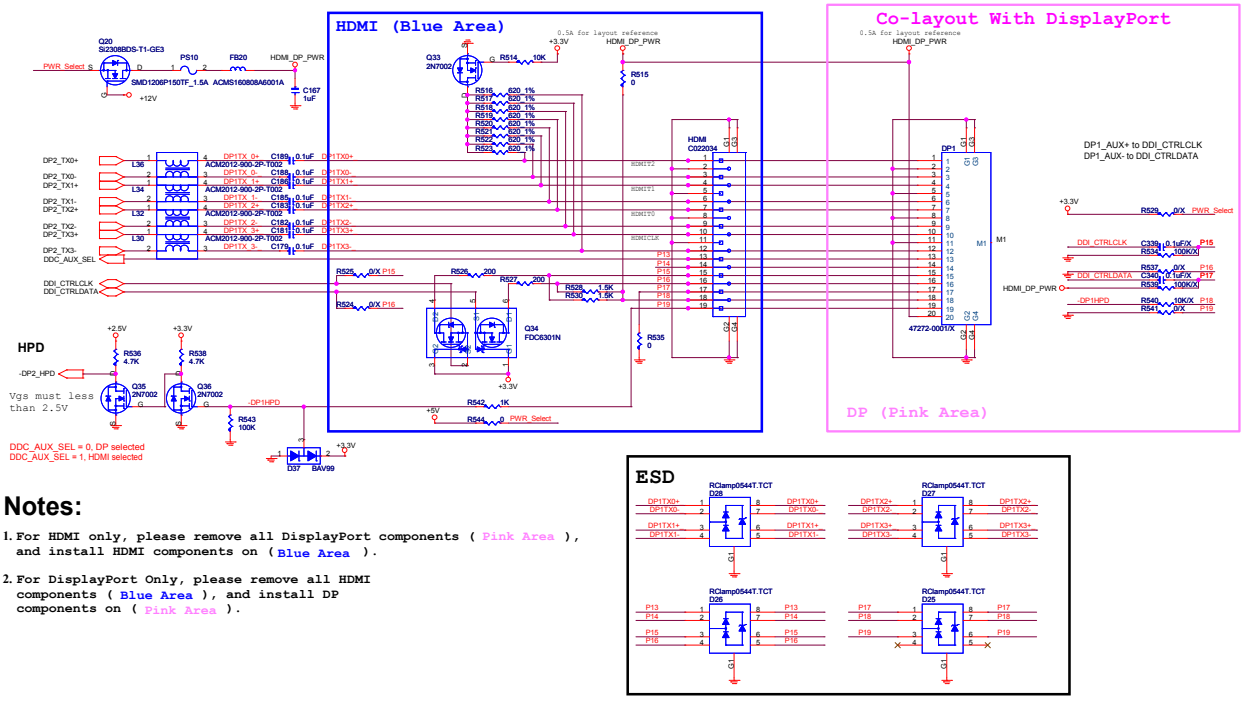
In Type 10 module, the corresponding DDI interfaces (DDI port 1) pin-out signals are defined in connector row B. In Type 6 module, the corresponding DDI interfaces (DDI port 2 and port 3) pin-out signals are defined in connector C-D.

Signal Name	Pin #	I/O	Description	Type
DDI0_PAIR0+	B71	O	Digital Display Interface 0 Pair 0 differential pair	10
DDI0_PAIR0-	B72			
DDI0_PAIR1+	B73	O	Digital Display Interface 0 Pair 1 differential pair	
DDI0_PAIR1-	B74			
DDI0_PAIR2+	B75	O	Digital Display Interface 0 Pair 2 differential pair	
DDI0_PAIR2-	B76			
DDI0_PAIR3+	B81	O	Digital Display Interface 0 Pair 3 differential pair	
DDI0_PAIR3-	B82			
DDI0_PAIR4+	B77	O	Digital Display Interface 0 Pair 4 differential pair	
DDI0_PAIR4-	B78			
DDI0_PAIR5+	B91	O	Digital Display Interface 0 Pair 5 differential pair	
DDI0_PAIR5-	B92			
DDI0_PAIR6+	B93	O	Digital Display Interface 0 Pair 6 differential pair	
DDI0_PAIR6-	B94			
DDI0_HPD	B89	I	Digital Display Interface 0 Hot-Plug Detect	
DDI2_PAIR0+	D39	O	Digital Display Interface 2 Pair 0 differential pair	6
DDI2_PAIR0-	D40			
DDI2_PAIR1+	D42	O	Digital Display Interface 2 Pair 1 differential pair	
DDI2_PAIR1-	D43			
DDI2_PAIR2+	D46	O	Digital Display Interface 2 Pair 2 differential pair	
DDI2_PAIR2-	D47			
DDI2_PAIR3+	D49	O	Digital Display Interface 2 Pair 3 differential pair	
DDI2_PAIR3-	D50			
DDI2_HPD	D44	I	Digital Display Interface 2 Hot-Plug Detect	
DDI2_CTRLCLK_AUX+	C32	IO	DP Aux+ function if DDI[2]_DDC_AUX_SEL is not connected	
			HDMI I²C CTRLCLK if DDI[2]_DDC_AUX_SEL is pulled high	
DDI2_CTRLDATA_AUX-	C33	IO	DP Aux- function if DDI[2]_DDC_AUX_SEL is not connected	
			HDMI I²C CTRLDATA if DDI[2]_DDC_AUX_SEL is pulled high	
DDI2_DDC_AUX_SEL	C34	I	Select the function of DDI[2]_CTRLCLK_AUX+ and DDI[2]_CTRLDATA_AUX-	
DDI3_PAIR0+	C39	O	Digital Display Interface 3 Pair 0 differential pair	
DDI3_PAIR0-	C40			
DDI3_PAIR1+	C42	O	Digital Display Interface 3 Pair 1 differential pair	
DDI3_PAIR1-	C43			

DDI3_PAIR2+	C46	O	Digital Display Interface 3 Pair 2 differential pair	6
DDI3_PAIR2-	C47			
DDI3_PAIR3+	C49	O	Digital Display Interface 3 Pair 3 differential pair	
DDI3_PAIR3-	C50			
DDI3_HPD	C44	I	Digital Display Interface 3 Hot-Plug Detect	
DDI3_CTRLCLK_AUX+	C36	IO	DP Aux+ function if DDI[3]_DDC_AUX_SEL is not connected	
			HDMI I²C CTRLCLK if DDI[3]_DDC_AUX_SEL is pulled high	
DDI3_CTRLDATA_AUX-	C37	IO	DP Aux- function if DDI[3]_DDC_AUX_SEL is not connected	
			HDMI I²C CTRLDATA if DDI[3]_DDC_AUX_SEL is pulled high	

Table 16: Digital Display Interface Signal Descriptions

4.3.2. DDI Reference Schematics



Notes:

1. For HDMI only, please remove all DisplayPort components (Pink Area), and install HDMI components on (Blue Area).
2. For DisplayPort Only, please remove all HDMI components (Blue Area), and install DP components on (Pink Area).

Figure 23: DDI Interface Implementation Example

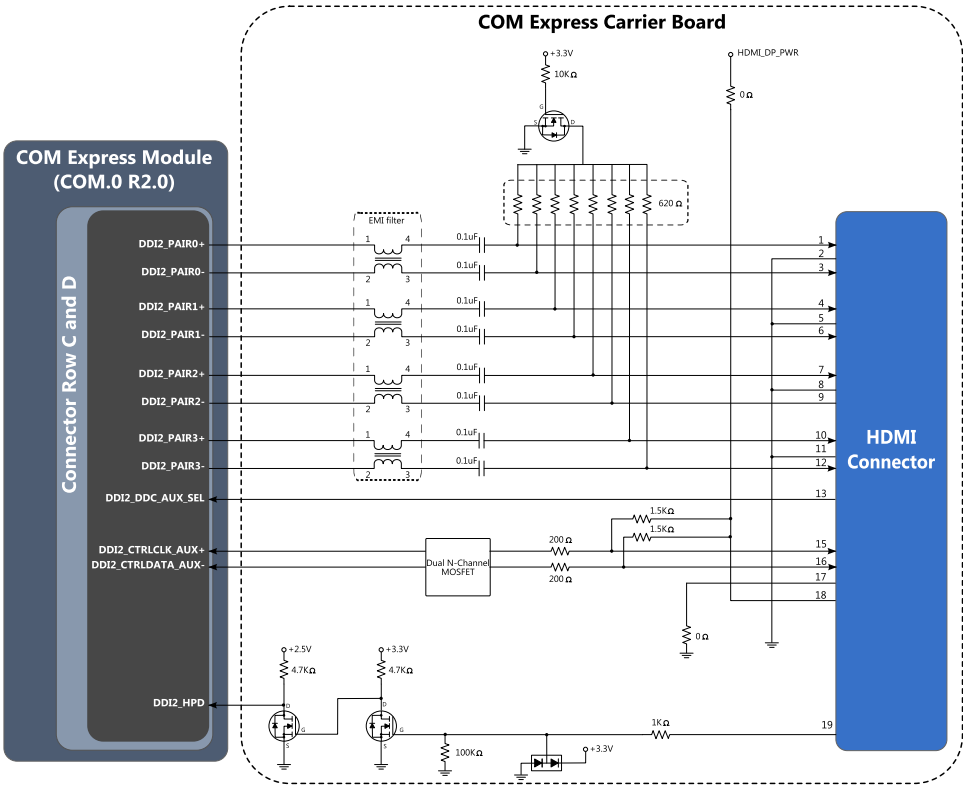


Figure 24: HDMI® Interface Connector Diagram

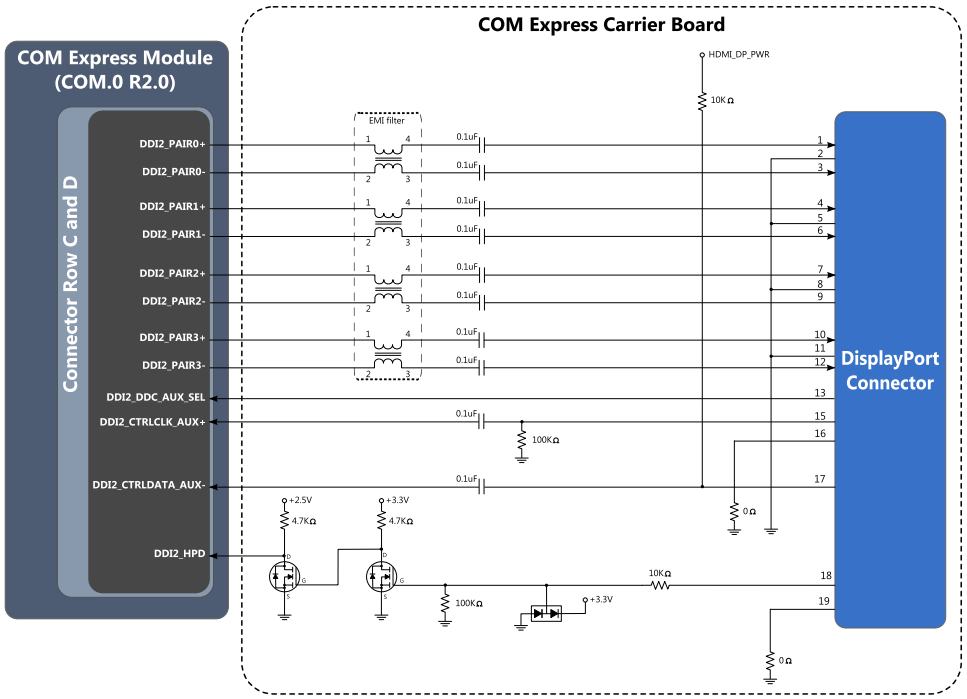


Figure 25: DisplayPort Interface Connector Diagram

4.3.2.1. DDI Layout and Routing Recommendations

The layout and routing recommendations for the DDI interface in COM Express carrier board are listed below:

- Differential pair should be all referenced to ground.
- Each differential pairs signal should route to parallel to each other with the same trace length.
- Route the DDI pairs on a single layer adjacent to a ground plane.

Signal Group	Signal Name	Termination Option	Routing Topology	Terminal Type
Differential Pair	DDI0_PAIR[5:0]+	None	Point to Point	None
	DDI0_PAIR[5:0]-			
	DDI2_PAIR[3:0]+			
	DDI2_PAIR[3:0]-			
	DDI3_PAIR[3:0]+			
	DDI3_PAIR[3:0]-			
Single-ended	DDI0_HPD	None	Point to Point	None
	DDI2_HPD			
	DDI3_HPD			
	DDI2_CTRLCLK_AUX+	None	Point to Point	None
	DDI3_CTRLCLK_AUX+			
	DDI2_CTRLDATA_AUX-			
	DDI3_CTRLDATA_AUX-			

Table 17: DDI Interface Termination Option and Routing Topology

Signal Grouping	Signal Name	Trace Impedance	Trace (Width : Spacing)	Spacing to Other Signal
Differential Pair	DDI0_PAIR[5:0]+	85Ω ± 15%	15 : 5 : 6 : 5 : 15	15 mil
	DDI0_PAIR[5:0]-			
	DDI2_PAIR[3:0]+			
	DDI2_PAIR[3:0]-			
	DDI3_PAIR[3:0]+			
	DDI3_PAIR[3:0]-			
Single-ended	DDI0_HPD	50Ω	5 : 6	6 mil
	DDI2_HPD			
	DDI3_HPD			
	DDI2_CTRLCLK_AUX+	50Ω	5 : 6	6 mil
	DDI3_CTRLCLK_AUX+			
	DDI2_CTRLDATA_AUX-			
	DDI3_CTRLDATA_AUX-			

Table 18: DDI Interface Trace Properties

Signal Grouping	Signal Name	Routing Layer	Trace Mismatch	Accumulated Trace Length
Differential Pair	DDI0_PAIR[5:0]+	Top or Bottom	< 100 mil	< 6"
	DDI0_PAIR[5:0]-			
	DDI2_PAIR[3:0]+			
	DDI2_PAIR[3:0]-			
	DDI3_PAIR[3:0]+			
	DDI3_PAIR[3:0]-			
Single-ended	DDI0_HPD	Top or Bottom	-	-
	DDI2_HPD			
	DDI3_HPD			
	DDI2_CTRLCLK_AUX+	Top or Bottom	-	-
	DDI3_CTRLCLK_AUX+			
	DDI2_CTRLDATA_AUX-			
	DDI3_CTRLDATA_AUX-			

Table 19: DDI Interface Layout Guidelines

Note:
We recommend the usage of a re-driver for some of the high speed interconnects including, but not limited to the DisplayPort and HDMI®. Please contact VIA FAE for additional information.

4.4. VGA Interface

The analog VGA interface signals defined in the connector row B of the COM Express specification.

4.4.1. VGA Signal Definition

Analog Red, Green and Blue (RGB) signals, Horizontal Sync (HSYNC), Vertical Sync (VSYNC) and I²C data control are the group of signals for the VGA interface implementation.

Signal Name	Pin #	I/O	Description	D-Sub 15-pin Connector	Type
VGA_RED	B89	O	Red component of analog DAC monitor	1	6 and 2
VGA_GRN	B91	O	Green component of analog DAC monitor	2	
VGA_BLU	B92	O	Blue component of analog DAC monitor	3	
VGA_HSYNC	B93	O	Horizontal sync output to VGA monitor	13	
VGA_VSYNC	B94	O	Vertical sync output to VGA monitor	14	
VGA_I2C_CK	B95	O	DDC clock line	15	
VGA_I2C_DAT	B96	IO	DDC data line	12	
GND			Ground	5, 8, 10	
Power			5V DDC supply voltage for monitor EEPROM	9	
NC			No connection	4, 11	

Table 20: VGA Signal Descriptions

4.4.2. VGA Reference Schematics

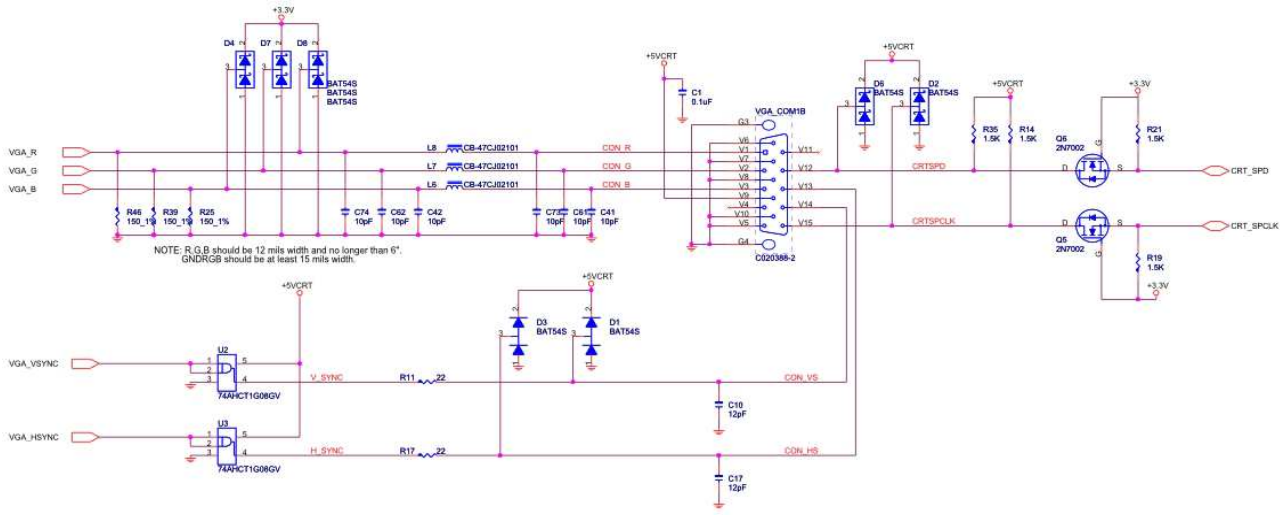


Figure 26: VGA Interface Connector Example

4.4.2.1. VGA Interface Topology

Analog Red, Green and Blue (RGB) traces should be designed to be as short as possible. The diagram below, the RGB outputs are current sources and therefore require 150Ω ± 1% load resistors from each RGB line to GND to create the output voltage (approximately 0 to 0.7 V). These resistors should be placed near the VGA port (a 15-pin D-Sub connector). The 22Ω series damping resistors for HSYNC and VSYNC should be placed near the D-Sub connector.

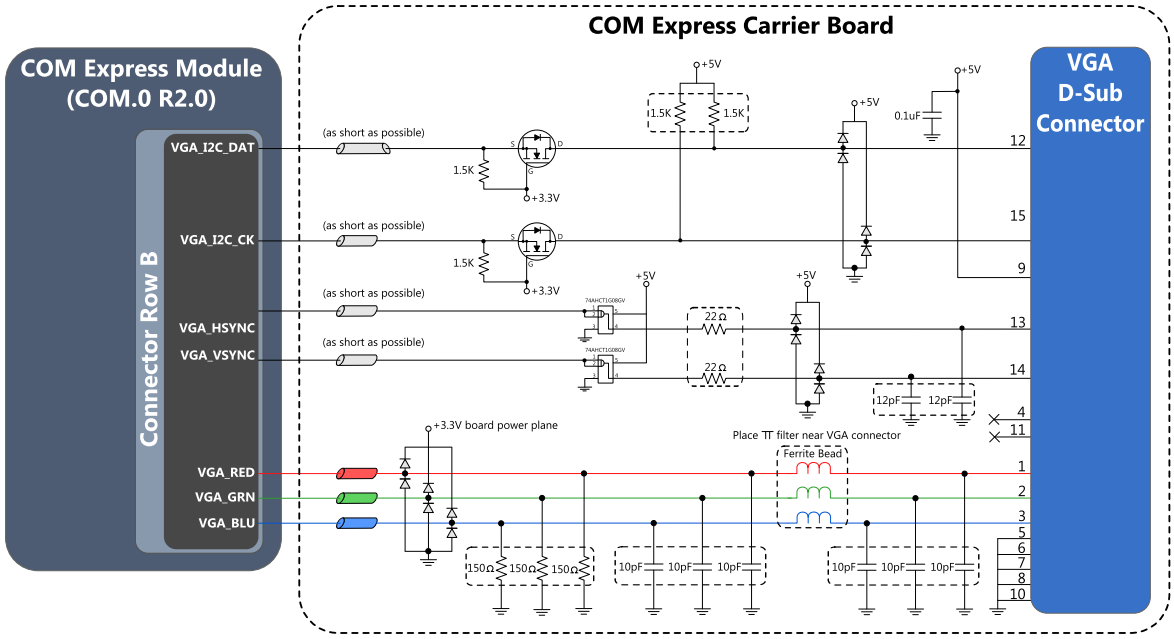


Figure 27: VGA Interface Sample Diagram

Note:
The ferrite beads used for the RGB signals should have high frequency characteristics. (75Ω at 100 MHz).

4.4.2.2. VGA Layout and Recommendations

The layout and routing recommendations for the VGA interface trace signals in COM Express Carrier Board are listed below:

- RGB signal traces should be designed to be as short as possible.
- In order to maximize noise rejection characteristics of the RGB video outputs, it is then recommended to route the RGB video outputs on the top layer over a solid ground plane.
- The routing for the RGB signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends and jogs)
- Route the RGB trace signals and two sync signals (HSYNC and VSYNC) as a single-ended signal with a trace impedance of 75Ω.
- RGB signals should be connected to their each respective π-filter and to the VGA connector, and then 150Ω ± 1% impedance should be strictly applied.
- To maximize the effectiveness of the EMI filtering, it is recommended to put the π-filter near to the VGA connector.

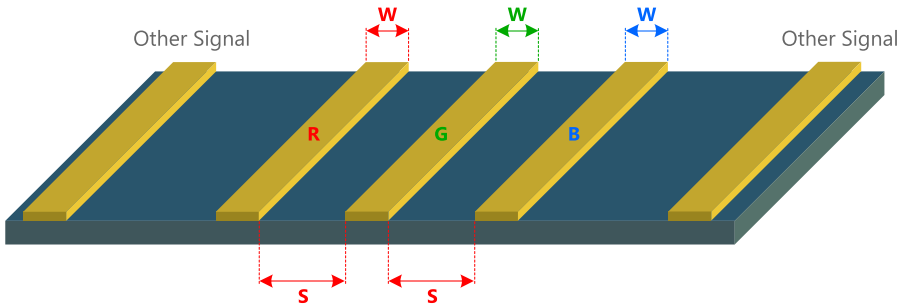


Figure 28: Recommended RGB Trace Properties

Signal Group	Signal Name	Trace (Width : Spacing)	Trace Impedance	Spacing in Other Group
Analog	VGA_AR	10 : 10	37.5Ω ± 15%	20 mil
	VGA_AG			
	VGA_AB			
Control	VGA_HSYNC	5 : 10	55Ω ± 15%	20 mil
	VGA_VSYNC			
	VGA_I2C_DATA			
	VGA_I2C_CK			

Table 21: VGA Interface Trace Properties

Signal Group	Signal Name	Termination Option	Routing Topology
Analog	VGA_AR	Pull-down	Point-to-Point
	VGA_AG		
	VGA_AB		
Control	VGA_HSYNC	None	Point-to-Point
	VGA_VSYNC		
	VGA_I2C_DATA		
	VGA_I2C_CK		

Table 22: VGA Interface Termination Option and Routing Topology

Signal Group	Signal Name	Routing Layer	Accumulated Trace Impedance	Trace Length Mismatch
Analog	VGA_AR	Top or Bottom	< 8"	< 0.5"
	VGA_AG			
	VGA_AB			
Control	VGA_HSYNC	Top or Bottom	< 15"	None
	VGA_VSYNC			
	VGA_I2C_DATA			
	VGA_I2C_CK			

Table 23: VGA Interface Layout Guidelines

Notes:

1. **Analog signal:** the analog trace length in VIA COM Express module is approximately 3.5" therefore the analog trace length in the carrier board should not be longer than 4".
2. **Control signal:** the control trace length in VIA COM Express Module is approximately 3.5" therefore the Control trace length in the carrier board should not be longer than 11".

4.5. LVDS Interface

The LVDS interface in the VIA COM Express module enables displaying graphics on LVDS and flat panel displays using a dual-channel LVDS. The dual channel LVDS supports 18-bit and 24-bit interfaces.

The LVDS signal interface consists of four differential data pairs and one differential clock pair for each channel and five single-ended support signals. The included five single-ended signals are used for LVDS power enable, backlight control, enable lines and I^2C interface.

4.5.1. LVDS Signal Definition

The LVDS interface signals are implemented in connector A-B.

Signal Name	Pin #	I/O	Description	Type
LVDS_A0+	A71	O	LVDS channel A differential signal pair 0	10, 6, and 2
LVDS_A0-	A72			
LVDS_A1+	A73	O	LVDS channel A differential signal pair 1	
LVDS_A1-	A74			
LVDS_A2+	A75	O	LVDS channel A differential signal pair 2	
LVDS_A2-	A76			
LVDS_A3+	A78	O	LVDS channel A differential signal pair 3	
LVDS_A3-	A79			
LVDS_A_CLK+	A81	O	LVDS channel A differential clock pair	
LVDS_A_CLK-	A82			
LVDS_B0+	B71	O	LVDS channel B differential signal pair 0	6 and 2
LVDS_B0-	B72			
LVDS_B1+	B73	O	LVDS channel B differential signal pair 1	
LVDS_B1-	B74			
LVDS_B2+	B75	O	LVDS channel B differential signal pair 2	
LVDS_B2-	B76			
LVDS_B3+	B77	O	LVDS channel B differential signal pair 3	
LVDS_B3-	B78			
LVDS_B_CLK+	B81	O	LVDS channel B differential clock pair	
LVDS_B_CLK-	B82			
LVDS_VDD_EN	A77	O	LVDS flat panel power enable	10, 6 and 2
LVDS_BLKT_EN	B79	O	LVDS flat panel backlight enable	
LVDS_BLKT_CTRL	B83	O	LVDS flat backlight brightness control	
LVDS_I2C_CK	A83	O	DDC I^2C clock signal for detection and control	
LVDS_I2C_DAT	A84	IO	DDC I^2C data signal for detection and control	

Table 24: LVDS Signal Descriptions

4.5.2. LVDS Reference Schematics

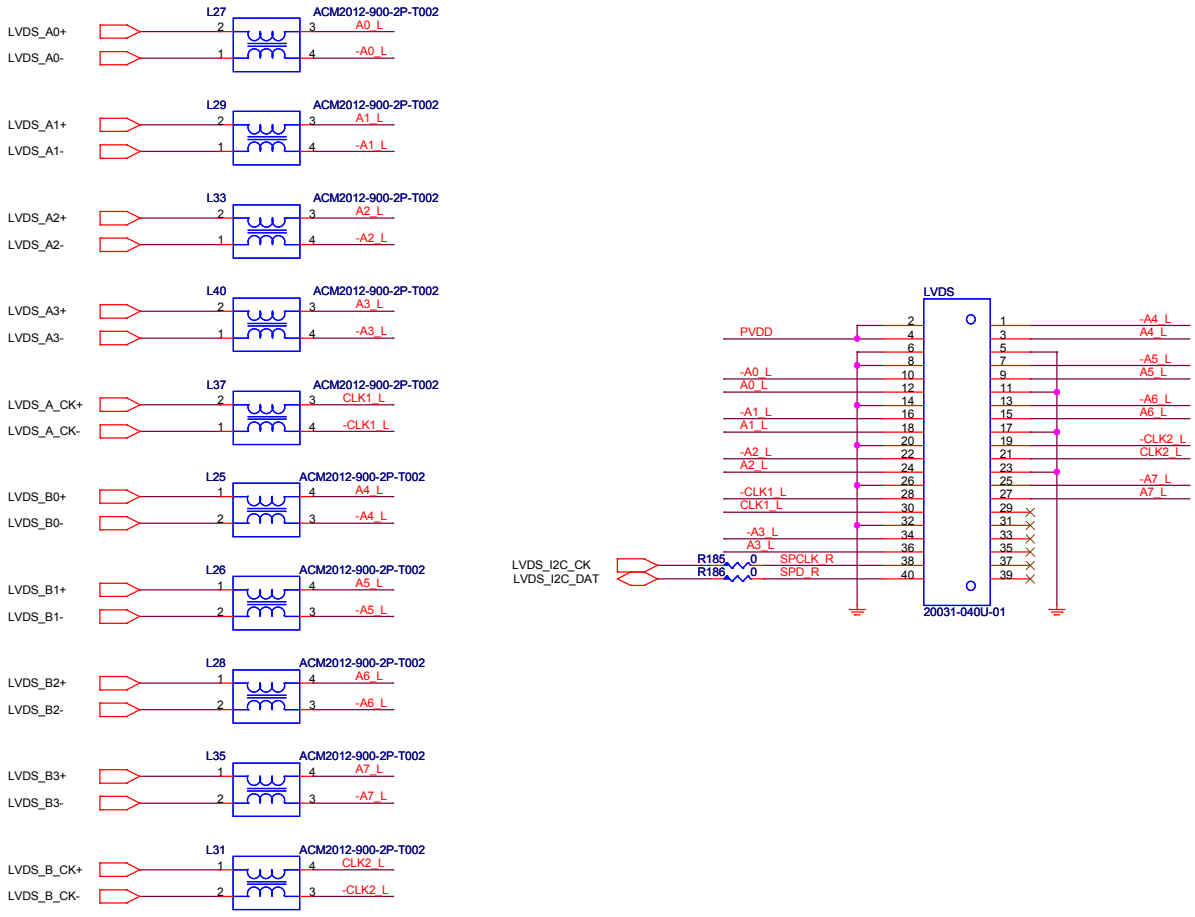


Figure 29: LVDS Connector Example

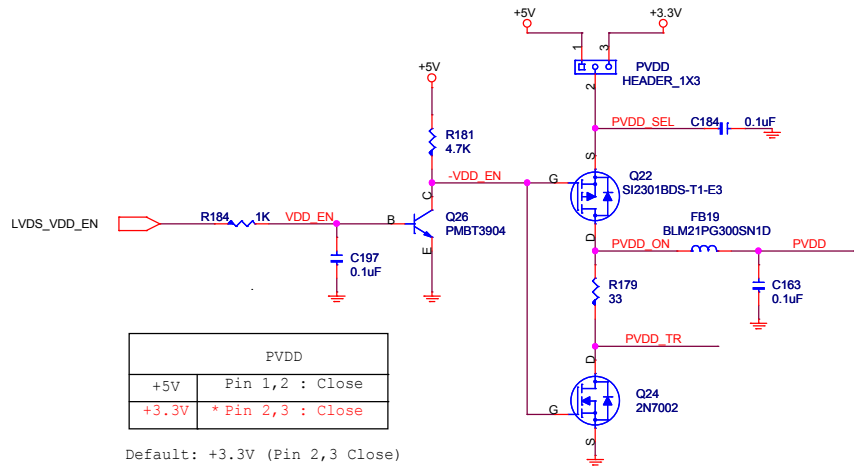


Figure 30: LVDS Panel Power

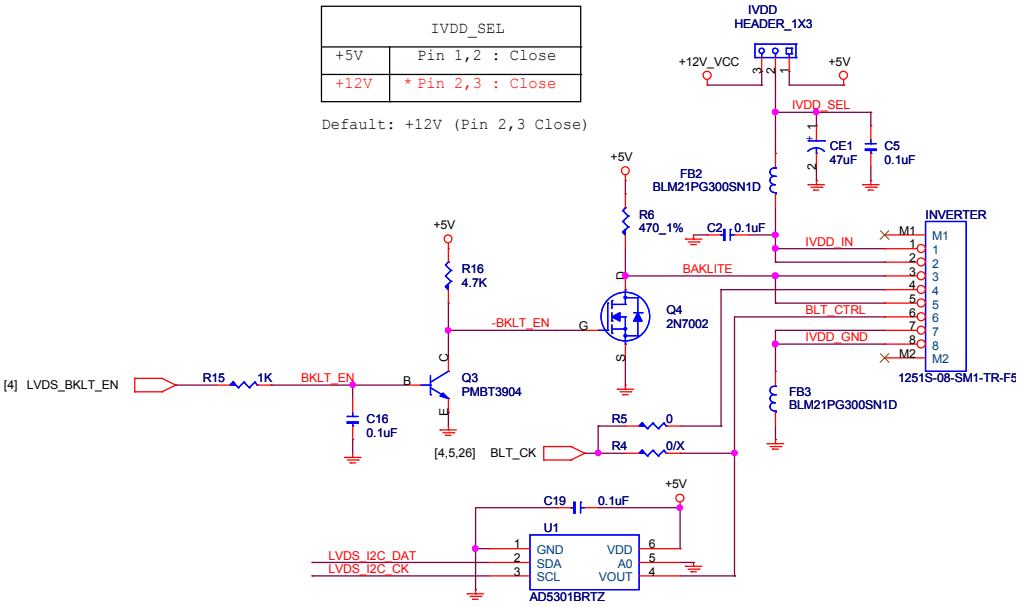


Figure 31: LVDS Backlight

4.5.2.1. LVDS Interface Topology

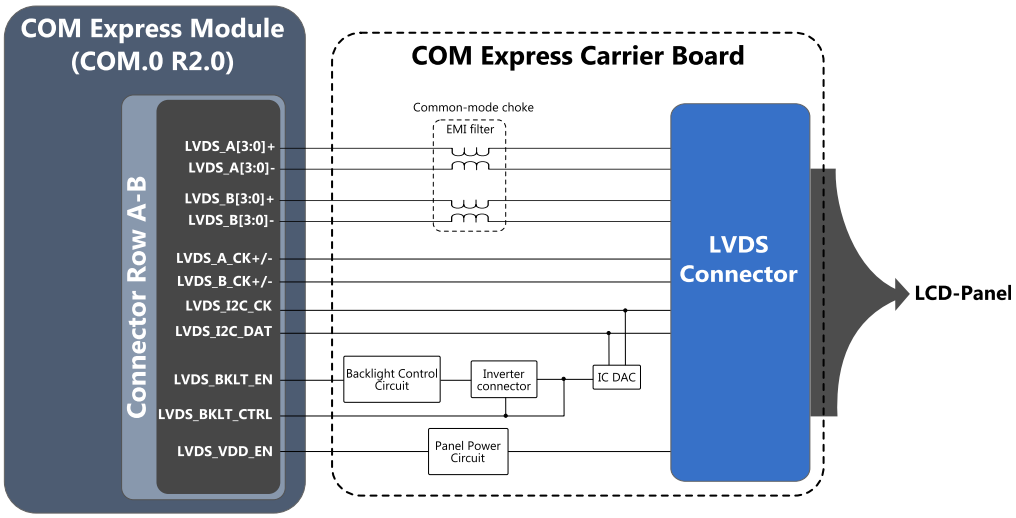


Figure 32: LVDS Interface Sample Diagram

4.5.2.2. LVDS Layout and Routing Recommendations

The layout and routing recommendations for the LVDS interface in COM Express Carrier board are listed below:

- Differential pairs should all be referenced to ground.
- Each differential pair signal (LVDS_A±, LVDS_B±) and clock differential pair (LVDS_A_CK±, LVDS_B_CK±) should be routed parallel to each other with the same trace length.
- Clock differential pair signals (LVDS_A_CK±, LVDS_B_CK±) should be length matched <20 mil.
- Route the LVDS pairs on a single layer adjacent to a ground plane.

Signal Group	Signal Name	Termination Option	Routing Topology	Terminal Type
Differential Pair	LVDS_A[3:0]+	None	Point to Point	None
	LVDS_A[3:0]-			
	LVDS_B[3:0]+			
	LVDS_B[3:0]-			
	LVDS_A_CLK+			
	LVDS_A_CLK-			
	LVDS_B_CLK+			
	LVDS_B_CLK-			
Single-ended	LVDS_BLKT_CTRL	None	Point to Point	None
	LVDS_I2C_CK			
	LVDS_I2C_DAT			
	LVDS_VDD_EN	None	Point to Point	None
	LVDS_BLKT_EN			

Table 25: LVDS Interface Termination Option and Routing Topology

Signal Group	Signal Name	Trace Impedance	Trace (Width : Spacing)	Spacing to Other Signal
Differential Pair	LVDS_A[3:0]+	100Ω ± 15%	20 : 5 : 8 : 5 : 20	20 mil
	LVDS_A[3:0]-			
	LVDS_B[3:0]+			
	LVDS_B[3:0]-			
	LVDS_A_CLK+	100Ω ± 15%	20 : 5 : 8 : 5 : 20	20 mil
	LVDS_A_CLK-			
	LVDS_B_CLK+			
	LVDS_B_CLK-			
Single-ended	LVDS_BLKT_CTRL	55Ω	5 : 8	8 mil
	LVDS_I2C_CK			
	LVDS_I2C_DAT			
	LVDS_VDD_EN	55Ω	5 : 8	8 mil
	LVDS_BLKT_EN			

Table 26: LVDS Interface Trace Properties

Signal Group	Signal Name	Routing Layer	Trace Mismatch	Accumulated Trace Length
Differential Pair	LVDS_A[3:0]+	Top or Bottom	< 100 mil	< 6.5"
	LVDS_A[3:0]-			
	LVDS_B[3:0]+			
	LVDS_B[3:0]-			
	LVDS_A_CLK+	Top or Bottom	< 100 mil	< 6.5"
	LVDS_A_CLK-			
	LVDS_B_CLK+			
	LVDS_B_CLK-			
Single-ended	LVDS_BLKT_CTRL	Top or Bottom	-	-
	LVDS_I2C_CK			
	LVDS_I2C_DAT			
	LVDS_VDD_EN	Top or Bottom	-	-
	LVDS_BLKT_EN			

Table 27: LVDS Interface Layout Guidelines

Note:
The LVDS trace length in VIA COM Express module is approximately 4.5". Therefore, the LVDS trace length in the carrier board should not be longer than 1.5".

4.6. Digital Video Port (DVP) Interface

The DVP interface is a parallel bus signals provided for interfacing DVP slot or an external digital TV Encoder/DVI transmitter. The Digital Video Port is a VIA proprietary interface and available only in VIA COM Express Type 6 and Type 2 modules.

4.6.1. DVP Signal Definition

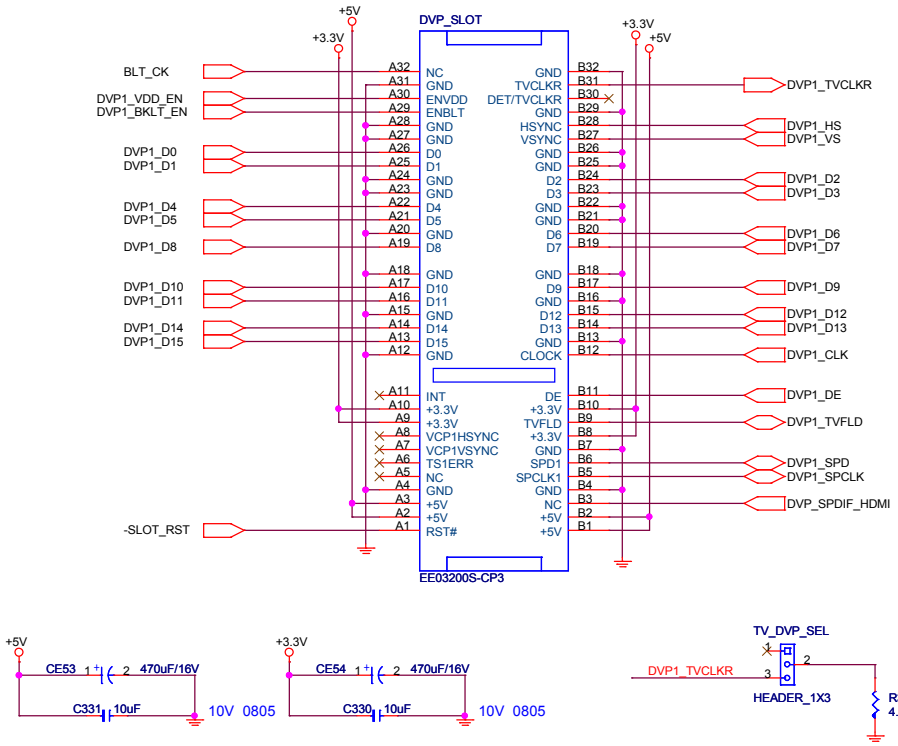
The DVP interface signals are implemented in connector C-D.

Signal Name	Pin #	I/O	Description	Type
DVP1_D0	C78	O	Digital Video Port 1 Data 0.	6 and 2
DVP1_D1	D78	O	Digital Video Port 1 Data 1.	
DVP1_D2	C79	O	Digital Video Port 1 Data 2.	
DVP1_D3	D79	O	Digital Video Port 1 Data 3.	
DVP1_D4	C81	O	Digital Video Port 1 Data 4.	
DVP1_D5	D81	O	Digital Video Port 1 Data 5.	
DVP1_D6	C82	O	Digital Video Port 1 Data 6.	
DVP1_D7	D82	O	Digital Video Port 1 Data 7.	
DVP1_D8	C85	O	Digital Video Port 1 Data 8.	
DVP1_D9	D85	O	Digital Video Port 1 Data 9.	
DVP1_D10	C86	O	Digital Video Port 1 Data 10.	
DVP1_D11	D86	O	Digital Video Port 1 Data 11.	
DVP1_D12	C88	O	Digital Video Port 1 Data 12.	
DVP1_D13	D88	O	Digital Video Port 1 Data 13.	
DVP1_D14	C89	O	Digital Video Port 1 Data 14.	
DVP1_D15	D89	O	Digital Video Port 1 Data 15.	
DVP1_DE	C91	O	Digital Video Port 1 Data Enable.	
DVP1_VS	D92	O	Digital Video Port 1 Vertical Sync.	
DVP1_HS	C94	O	Digital Video Port 1 Horizontal Sync.	
DVP1_TVFLD	C95	IO	Digital Video Port 1 TV Field Out.	
DVP1_TVCLKR	D91	I	Digital Video Port 1 TV Return Clock.	
DVP1_CLK	D94	O	Digital Video Port 1 Clock.	
DVP1_SPD	C98	IO	Digital Video Port 1 I²C Data.	
DVP1_SPCLK	C99	IO	Digital Video Port 1 I²C Clock.	
DVP1_VDD_EN	D98	O	Enable Panel VDD Power.	
DVP1_BKLT_EN	D99	O	Enable Panel Back Light.	

Table 28: DVP Signal Descriptions

Note:
The DVP interface is not defined in standard COM Express Specification.

4.6.2. DVP Reference Schematics



TV_DVP_SEL	DVP1TVCLKR function selection
1-2	TTL/TV from DVP
2-3*	Plug detection from DVP

Figure 33: DVP Slot Example

4.6.2.1. DVP Interface Topology

The topology example below shows the DVP signal interface from a VIA COM Express (Type 6/Type 2) module connected to the DVP slot, external digital TV encoder, external DVI transmitter and TTL Panel connector.

The DVP slot is designed for a TV encoder/DVI transmitter add-in card. The DVP slot enables the connection of a TV monitor for displaying graphics on DVI flat panel.

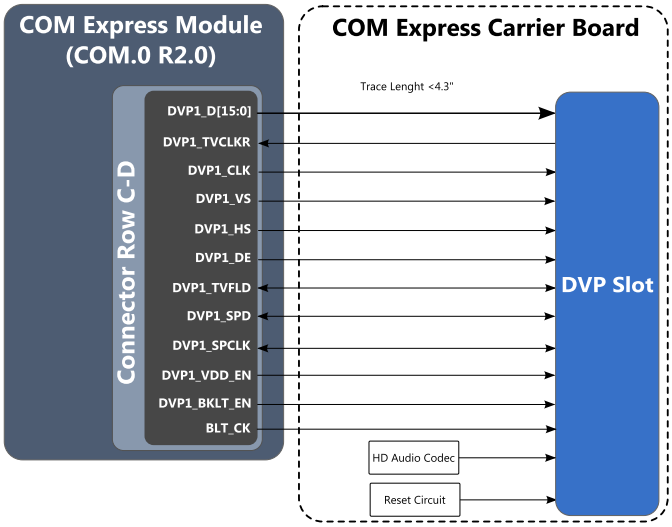


Figure 34: DVP Slot Interface Diagram

By using a digital TV encoder, PC images can be displayed on a TV set. The TV-Out interface example connected to an external TV encoder (or compatible device) is shown in Figure 35. TV output is generated whenever the clock input from the encoder is present to the TV_CLK.

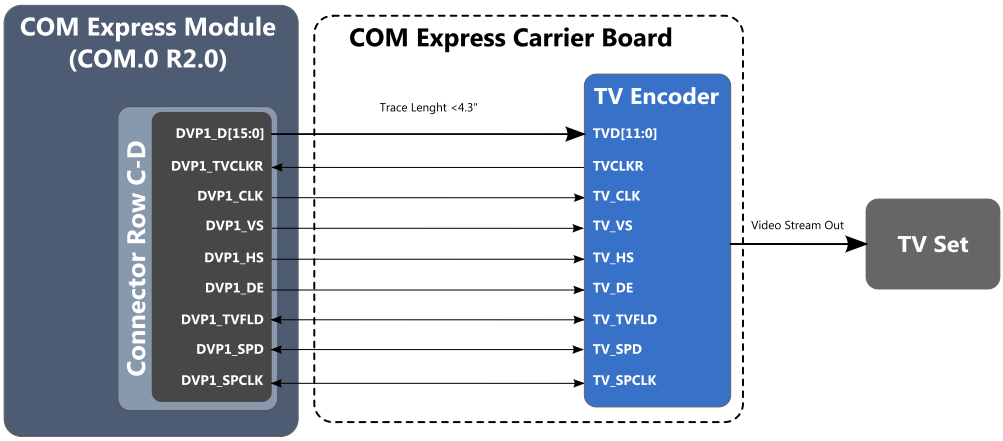


Figure 35: Digital TV-out Interface using External TV Encoder Implementation

One of the functions of the VIA COM Express module is displaying graphics on DVI flat panels (using a DVP 12-bit digital interface DVP_D[11:00] to an external encoder or a DVI transmitter). The DVI technology can transfer data, clock, and control signals from the host graphics controller to high resolution, high color flat-panel-display-based monitors. This interface example below uses the VIA VT1632A DVI transmitter chip (refer to the VT1632A data sheet and application notes for more details). Special attention needs to be paid during voltage conversion of DVI hot plug (+5V) to +3.3V. A single pixel per clock interface example supporting the industry standard Digital Flat Panel (DFP) interface or Digital Video Interface (DVI) is shown in figure below.

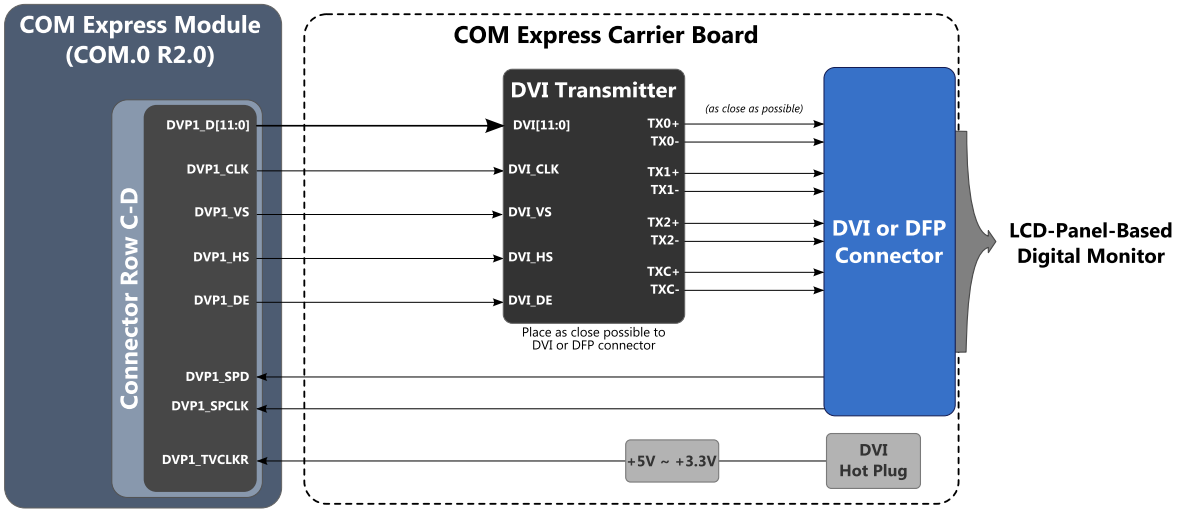


Figure 36: Digital Panel Interface using External DVI Transmitter Implementation

Another feature supported by the VIA COM Express module is displaying graphics on TTL LCD panel monitors through the TTL panel (using an DVP digital interface DVP_D[15:00], DVP_DE, DVP_TVFLD, DVP_VS, DVP_CLK and DVP_TVCLKR).

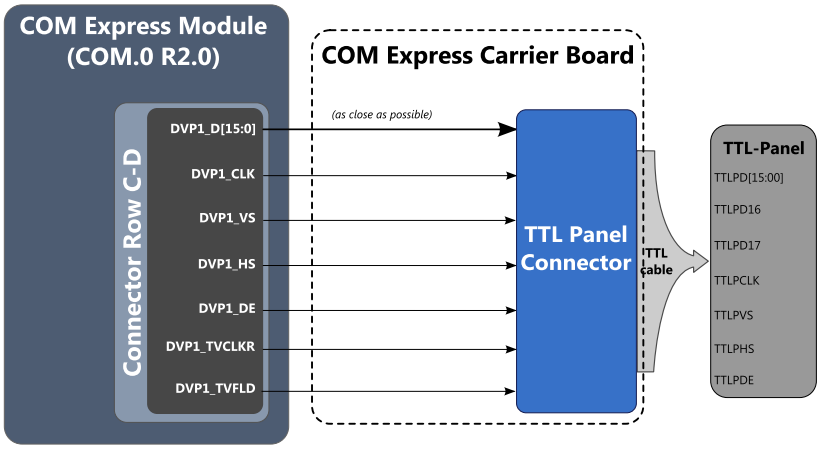


Figure 37: TTL Panel Interface using External TTL Panel Implementation

4.6.3. Digital Video Port Layout and Routing Recommendation

- Route traces to minimum whenever possible.
- Place the DVI transmitter or TV Encoder as close to connector (LCD/ DVI /TV) as possible.
- Each trace should route to parallel to each other with the same trace length.
- The spacing of trace must be equal at all times (in parallel), even during trace bending and serpentine topology.
- All trace must be routed on the same layer with maximum of one signal layer change allowed.
- To minimize signal crosstalk, wider spacing is recommended wherever possible between traces.
- It is always best to reduce the line mismatch to add to the timing margin. In other words, a balanced topology can match the trace lengths within the groups to minimize skew.

Signal Group	Signal Name	Termination Option	Routing Topology	Termination Type
Data Bus	DVP1_D[15:00]	None	Point-to-Point	None
Control	DVP1_DE	None	Point-to-Point	None
	DVP1_VS			
	DVP1_HS			
	DVP1_TVFLD			
	DVP1_TVCLKR			
	DVP1_CLK			
	DVP1_SPD			
	DVP1_SPCLK			
	DVP1_VDD_EN			
	DVP1_BKLT_EN			
	BLT_CK			

Table 29: DVP Interface Termination Option and Routing Topology

Signal Group	Signal Name	Signal Type	Trace (Width : Spacing)	Trace Impedance	Spacing to Other Group
Data Bus	DVP1_D[15:00]	Single-ended	5 : 10	55Ω ± 10%	15 mil
Control	DVP1_DE	Single-ended	5 : 10	55Ω ± 10%	15 mil
	DVP1_VS				
	DVP1_HS				
	DVP1_TVFLD				
	DVP1_TVCLKR				
	DVP1_CLK				
	DVP1_SPD				
	DVP1_SPCLK				
	DVP1_VDD_EN				
	DVP1_BKLT_EN				
	BLT_CK				

Table 30: DVP Interface Trace Properties

Signal Group	Signal Name	Routing Layer	Trace Length Mismatch	Accumulated Trace Length
Data Bus	DVP1_D[15:00]	Top or Bottom	500 mil	≤ 9″
Control	DVP1_DE	Top or Bottom	500 mil	≤ 9″
	DVP1_VS			
	DVP1_HS			
	DVP1_TVFLD			
	DVP1_TVCLKR			
	DVP1_CLK			
	DVP1_SPD			
	DVP1_SPCLK			
	DVP1_VDD_EN			
	DVP1_BKLT_EN			
	BLT_CK			

Table 31: DVP Interface Layout Guidelines

Note:
The DVP interface trace length in VIA COM Express module is approximately ≤ 4.5″. Therefore, the DVP trace length in the carrier board should not be longer than 4.3″.

4.7. Low Pin Count Interface

A Low Pin Count (LPC) interface is provided in VIA COM Express modules. The LPC interface serves as a bus interface between the COM Express module and the LPC Super I/O chip to add peripheral devices (e.g., mouse, keyboard, parallel port, COM port interface, etc.) on the carrier board design. The LPC Super I/O chip is a controller that allows the integration of low-bandwidth legacy input/output (I/O) components in the system. The data transfer on the LPC bus interface is serialized over a 4-bit bus and uses PCI 33MHz electrical signal characteristics.

4.7.1. LPC Signal Definition

The LPC interface signals are implemented in connector A-B.

Signal Name	Pin #	I/O	Description	Type
LPC_SERIRQ	A50	IO	LPC serial IRQ	10, 6 and 2
LPC_FRAME#	B3	O	LPC frame indicates starts of new cycle or termination of broken cycle	
LPC_AD0	B4	IO	LPC command, address and data	
LCP_AD1	B5	IO		
LPC_AD2	B6	IO		
LPC_AD3	B7	IO		
LPC_DRQ0#	B8	I	LPC encoded DMA/Bus master request	
LPC_DRQ1#	B9	I		
LPC_CLK	B10	O	LPC clock output 33MHz	

Table 32: LPC Signal Descriptions

4.7.2. LPC Reference Schematics

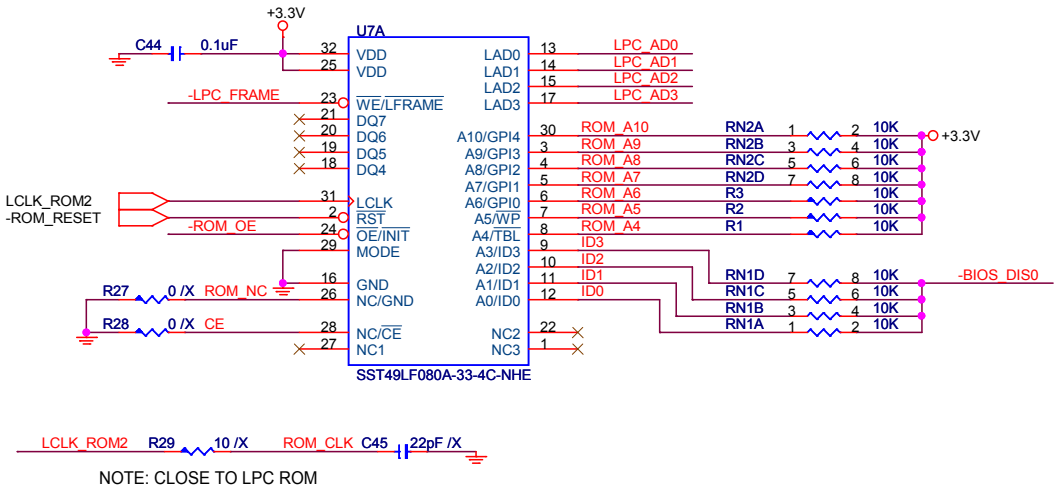


Figure 38: LPC Flash ROM Interface

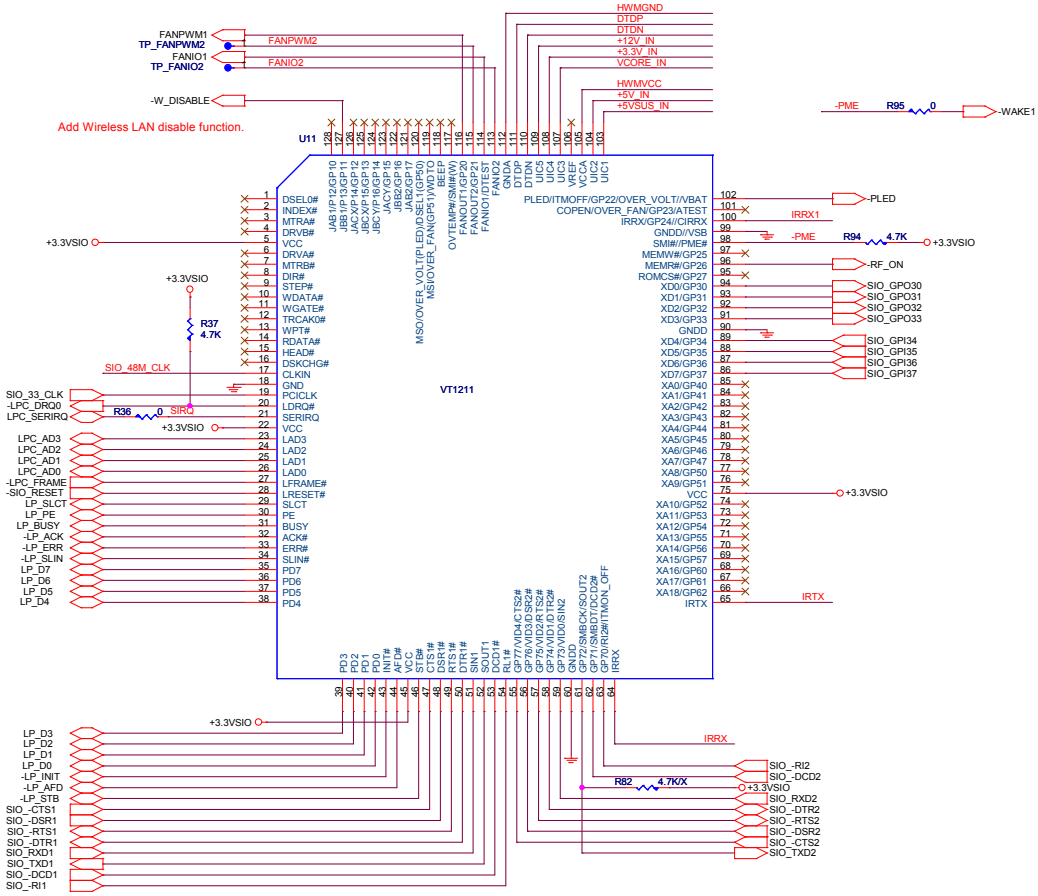


Figure 39: LPC Super I/O Example

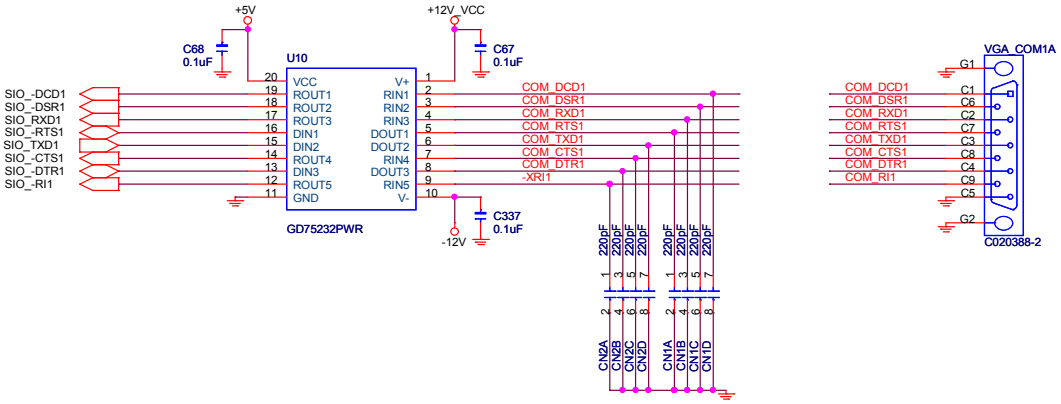


Figure 40: LPC COM Interfaces

4.7.2.1. LPC Interface Topology

The topology example below shows the LPC signal interface from VIA COM Express (Type 10/Type 6/Type 2) module connected to the LPC Super I/O controller.

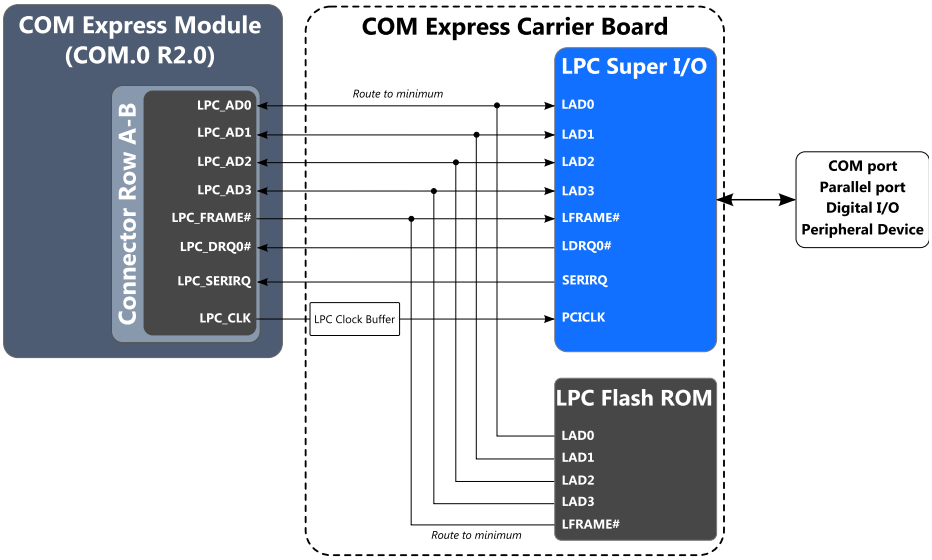


Figure 41: LPC Topology Example

4.7.2.2. LPC Layout and Routing Recommendations

The layout guidelines for the LPC interface are listed below.

- Route traces to minimum whenever possible.
- Route LPC clocks as single-ended with 55Ω trace impedance and referenced to ground.
- One source of the LPC clock comes from COM Express connector. And if there are multiple devices or slots implemented on the carrier board, a zero delay clock buffer is required to expend the number of LPC clocks.

Signal Name	Signal Type	Topology	Routing Layer	Accumulated Trace Length
LPC_AD0	Single-ended	Point to Point	Top or Bottom	< 16"
LPC_AD1				
LPC_AD2				
LPC_AD3				
LPC_FRAME#	Single-ended	Point to Point	Top or Bottom	< 16"
LPC_SERIRQ				
LPC_DRQ0#				
LPC_DRQ1#				
LPC_CLK	Single-ended	Point to Point	Top or Bottom	-

Table 33: LPC Interface Topology, Signal Type and Layout Guidelines

Signal Name	Trace (Width : Spacing)	Trace Impedance	Spacing in Other Group
LPC_AD0	5 : 10	55Ω	-
LPC_AD1			
LPC_AD2			
LPC_AD3			
LPC_FRAME#	5 : 10	55Ω	-
LPC_SERIRQ			
LPC_DRQ0#			
LPC_DRQ1#			
LPC_CLK	5 : 10	55Ω	-

Table 34: LPC Interface Trace Properties

Note:
The LPC interface trace length in VIA COM Express module is approximately 4.7". Therefore, the LPC interface trace length in the carrier board should not longer than 8.4".

4.8. Serial COM Interface

The Serial COM interface is newly defined in the COM.0 R2.0 specifications in response to the demands of the market. The VIA COM Express Type 10 and Type 6 modules offer a Serial COM interface that enables interfacing two Serial COM ports on the carrier board design. The two Serial COM interface bus can support standard RS-232 serial communications.

4.8.1. Serial COM Signal Definition

The Serial COM interface signals are defined in the connector row A.

Signal Name	Pin #	I/O	Description	Type
SER0_TX	A98	O	General purpose serial port 0 transmitter.	10 and 6
SER0_RX	A99	I	General purpose serial port 0 receiver.	
SER1_TX	A101	O	General purpose serial port 1 transmitter.	
SER1_RX	A102	I	General purpose serial port 1 receiver.	

Table 35: Serial COM Signal Descriptions

4.8.2. Serial COM Reference Schematics

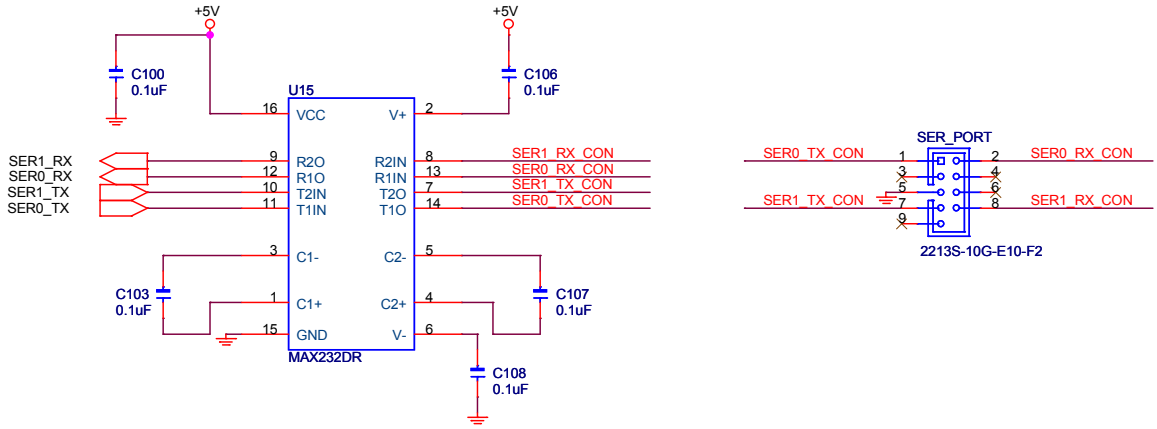


Figure 42: Serial COM port Interface Example

4.8.2.1. Serial COM Interface Topology

The topology example below shows the Serial COM interface signal from VIA COM Express (Type 10 and Type 6) module connected to the Serial COM port.

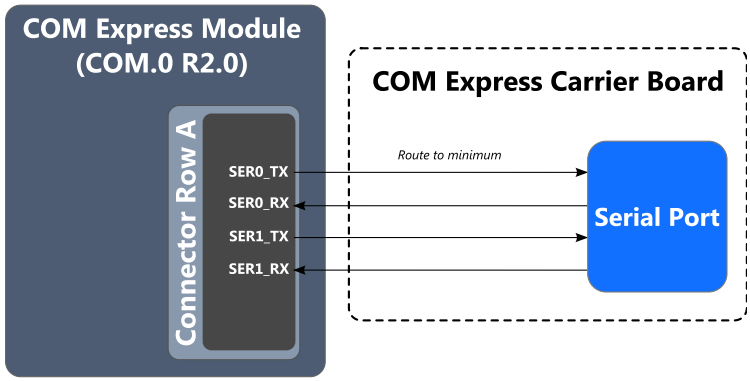


Figure 43: Serial COM port Interface Topology Example

4.8.2.2. Serial COM Layout and Routing Recommendations

Signal Name	Signal Type	Topology	Routing Layer	Accumulated Trace Length
SER0_TX	Single-ended	Point to Point	Top or Bottom	< 16"
SER0_RX				
SER1_TX				
SER1_RX				

Table 36: Serial COM Interface Topology, Signal Type and Layout Guidelines

Signal Name	Trace (Width : Spacing)	Trace Impedance	Spacing in Other Group
SER0_TX	5 : 10	55Ω	-
SER0_RX			
SER1_TX			
SER1_RX			

Table 37: Serial COM Interface Trace Properties

4.9. General Purpose I²C Bus Interface

VIA COM Express modules provide a General Purpose I²C interface signal for serial EEPROM memory.

4.9.1. General Purpose I²C Signal Definition

The General Purpose I²C interface signals are defined in the connector row A.

Signal Name	Pin #	I/O	Description	Type
I2C_CK	B33	O	General Purpose I²C Clock Output	10, 6 and 2
I2C_DAT	B34	IO	General Purpose I²C Data I/O line	

Table 38: General Purpose I²C Signal Descriptions

4.9.2. General Purpose I²C Reference Schematics

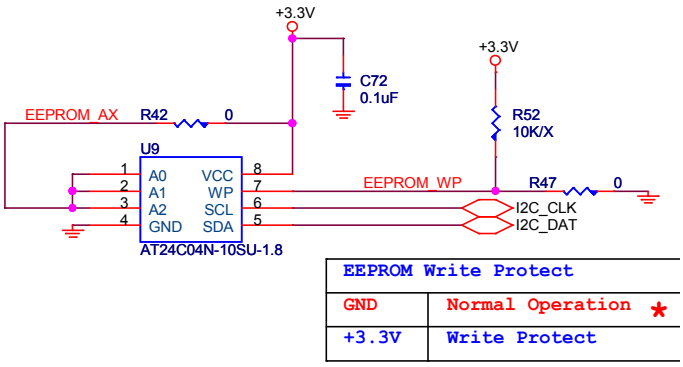


Figure 44: EEPROM Circuitry Reference Example

4.9.2.1. General Purpose I²C Layout and Routing Recommendations

Signal Name	Signal Type	Topology	Routing Layer	Accumulated Trace Length
I2C_CK I2C_DAT	Single-ended	Point to Point	Top or Bottom	-

Table 39: General Purpose I²C Interface Topology, Signal Type and Layout Guidelines

Signal Name	Trace (Width : Spacing)	Trace Impedance	Spacing to Other Group
I2C_CK I2C_DAT	5 : 10	55Ω	-

Table 40: General Purpose I²C Interface Trace Properties

4.10. PCI Interface (Type 2 Only)

The VIA COM Express Type 2 modules have a PCI bus interface that runs at 33MHz and can support up to a maximum of three PCI slots or PCI compliant devices designed on the carrier board. The PCI interface has a daisy chain topology and the signal traces may be laid out on either the component layer (top) or the solder layer (bottom). The PCI interface is only supported in Type 2 modules.

4.10.1. PCI Signal Definition

The PCI interface pin-out signals are implemented in connector C-D.

Signal Name	Pin #	I/O	Description	Type
PCI_AD0	C24	IO	PCI bus multiplexed data and address lines	
PCI_AD1	D22	IO	PCI bus multiplexed data and address lines	
PCI_AD2	C25	IO	PCI bus multiplexed data and address lines	
PCI_AD3	D23	IO	PCI bus multiplexed data and address lines	
PCI_AD4	C26	IO	PCI bus multiplexed data and address lines	
PCI_AD5	D24	IO	PCI bus multiplexed data and address lines	
PCI_AD6	C27	IO	PCI bus multiplexed data and address lines	
PCI_AD7	D25	IO	PCI bus multiplexed data and address lines	
PCI_AD8	D28	IO	PCI bus multiplexed data and address lines	
PCI_AD9	D27	IO	PCI bus multiplexed data and address lines	
PCI_AD10	C29	IO	PCI bus multiplexed data and address lines	
PCI_AD11	D28	IO	PCI bus multiplexed data and address lines	
PCI_AD12	C30	IO	PCI bus multiplexed data and address lines	
PCI_AD13	D29	IO	PCI bus multiplexed data and address lines	
PCI_AD14	C32	IO	PCI bus multiplexed data and address lines	
PCI_AD15	D30	IO	PCI bus multiplexed data and address lines	
PCI_AD16	D37	IO	PCI bus multiplexed data and address lines	
PCI_AD17	C39	IO	PCI bus multiplexed data and address lines	
PCI_AD18	D38	IO	PCI bus multiplexed data and address lines	
PCI_AD19	C40	IO	PCI bus multiplexed data and address lines	
PCI_AD20	D39	IO	PCI bus multiplexed data and address lines	
PCI_AD21	C42	IO	PCI bus multiplexed data and address lines	
PCI_AD22	D40	IO	PCI bus multiplexed data and address lines	2
PCI_AD23	C43	IO	PCI bus multiplexed data and address lines	
PCI_AD24	D42	IO	PCI bus multiplexed data and address lines	
PCI_AD25	C45	IO	PCI bus multiplexed data and address lines	
PCI_AD26	D43	IO	PCI bus multiplexed data and address lines	
PCI_AD27	C46	IO	PCI bus multiplexed data and address lines	
PCI_AD28	D44	IO	PCI bus multiplexed data and address lines	
PCI_AD29	C47	IO	PCI bus multiplexed data and address lines	
PCI_AD30	D45	IO	PCI bus multiplexed data and address lines	
PCI_AD31	C48	IO	PCI bus multiplexed data and address lines	
PCI_C/BE0#	D26	IO	PCI bus byte enable line 0	
PCI_C/BE1#	C33	IO	PCI bus byte enable line 0	
PCI_C/BE2#	C38	IO	PCI bus byte enable line 0	
PCI_C/BE3#	C44	IO	PCI bus byte enable line 0	
PCI_DEVSEL#	C36	IO	PCI bus device select	
PCI_FRAME#	D36	IO	PCI bus frame control line	
PCI_IRDY#	C37	IO	PCI bus initiator ready control line	
PCI_TRDY#	D35	IO	PCI bus target ready control line	
PCI_STOP#	D34	IO	PCI bus STOP control line	
PCI_PAR	D32	IO	PCI bus parity	
PCI_PERR#	C34	IO	Parity error	
PCI_REQ0#	C22	IO	PCI bus master request input line	
PCI_REQ1#	C19	IO	PCI bus master request input line	

PCI_REQ2#	C17	IO	PCI bus master request input line	2
PCI_REQ3#	D20	IO	PCI bus master request input line	
PCI_GNT0#	C20	IO	PCI bus grant output line	
PCI_GNT1#	C18	IO	PCI bus grant output line	
PCI_GNT2#	C16	IO	PCI bus grant output line	
PCI_GNT3#	D19	IO	PCI bus grant output line	
PCI_RESET#	C23	IO	PCI reset output	
PCI_SERR#	D33	IO	System error	
PCI_PME#	C15	IO	PCI power management event	
PCI_IRQA#	C49	IO	PCI interrupt request line A	
PCI_IRQB#	C50	IO	PCI interrupt request line B	
PCI_IRQC#	D46	IO	PCI interrupt request line C	
PCI_IRQD#	D47	IO	PCI interrupt request line D	
PCI_CLK	D50	IO	PCI clock output 33MHz	

Table 41: PCI Signal Descriptions

4.10.2. PCI Reference Schematics

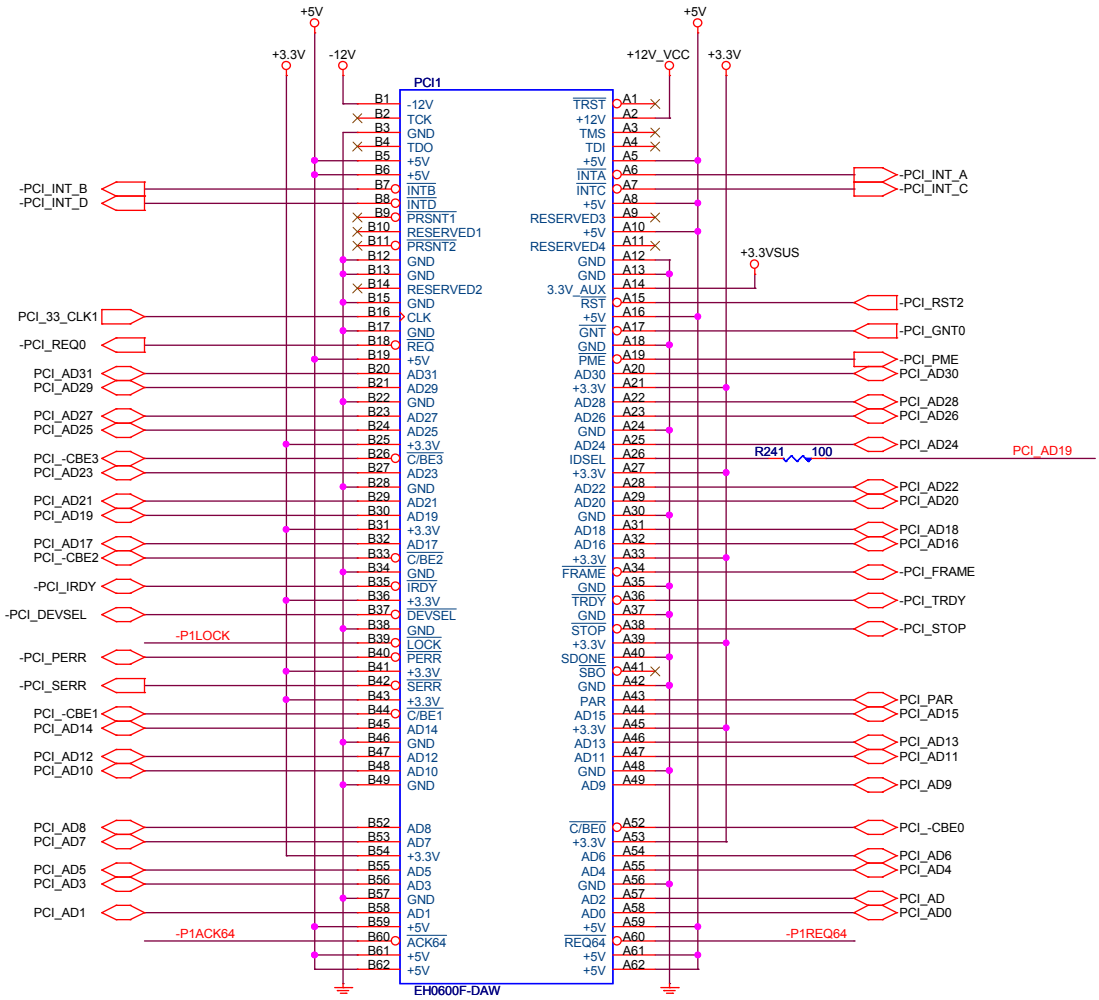


Figure 45: PCI Connector Example

4.10.2.1. PCI Interface Topology

A topology example using three PCI slots on the carrier board connected to the COM Express module is shown in Figure 46. Please note that the number of supported PCI slots will vary according to the design of the carrier board.

The PCI control signals always require pull-up resistors, typically 4.7KΩ pull-up for +5V signaling; on the carrier board to ensure that they do not float during the PCI idle state. Therefore each of the following signals PCI_IRDY#, PCI_TRDY#, PCI_DEVSEL#, PCI_STOP#, PCI_PERR#, PCI_SERR#, PCI_FRAME# and PCI_IRQ[D:A] requires a 4.7KΩ pull-up to +5V. The PCI_REQ[3:0]# and PCI_GNT[3:0]# signals need 4.7KΩ pull-up to +3.3V.

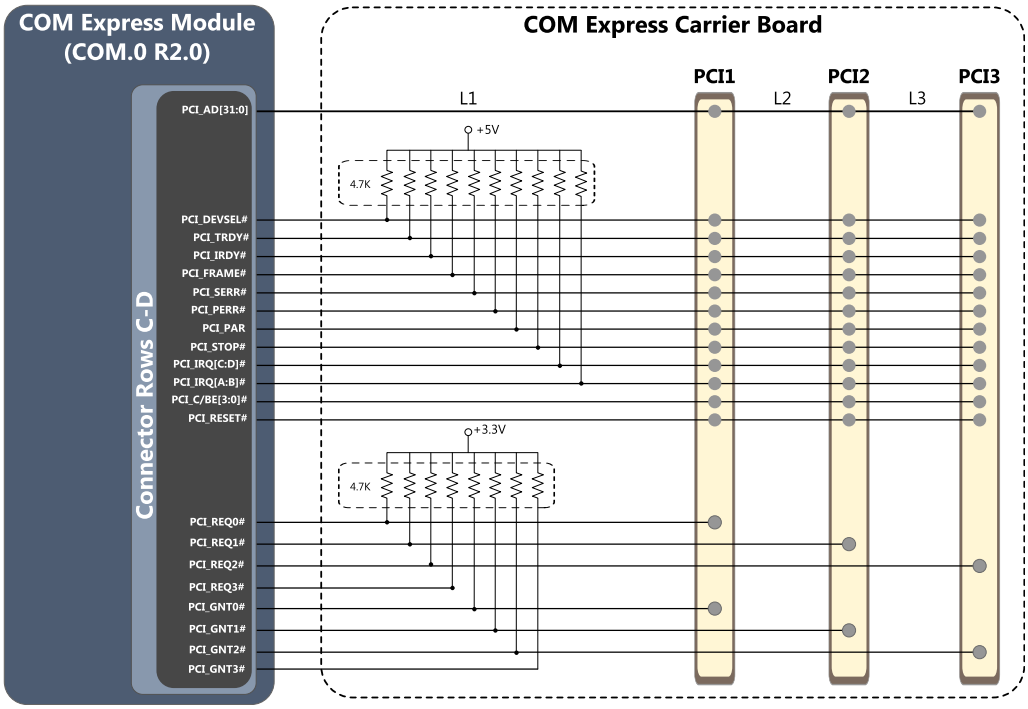


Figure 46: PCI Interface Topology Example

4.10.2.2. PCI Layout and Routing Recommendations

Recommended layout rules for connecting PCI slots to the COM Express module are listed below:

- Routing the PCI clock as single-ended 55Ω trace impedance and referencing to the ground plane is recommended.
- One source of the PCI clock comes from the COM Express connector, and if there are multiple devices or slots implemented on the carrier board, a zero delay clock buffer is required to expend the number of PCI clocks.
- For PCI device-down application, the trace of PCI clock on carrier board should longer than 3.5" from PCI device-up application.
- Signal traces do not need to be matched; nor be serpentine in order to meet the minimum length guidelines.
- Routing to minimum is preferred.

Signal Name	PCI Slots		
	PCI 1	PCI 2	PCI 3
REQ Signals	REQ0#	REQ1#	REQ2#
GNT Signals	GNT0#	GNT1#	GNT2#

Table 42: PCI slot connection

Trace Impedance	No. of PCI Slots	Maximum Trace Length		
		L1	L2	L3
55Ω ± 10%	1	5″ ~ 10″	N/A	N/A
	2	5″ ~ 10″	1″	N/A
	3	5″ ~ 10″	1″	1″

Table 43: PCI Interface Routing Requirements

Signal Grouping	Topology	Routing Layer	Accumulated Trace Length
Single-ended	Daisy Chain	Top or Bottom	< 10″ (Route to minimum)

Table 44: PCI Interface Layout Guidelines

Signal Grouping	Trace Impedance	Trace (Width : Spacing)	Spacing in Other Group
Single-ended	55Ω ± 10%	5 : 5 mil	20 mil

Table 45: PCI Interface Trace Properties

Note:

The PCI trace length in VIA COM Express Type 2 modules is approximately 3.5". Therefore, the PCI trace length in carrier board should not be longer than 6".

4.11. IDE Interface (Type 2 Only)

VIA COM Express Type 2 modules provide the IDE interface signals for interfacing IDE drives. The IDE interface is a disk drive interface that supports one independent enhanced IDE channel. And this IDE channel can supports up to two enhanced IDE devices using the UltraDMA33 / 66 / 100 / 133 IDE devices in a master or slave configuration.

4.11.1. IDE Signal Definition

The corresponding IDE interface signals are defined in connector C-D.

Signal Name	Pin #	I/O	Description	Type
IDE_D0	D7	IO	Bidirectional data to or from IDE device	
IDE_D1	C10	IO	Bidirectional data to or from IDE device	
IDE_D2	C8	IO	Bidirectional data to or from IDE device	
IDE_D3	C4	IO	Bidirectional data to or from IDE device	
IDE_D4	D6	IO	Bidirectional data to or from IDE device	
IDE_D5	D2	IO	Bidirectional data to or from IDE device	
IDE_D6	C3	IO	Bidirectional data to or from IDE device	
IDE_D7	C2	IO	Bidirectional data to or from IDE device	
IDE_D8	C6	IO	Bidirectional data to or from IDE device	
IDE_D9	C7	IO	Bidirectional data to or from IDE device	
IDE_D10	D3	IO	Bidirectional data to or from IDE device	
IDE_D11	D4	IO	Bidirectional data to or from IDE device	
IDE_D12	D5	IO	Bidirectional data to or from IDE device	
IDE_D13	C9	IO	Bidirectional data to or from IDE device	
IDE_D14	C12	IO	Bidirectional data to or from IDE device	2
IDE_D15	C5	IO	Bidirectional data to or from IDE device	
IDE_A0	D13	O	Address line to IDE device	
IDE_A1	D14	O	Address line to IDE device	
IDE_A2	D15	O	Address line to IDE device	
IDE_IOW#	D9	O	Input/Output write line to IDE device	
IDE_IOR#	C14	O	Input/Output read line to IDE device	
IDE_REQ	D8	I	DMA request	
IDE_ACK#	D10	O	DMA acknowledge	
IDE_CS1#	D16	O	Chip select for 1F0h to 1FFh	
IDE_CS3#	D17	O	Chip select for 30F0h to 3FFh	
IDE_IORDY	C13	I	IDE device Input/Output ready input	
IDE_RESET#	D18	O	Reset output to IDE device	
IDE_IRQ	D12	I	Interrupt request from IDE device	
IDE_CBLID#	D77	I	IDE cable type detector	

Table 46: IDE Signal Descriptions

4.11.2. IDE Reference Schematics

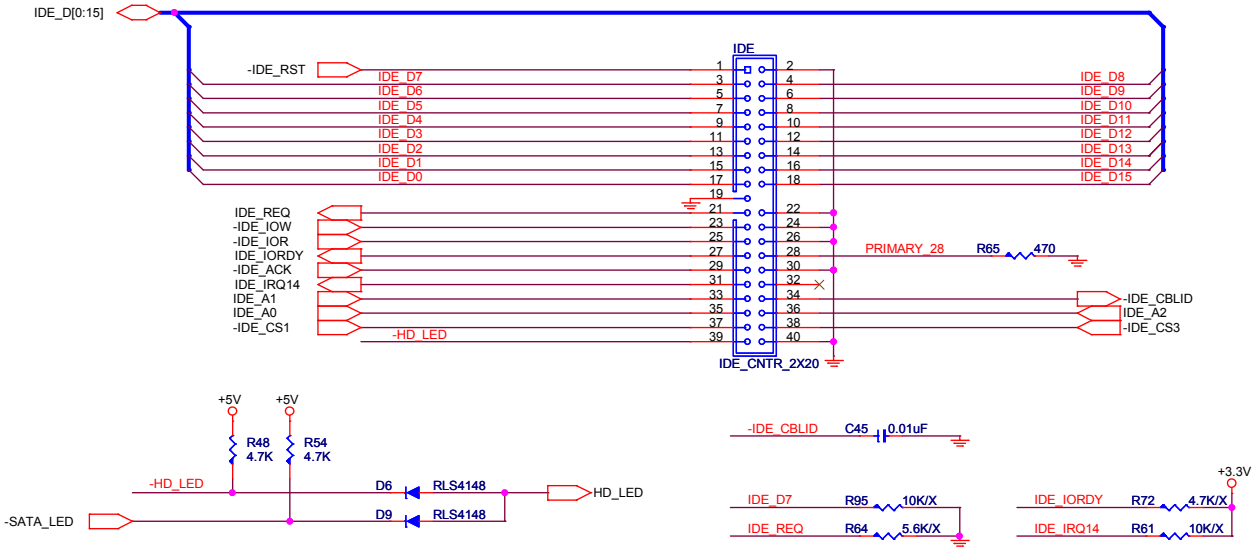
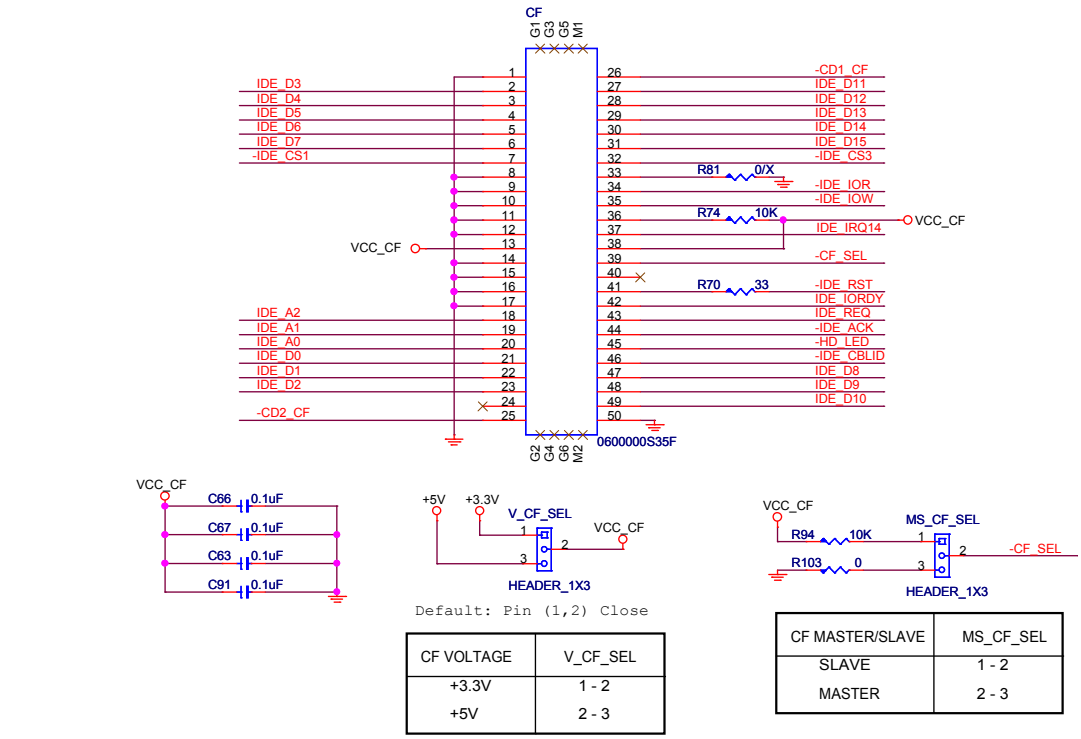


Figure 47: IDE Connector



CF VOLTAGE	V_CF_SEL
+3.3V	1 - 2
+5V	2 - 3

CF MASTER/SLAVE	MS_CF_SEL
SLAVE	1 - 2
MASTER	2 - 3

Figure 48: CF Card Socket

4.11.2.1. IDE Interface Topology

The topology example below shows the IDE interface signal from VIA COM Express Type 2 module connected to two IDE devices: the IDE port and CF card socket. The master-slave setting configuration should be applied if using the IDE connector and CF card socket at the same time.

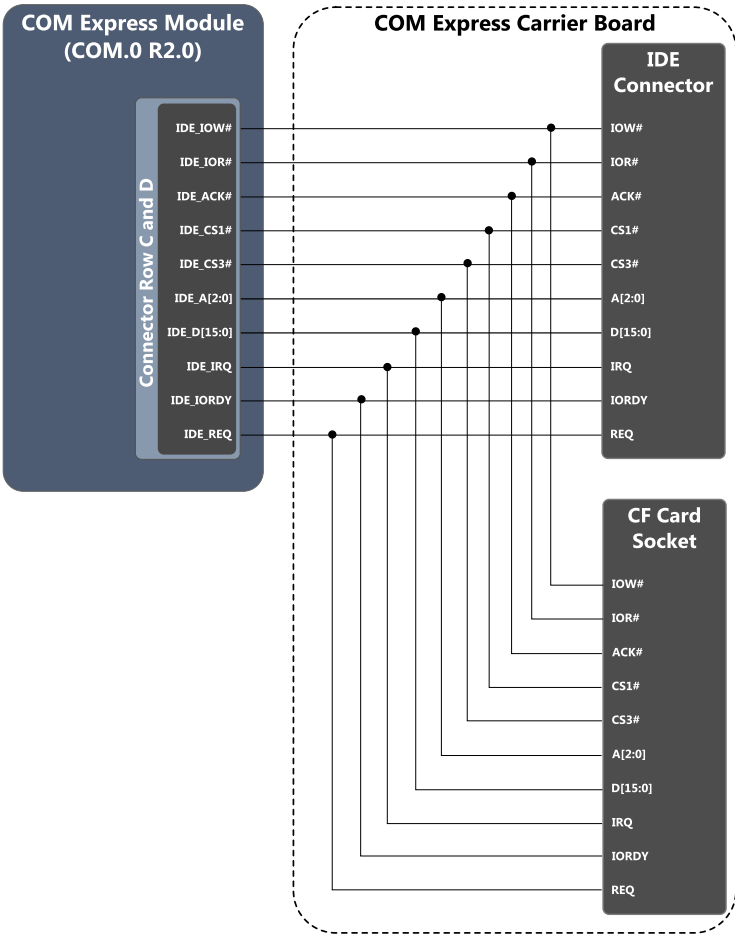


Figure 49: IDE Devices Layout Guidelines

4.11.2.2. IDE Supporting Modes

For IDE supporting modes, transfer rate and cable type; refer to Table 47. The transfer rate for each device can support up to 133 MB/s to cover up to PIO Mode 4, Multiword DMA Mode 2 and Ultra DMA Mode 6. An additional 80-conductor cable is required for all Ultra DMA modes higher than Mode 2. It is interchangeable with the standard (40-conductor) cable for the remaining modes. There is no need for new connectors on host or devices. Comparing to 40-conductor cable, 40 additional lines of the 80-conductor cable interleaved between these original 40 signal/ground lines are all ground.

Supporting Modes	Transfer Rate (MB/s)	Cable Type
PIO	Mode 0: 3.3	40-Conductor
	Mode 1: 5.2	
	Mode 2: 8.3	
	Mode 3: 11.1	
	Mode 4: 16.7	
Multiword DMA	Mode 0: 4.2	40-Conductor
	Mode 1: 13.3	
	Mode 2: 16.7	
Ultra DMA	Mode 0: 16.7	40-Conductor
	Mode 1: 25	
	Mode 2: 33.3 (Ultra DMA 33)	
	Mode 3: 44.4 (Ultra DMA 66)	80-Conductor
	Mode 4: 66.6 (Ultra DMA 66)	
	Mode 5: 100 (Ultra DMA 100)	
	Mode 6: 133 (Ultra DMA 133)	

Table 47: IDE Supporting Modes, Transfer Rate and Cable Type

4.11.2.3. IDE Cable Detection

The 80-conductor cable required by the Ultra DMA66 / 100 / 133 IDE interface is the major difference from the 40-conductor cable of the former standard IDE interface (Ultra DMA33 specification below). For the detection of the 80-conductor cable, pin 34 (-IDE_CBLID) of IDE connector may be used to provide a signal state from an Ultra DMA66 / 100 / 133 device to COM Express module. The COM Express module detects the cable type through BIOS operation with a 0.01 µF capacitor. The Ultra DMA mode 3, 4, 5 and 6 devices will drive –IDE_CBLID low. Then the drive will sample the –IDE_CBLID signal after releasing it. The drive can detect the difference in rise times and it reports the cable type to the module BIOS when it sends the IDENTIFY_DEVICE packet during system boot.

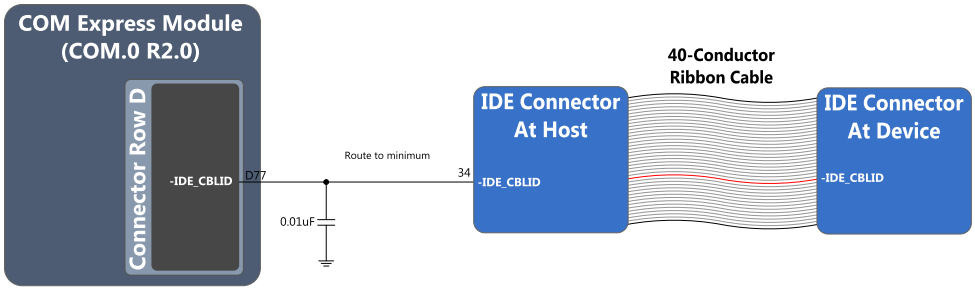


Figure 50: IDE Cable Detection with 40-Conductor Ribbon Cable

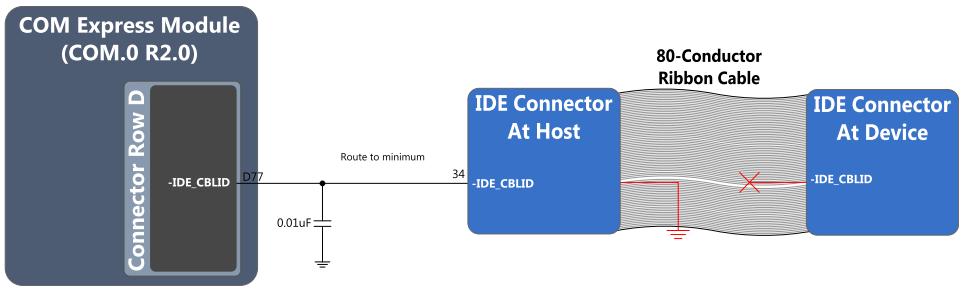


Figure 51: IDE Cable Detection with 80-Conductor Ribbon Cable

4.11.2.4. IDE Layout and Routing Recommendation

With the increase in speed, transmission line effects, signal crosstalk and bus timing issues emerge in the IDE (PATA) related signals. And to eliminate the ringing and reflection caused by the transmission line effect, proper routing, layout and impedance matching must be taken into account.

Recommended layout guidelines for IDE interface are listed below:

- The IDE data lines for Ultra DMA mode operation should be routed as a bus.
- All IDE signal lines should be as short as possible.
- The IDE signals do not require series termination resistors, because the required series resistors are present on the VIA COM Express Module.

Signal Group	Signal Name	Signal Type	Topology
Address	IDE_A[2:0]	Single-ended	Point-to-Point
Data	IDE_D[15:0]	Single-ended	Point-to-Point
	IDE_IORDY		
	IDE_IOR#		
	IDE_IOW#		
Control	IDE_ACK#	Single-ended	Point-to-Point
	IDE_CS1#		
	IDE_CS3#		
	IDE_REQ		
	IDE_IRQ		

Table 48: IDE Interface Signal Type and Routing Topology

Signal Group	Signal Name	Trace (Width : Spacing)	Trace Impedance	Spacing to Other Group
Address	IDE_A[2:0]	5 : 10	55Ω	20 mil
Data	IDE_D[15:0]	5 : 10	55Ω	20 mil
	IDE_IORDY			
	IDE_IOR#			
	IDE_IOW#			
Control	IDE_ACK#	5 : 10	55Ω	20 mil
	IDE_CS1#			
	IDE_CS3#			
	IDE_REQ			
	IDE_IRQ			

Table 49: IDE Interface Trace Properties

Signal Group	Signal Name	Routing Layer	Trace Mismatch	Accumulate Trace Length
Address	IDE_A[2:0]	Top or Bottom	< 5"	< 0.5"
Data	IDE_D[15:0]	Top or Bottom	< 5"	< 0.5"
	IDE_IORDY			
	IDE_IOR#			
	IDE_IOW#			
Control	IDE_ACK#	Top or Bottom	< 5"	< 0.5"
	IDE_CS1#			
	IDE_CS3#			
	IDE_REQ			
	IDE_IRQ			

Table 50: IDE Interface Layout Guidelines

Note:
The IDE trace length in VIA COM Express module is approximately 2.7", therefore the IDE trace length in the carrier board should not be longer than 2.3".

4.12. SATA Interface

The VIA COM Express modules support a SATA interface that complies with SATA Revision 1.0 and SATA Revision 2.0. The VIA COM Express Type 2 module is designed to support up to four SATA ports, and the VIA Type 6 and Type 10 modules can support up to two SATA ports. The SATA interface has a point-to-point topology and it is configurable to support either SATA (3 Gbps) master port or SATA (1.5 Gbps) master/slave port.

4.12.1. SATA Signal Definition

The corresponding SATA interface signals are defined in the connector A-B.

Signal Name	Pin #	I/O	Description	Type
SATA0_TX+	A16	O	Serial ATA transmit output differential pair, channel 0	10, 6 and 2
SATA0_TX-	A17	O		
SATA0_RX+	A19	I	Serial ATA receive input differential pair, channel 0	
SATA0_RX-	A20	I		
SATA1_TX+	B16	O	Serial ATA transmit output differential pair, channel 1	10, 6 and 2
SATA1_TX-	B17	O		
SATA1_RX+	B19	I	Serial ATA receive input differential pair, channel 1	
SATA1_RX-	B20	I		
SATA2_TX+	A22	O	Serial ATA transmit output differential pair, channel 2	2
SATA2_TX-	A23	O		
SATA2_RX+	A25	I	Serial ATA receive input differential pair, channel 2	
SATA2_RX-	A26	I		
SATA3_TX+	B22	O	Serial ATA transmit output differential pair, channel 3	2
SATA3_TX-	B23	O		
SATA3_RX+	B25	I	Serial ATA receive input differential pair, channel 3	
SATA3_RX-	B26	I		
SATA_ACT#	A28	O	SATA activity LED	10, 6 and 2

Table 51: SATA Signal Descriptions

4.12.2. SATA Reference Schematics

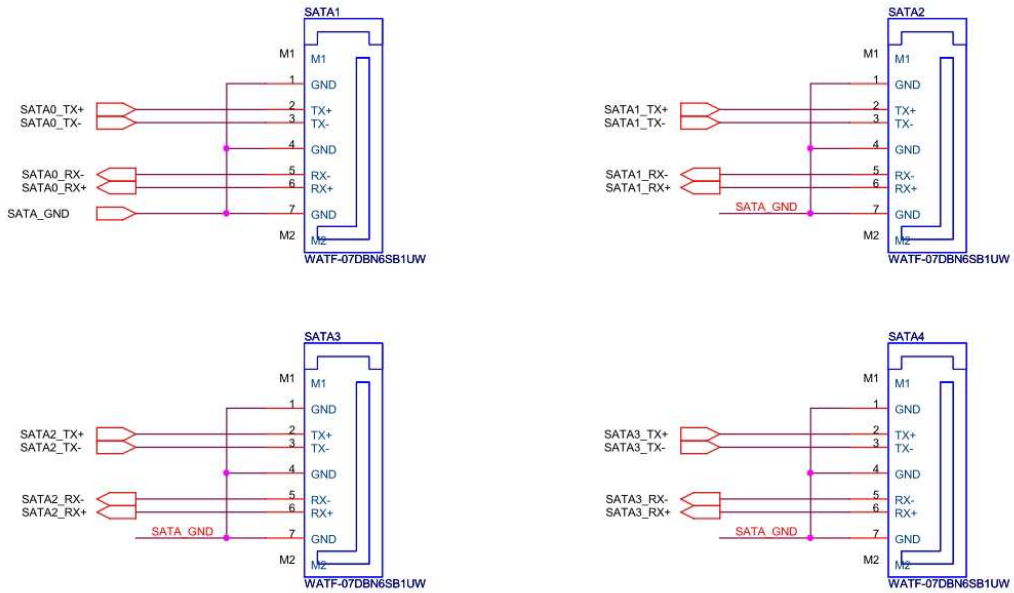


Figure 52: SATA Connectors

4.12.2.1. SATA Layout and Routing Recommendations

- Signal pairs should be referenced to the ground.
- Each pair of SATA traces must be in parallel to each other with the same trace length and not parallel with other signals to minimize crosstalk.
- Receive and transmit group of traces do not need to be matched; nor be serpentine in order to meet the minimum length guidelines.
- Have all related SATA signals routed without interruptions on continuous ground planes. This is recommended because any routing discontinuity or ground plane separation would impact signal transmission.
- For the SATA traces, do not route under magnetic devices or IC's, oscillators, clock synthesizers, crystals that use and/or duplicate clocks.
- Signal trace with single-ended should maintain 55Ω impedance.

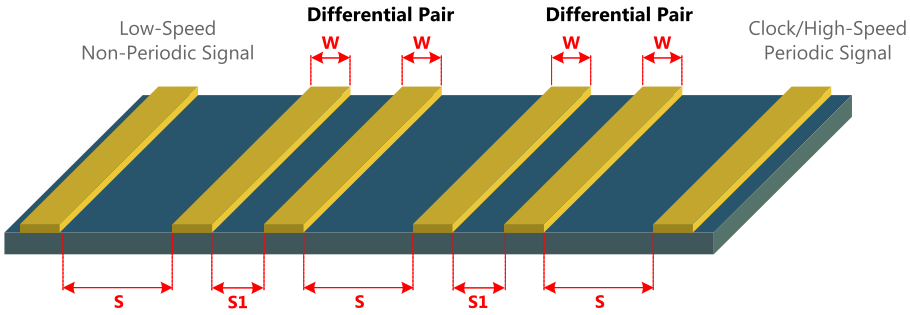


Figure 53: SATA Trace Spacing

Group	Signal Name	Differential Trace Impedance	Differential Pair Trace Mismatch	Differential Trace (S : W : S1 : W : S)
SATA0	SATA0_TX+	85Ω ± 10%	< 5 mil	20 : 5 : 5 : 5 : 20
	SATA0_TX-			
	SATA0_RX+			
	SATA0_RX-			
SATA1	SATA1_TX+	85Ω ± 10%	< 5 mil	20 : 5 : 5 : 5 : 20
	SATA1_TX-			
	SATA1_RX+			
	SATA1_RX-			
SATA2	SATA2_TX+	85Ω ± 10%	< 5 mil	20 : 5 : 5 : 5 : 20
	SATA2_TX-			
	SATA2_RX+			
	SATA2_RX-			
SATA3	SATA3_TX+	85Ω ± 10%	< 5 mil	20 : 5 : 5 : 5 : 20
	SATA3_TX-			
	SATA3_RX+			
	SATA3_RX-			

Table 52: SATA Trace Properties

Group	Signal Name	Routing Layer	Topology	Accumulated Trace Length
SATA0	SATA0_TX+	Top or Bottom	Point-to-Point	< 1.5″
	SATA0_TX-			
	SATA0_RX+			
	SATA0_RX-			
SATA1	SATA1_TX+	Top or Bottom	Point-to-Point	< 1.5″
	SATA1_TX-			
	SATA1_RX+			
	SATA1_RX-			
SATA2	SATA2_TX+	Top or Bottom	Point-to-Point	< 1.5″
	SATA2_TX-			
	SATA2_RX+			
	SATA2_RX-			
SATA3	SATA3_TX+	Top or Bottom	Point-to-Point	< 1.5″
	SATA3_TX-			
	SATA3_RX+			
	SATA3_RX-			

Table 53: SATA Routing, Topology and Layout Guidelines

Notes:

1. The SATA signal trace length in VIA COM Express is approximately 1″, therefore the SATA trace length in the carrier board should not be longer than 1.5″.
2. The placement of coupling capacitors is different between VIA COMe-8X80 / COMe-8X90 and COMe-9X90 COM Express module.
3. The coupling capacitors are already present in VIA COMe-8X80 and COMe-8X90 modules, but not in VIA COMe-9X90 module. The coupling capacitor for COMe-9X90 module should be present in its carrier board.

4.13. USB 2.0 and USB 3.0 Interface

The Universal Serial Bus (USB) provides a bi-directional, isochronous, hot-attachable Plug and Play serial interface for adding external peripheral devices (e.g., game controllers, communication devices, and input devices) on a single bus. The VIA COM Express Type 10, Type 6 and Type 2 modules can support up to eight USB 2.0 interface ports and each USB port has its own over-current detect pin.

However, the VIA COM Express Type 6 module has four new USB interfaces designated only for SuperSpeed USB or commonly knows as USB 3.0 interface. The pin-out of Type 6 uses the previously assigned IDE interface in the pin-out of Type 2 for new USB 3.0 interface. Therefore, a Type 6 module does not support the IDE interface anymore. Type 6 modules can support four USB 3.0 interface and eight USB 2.0 interface signals. Type 10 and Type 2 use all eight USB interface for USB 2.0 signals.

4.13.1. USB 2.0 and USB 3.0 Signal Definition

The corresponding USB 2.0 interface signals are defined in connector A-B, while the USB 3.0 interface signals are implemented in connector C-D.

Signal Name	Pin #	I/O	Description	Type
USB0+	A46	IO	USB 2.0 port 0, data+	10, 6 and 2
USB0-	A45	IO	USB 2.0 port 0, data-	
USB1+	B46	IO	USB 2.0 port 1, data+	
USB1-	B45	IO	USB 2.0 port 1, data-	
USB2+	A43	IO	USB 2.0 port 2, data+	
USB2-	A42	IO	USB 2.0 port 2, data-	
USB3+	B43	IO	USB 2.0 port 3, data+	
USB3-	B42	IO	USB 2.0 port 3, data-	
USB4+	A40	IO	USB 2.0 port 4, data+	
USB4-	A39	IO	USB 2.0 port 4, data-	
USB5+	B40	IO	USB 2.0 port 5, data+	
USB5-	B39	IO	USB 2.0 port 5, data-	
USB6+	A37	IO	USB 2.0 port 6, data+	
USB6-	A36	IO	USB 2.0 port 6, data-	
USB7+	B37	IO	USB 2.0 port 7, data+	
USB7-	B36	IO	USB 2.0 port 7, data-	
USB_0_1_OC#	B44	I	USB over-current sense, USB port 0 and 1	10, 6 and 2
USB_2_3_OC#	A44	I	USB over-current sense, USB port 2 and 3	
USB_4_5_OC#	B38	I	USB over-current sense, USB port 4 and 5	
USB_6_7_OC#	A38	I	USB over-current sense, USB port 6 and 7	

Table 54: USB 2.0 Signal Descriptions

Signal Name	Pin #	I/O	Description	Type
USB_SSTX0+	D4	O	USB 3.0 transmit output differential pair, channel 0	6
USB_SSTX0-	D3			
USB_SSRX0+	C4	I	USB 3.0 receive input differential pair, channel 0	
USB_SSRX0-	C3			
USB_SSTX1+	D7	O	USB 3.0 transmit output differential pair, channel 1	
USB_SSTX1-	D6			
USB_SSRX1+	C7	I	USB 3.0 receive input differential pair, channel 1	
USB_SSRX1-	C6			
USB_SSTX2+	D10	O	USB 3.0 transmit output differential pair, channel 2	
USB_SSTX2-	D9			
USB_SSRX2+	C10	I	USB 3.0 receive input differential pair, channel 2	
USB_SSRX2-	C9			
USB_SSTX3+	D13	O	USB 3.0 transmit output differential pair, channel 3	
USB_SSTX3-	D12			
USB_SSRX3+	C13	I	USB 3.0 receive input differential pair, channel 3	
USB_SSRX3-	C12			

Table 55: USB 3.0 Signal Descriptions

4.13.2. USB 2.0 and USB 3.0 Reference Schematics

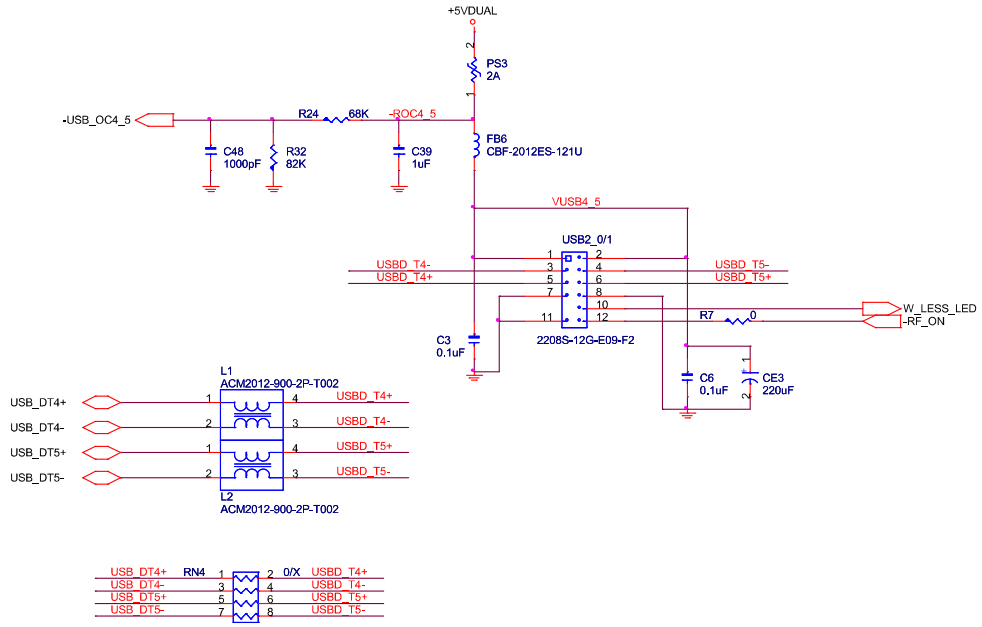
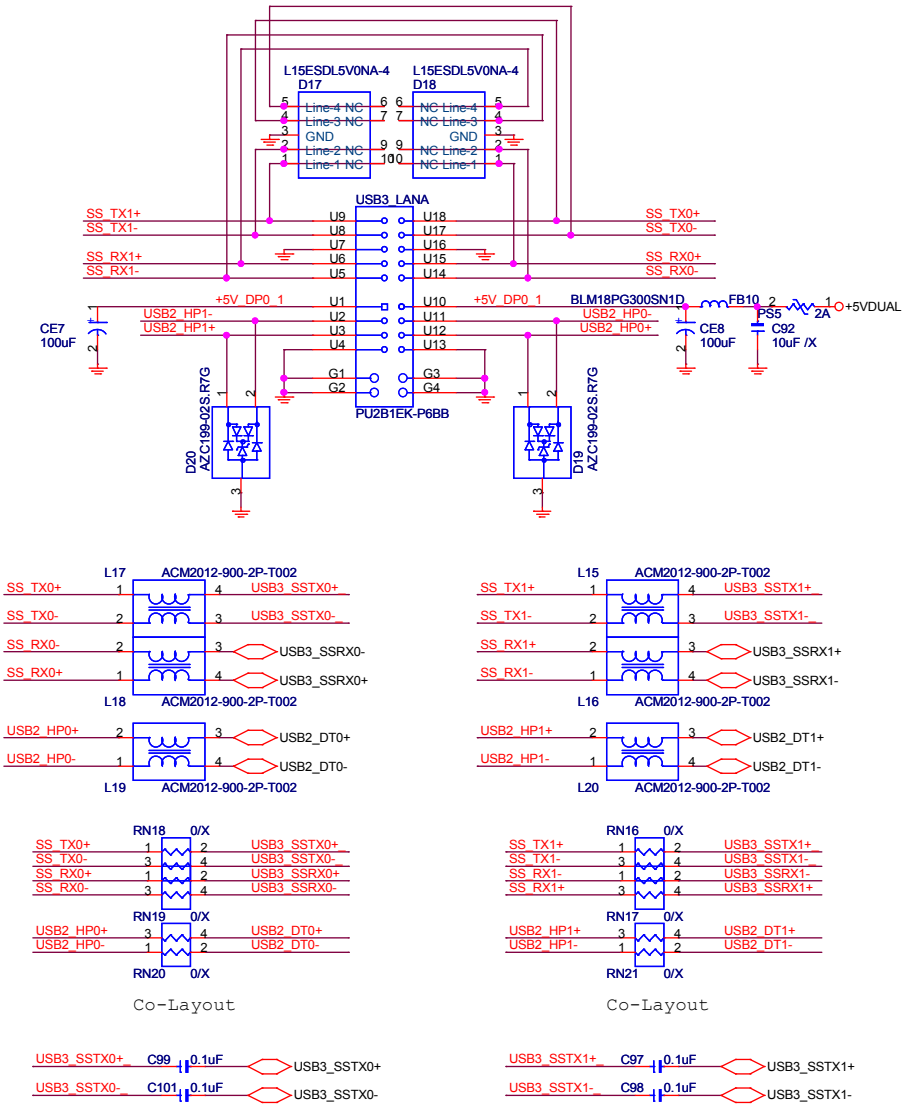


Figure 54: USB 2.0 (port 0 and port 1) Interface



Note: Please place those parts close to USB Connector

Figure 55: USB 3.0 (port 0 and port 1) Interface

4.13.2.1. USB Layout and Routing Recommendations

The layout guidelines for the USB data lines are listed below. And a routing example for two pairs of USB data buses is shown in Figure 58.

- The differential pair signals should be all referenced to ground.
- Differential pair route in parallel and in equal length.
- The amount of vias and corners used for the USB 2.0 and USB 3.0 signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Each pair of USB data lines is required to be parallel to each other with the same trace length (see Figure 58), and not parallel with other signals to minimize crosstalk.
- Separate the signal traces into similar groups and route similar signal traces together. In addition, it is recommended to have differential pairs routed together on the motherboard.
- Control trace signals (USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_0_6_7_OC#) impedance should maintain 55Ω ± 10%.
- For the USB traces, do not route them under oscillators, crystals, clock synthesizers, magnetic devices or IC's which could be using duplicate clocks.

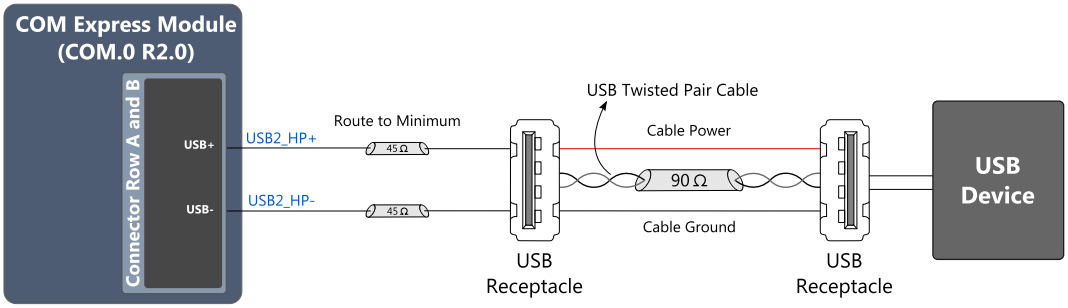


Figure 56: USB 2.0 Differential Signal Layout Recommendations

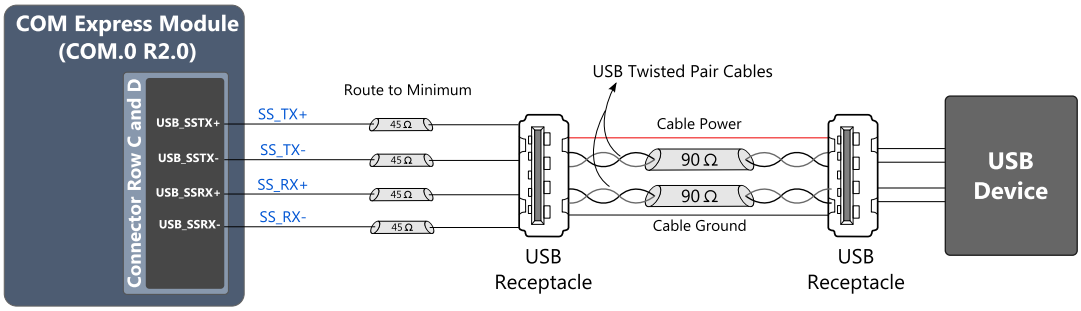


Figure 57: USB 3.0 Differential Signal Layout Recommendations

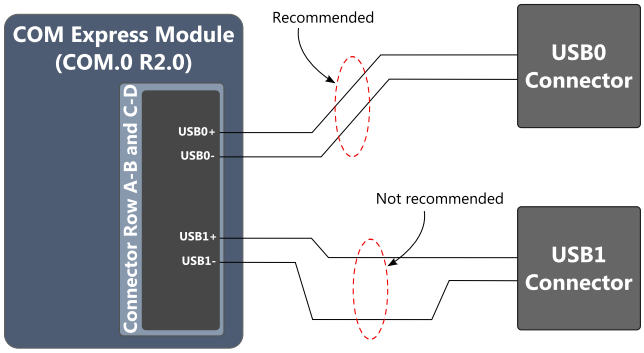


Figure 58: USB Differential Signal Routing Example

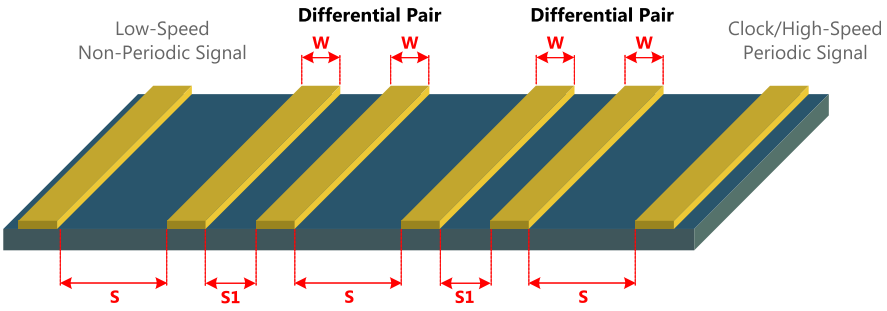


Figure 59: USB 2.0 and 3.0 Trace Spacing

Signal Grouping		Signal Name	Termination Option	Signal Type	Topology
Differential Data Pair	Port 0	USB0+, USB0-	None	Differential Data I/O Pairs	Point to Point
	Port 1	USB1+, USB1-			
	Port 2	USB2+, USB2-			
	Port 3	USB3+, USB3-			
	Port 4	USB4+, USB4-			
	Port 5	USB5+, USB5-			
	Port 6	USB6+, USB6-			
	Port 7	USB7+, USB7-			
Control	USB_0_1_OC#		None	Input Signals	Point to Point
	USB_2_3_OC#				
	USB_4_5_OC#				
	USB_6_7_OC#				

Table 56: USB 2.0 Interface Routing Topology and Signal Type

Signal Grouping		Signal Name	Routing Layer	Term Stub Length	Trace Mismatch	Accumulated Trace Length
Differential Data Pair	Port 0	USB0+, USB0-	Top or Bottom	< 1″	< 0.005″	Route to minimum (or < 9″)
	Port 1	USB1+, USB1-				
	Port 2	USB2+, USB2-				
	Port 3	USB3+, USB3-				
	Port 4	USB4+, USB4-				
	Port 5	USB5+, USB5-				
	Port 6	USB6+, USB6-				
	Port 7	USB7+, USB7-				
Control	USB_0_1_OC#		Top or Bottom	< 1″	-	Route to Minimum
	USB_2_3_OC#					
	USB_4_5_OC#					
	USB_6_7_OC#					

Table 57: USB 2.0 Interface Layout Guidelines

Signal Name	Signal Type	Trace Impedance	Trace (Width : Spacing) S : W : S1 : W : S	Spacing to Other Group
USB0+, USB0-	Differential	90Ω ± 15%	20 : 6 : 7 : 6 : 20	< 0.03″
USB1+, USB1-				
USB2+, USB2-				
USB3+, USB3-				
USB4+, USB4-				
USB5+, USB5-				
USB6+, USB6-				
USB7+, USB7-				
USB_0_1_OC#	Single-ended	55Ω ± 10%	5 : 10	< 0.02″
USB_2_3_OC#				
USB_4_5_OC#				
USB_6_7_OC#				

Table 58: USB 2.0 Trace Properties

Signal Grouping		Signal Name	Termination Option	Signal Type	Topology
Differential Data Pair	Port 0	USB3_SSTX0+, USB3_SSTX0-	None	Differential Data I/O Pairs	Point to Point
		USB3_SSRX0+, USB3_SSRX0-			
	Port 1	USB3_SSTX1+, USB3_SSTX1-			
		USB3_SSRX1+, USB3_SSRX1-			
	Port 2	USB3_SSTX2+, USB3_SSTX2-			
		USB3_SSRX2+, USB3_SSRX2-			
	Port 3	USB3_SSTX3+, USB3_SSTX3-			
		USB3_SSRX3+, USB3_SSRX3-			
Control		USB_0_1_OC#	None	Input Signals	Point to Point
		USB_2_3_OC#			

Table 59: USB 3.0 Interface Routing Topology and Signal Type

Signal Grouping		Signal Name	Routing Layer	Term Stub Length	Trace Mismatch	Accumulated Trace Length
Differential Data Pair	Port 0	USB3_SSTX0+, USB3_SSTX0-	Top or Bottom	< 1″	< 0.005″	Route to Minimum (or < 3″)
		USB3_SSRX0+, USB3_SSRX0-				
	Port 1	USB3_SSTX1+, USB3_SSTX1-				
		USB3_SSRX1+, USB3_SSRX1-				
	Port 2	USB3_SSTX2+, USB3_SSTX2-				
		USB3_SSRX2+, USB3_SSRX2-				
	Port 3	USB3_SSTX3+, USB3_SSTX3-				
		USB3_SSRX3+, USB3_SSRX3-				
Control		USB_0_1_OC#	Top or Bottom	< 1″	-	Route to minimum
		USB_2_3_OC#				

Table 60: USB 3.0 Interface Layout Guidelines

Signal Name	Signal Type	Trace Impedance	Trace (Width : Spacing) S : W : S1 : W : S	Spacing to Other Group
USB3_SSTX0+, USB3_SSTX0-	Differential	85Ω ± 15%	20 : 5 : 5 : 5 : 20	< 0.03″
USB3_SSRX0+, USB3_SSRX0-				
USB3_SSTX1+, USB3_SSTX1-				
USB3_SSRX1+, USB3_SSRX1-				
USB3_SSTX2+, USB3_SSTX2-				
USB3_SSRX2+, USB3_SSRX2-				
USB3_SSTX3+, USB3_SSTX3-				
USB3_SSRX3+, USB3_SSRX3-				
USB_0_1_OC#	Single-ended	55Ω ± 10%	5 : 10	< 0.02″
USB_2_3_OC#				

Table 61: USB 3.0 Trace Properties

Note:
The USB 2.0 and USB 3.0 trace length in VIA COM Express module is approximately 2.5″, therefore the USB 2.0 and USB 3.0 trace length in the carrier board should not longer than 9″ and 3″ respectively.

4.14. Audio Interface

The Audio Interface is a link between the VIA COM Express modules and Audio Codec that supports the AC'97 and High Definition Audio in the carrier board design. This section contains AC'97 and High Definition Audio layout and routing information. Although codec for AC'97 and High Definition Audio use the same signal interface, these two are different and cannot be used at the same time on the board.

4.14.1. Audio Signal Definition

The corresponding audio interface pin-out signals are defined in connector A-B.

Signal Name	Pin #	I/O	Description	Type
AC/HDA_RST#	A30	O	Codec reset	10, 6 and 2
AC/HDA_SYNC	A29	O	Serial Sample Rate Synchronization	
AC/HDA_BITCLK	A32	O	Bit clock for Codec	
AC/HDA_SDOUT	A33	O	Serial Data Output	
AC/HDA_SDIN0	B30	I	Serial Data Input Stream from Codec 1	
AC/HDA_SDIN1	B29	I	Serial Data Input Stream from Codec 2	
AC/HDA_SDIN3	B28	I	Serial Data Input Stream from Codec 3	

Table 62: Audio Interface Signal Descriptions

4.14.2. Audio Reference Schematics

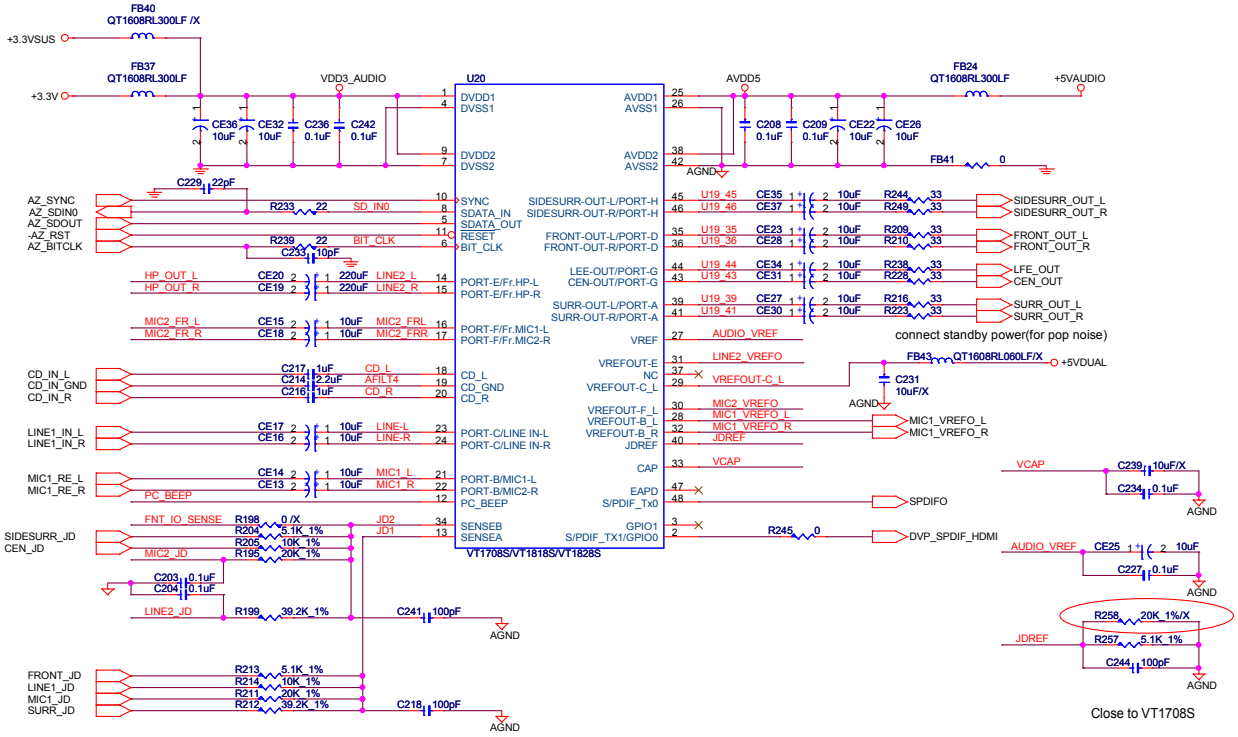


Figure 60: HD Audio Codec Implementation Example

4.14.2.1. Audio Layout and Routing Recommendations

- Route the analog and digital trace signals as far as possible from each other to prevent noise.
- Route the clock trace away from any analog input and voltage reference pins.
- Isolate the codec or put away from any major current path or ground bounce.
- Fill with copper the regions between the analog traces and attached it to the analog ground.
- Fill with copper the regions between the digital traces and attached it to the digital ground.
- Use the metal film resistors for all resistors in the signal path.
- Grouped analog parts in one area and all digital parts in another area.
- Route traces as short as possible.

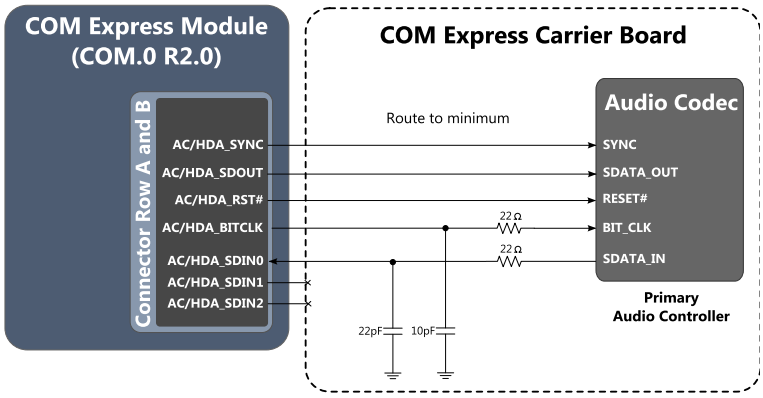


Figure 61: Single On-Board High Definition Audio Codec Implementation Example

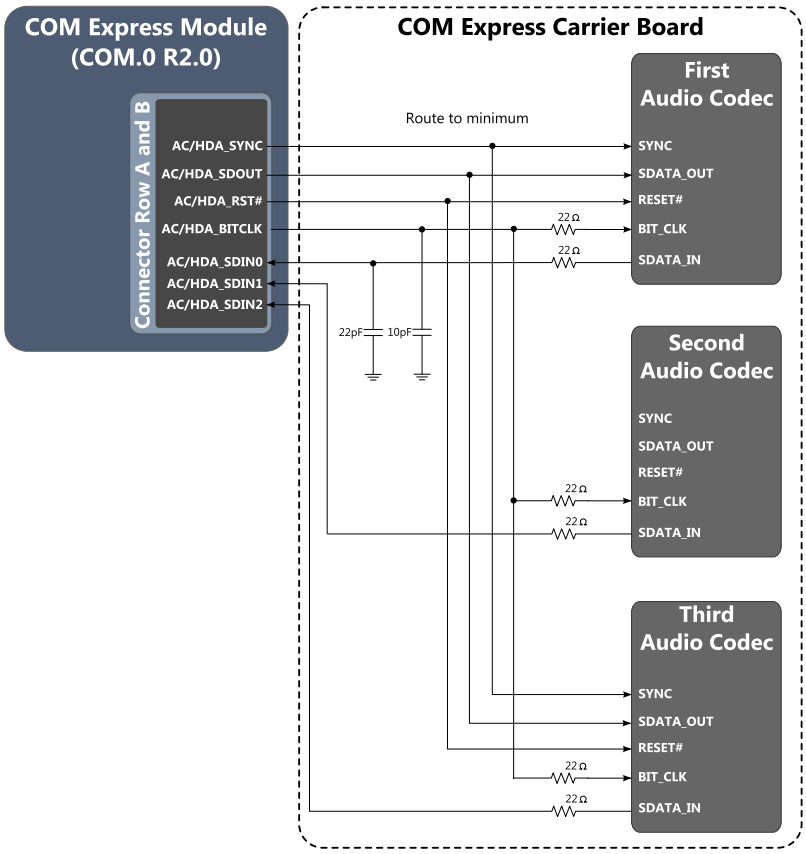


Figure 62: Fully On-Board High Definition Audio Codec Implementation Example

Signal Name	Trace (Width : Spacing)	Trace Impedance	Spacing to Other Group
AC/HDA_RST#	5 : 10	55Ω ± 10%	-
AC/HDA_SYNC			
AC/HDA_SDOUT			
AC/HDA_SDIN0	5 : 10	55Ω ± 10%	-
AC/HDA_SDIN1			
AC/HDA_SDIN2			
AC/HDA_BITCLK	5 : 20	55Ω ± 10%	-

Table 63: Trace Properties for Audio Interface

Signal Name	Routing Layer	Topology	Accumulated Trace Length
AC/HDA_RST#	Top Layer	Point to Point	< 17″
AC/HDA_SYNC			
AC/HDA_SDOUT			
AC/HDA_SDIN0	Top Layer	Point to Point	< 17″
AC/HDA_SDIN1			
AC/HDA_SDIN2			
AC/HDA_BITCLK	Top Layer	Point to Point	< 17″

Table 64: Topology and Layout Guidelines for Audio Interface

Notes:

1. The audio trace length in VIA COM Express module is approximately 3″, therefore the audio trace length in the carrier board should not be longer than 14″.
2. The values of the series resistors depend on the design, and should be verified for optimized timing and signal quality.

4.15. System Management Bus (SMBus) Interface

The System Management Bus (SMBus) is a two-wire interface, which uses I²C bus to make a communication between the COM Express module and the rest of the system.

4.15.1. System Management Bus Signal Definition

The corresponding SMBus interface pin-out signals are defined in connector row B.

Signal Name	Pin #	I/O	Description	Type
SMB_CLK	B13	IO	SMBus bi-directional clock line	10, 6 and 2
SMB_DAT	B14	IO	SMBus bi-directional data line	
SMB_ALERT#	B15	I	SMBus Alert	

Table 65: SMBus Interface Signal Descriptions

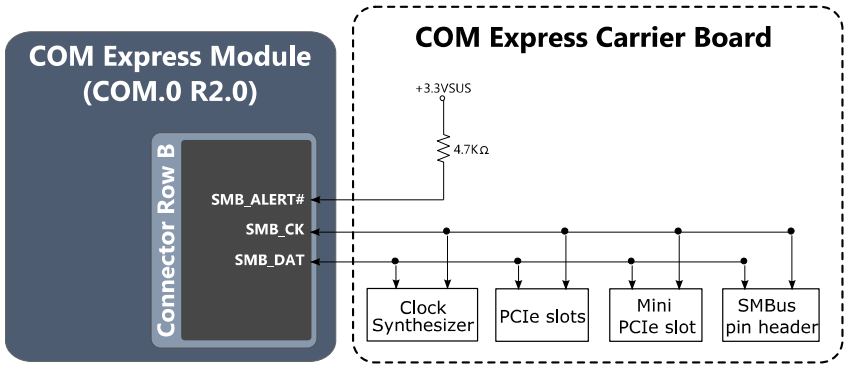


Figure 63: SMBus Interface Example

4.15.1.1. SMBus Layout and Routing Recommendations

Signal Name	Trace (Width : Spacing)	Trace Impedance	Note
SMB_CK	5 : 10	55Ω ± 10%	Route to minimum whenever possible
SMB_DAT	5 : 10	55Ω ± 10%	
SMB_ALERT#	5 : 10	55Ω ± 10%	

Table 66: Trace Properties for SMBus Interface

Signal Name	Routing Layer	Topology	Accumulated Trace Length
SMB_CK	Top Layer	Point to Point	-
SMB_DAT	Top Layer	Point to Point	-
SMB_ALERT#	Top Layer	Point to Point	-

Table 67: Topology and Layout Guidelines for SMBus Interface

4.16. LAN Interface

The LAN interface supports a 10/100Mbps and 1000Mbps (Gigabit Ethernet), and complies with the IEEE standard for 10BASE-T, 100BASE-T, 1000BASE-T, TX and T4 Ethernet interfaces. It consists of four differential signals and control signals for activity link indicators. These signals can be used to connect to the RJ-45 connector with integrated or external isolation magnetic (transformer) on the carrier board.

4.16.1. LAN Signal Definition

The corresponding LANs interface pin-out signals are defined in connector A-B.

Signal Name	Pin #	I/O	Description	Type
GBE0_MDI0+	A13	IO	Media Dependent Interface differential pair 0	10, 6 and 2
GBE0_MDI0-	A12			
GBE0_MDI1+	A10	IO	Media Dependent Interface differential pair 1	
GBE0_MDI1-	A9			
GBE0_MDI2+	A7	IO	Media Dependent Interface differential pair 2	
GBE0_MDI2-	A6			
GBE0_MDI3+	A3	IO	Media Dependent Interface differential pair 3	
GBE0_MDI3-	A2			
GBE0_CTREF	A14		Reference voltage for carrier board Ethernet channel 0 magnetic center tap	
GBE0_LINK100#	A4	O	Ethernet controller 0 100Mbps link indicator	
GBE0_LINK1000#	A5	O	Ethernet controller 0 1000Mbps link indicator	
GBE0__ACT#	B2	O	Ethernet controller 0 activity indicator	

Table 68: LAN Signal Descriptions

4.16.2. LAN Reference Schematics

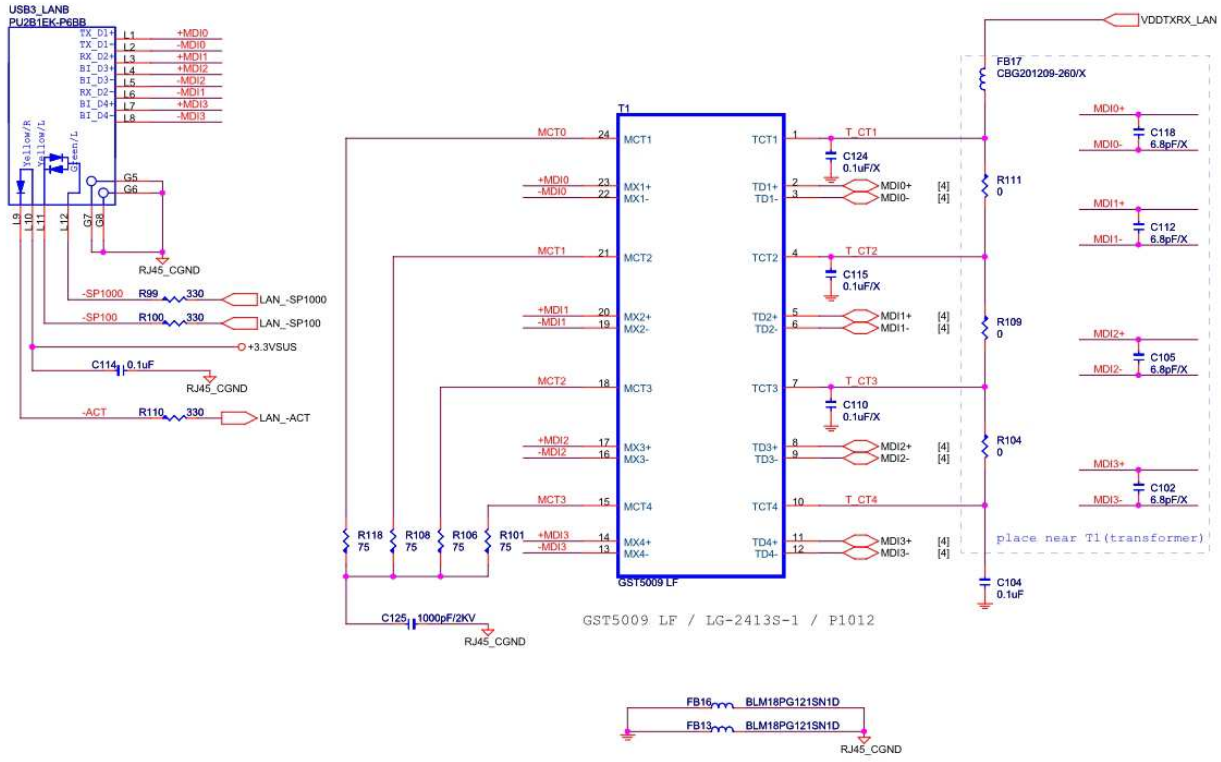


Figure 64: LAN Implementation Example

4.16.2.1. LAN Layout and Routing Recommendations

This section shows the layout recommendations of both transmit and receive differential data pairs and single-ended control signal between the COM Express module and the transformer (magnetic module), between the transformer and RJ-45 connector, and between the COM Express module and RJ-45 connector with integrated magnetic module.

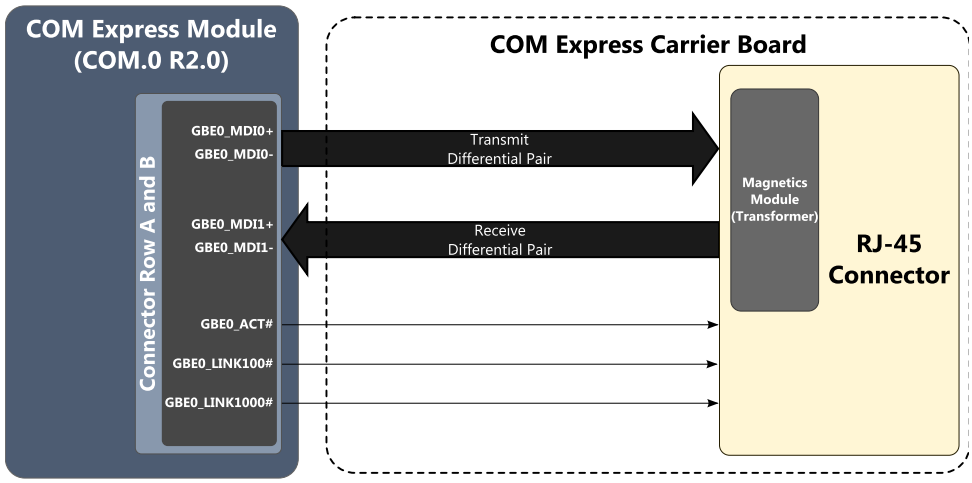


Figure 65: 10/100 Ethernet Layout Recommendation (integrated magnetic module)

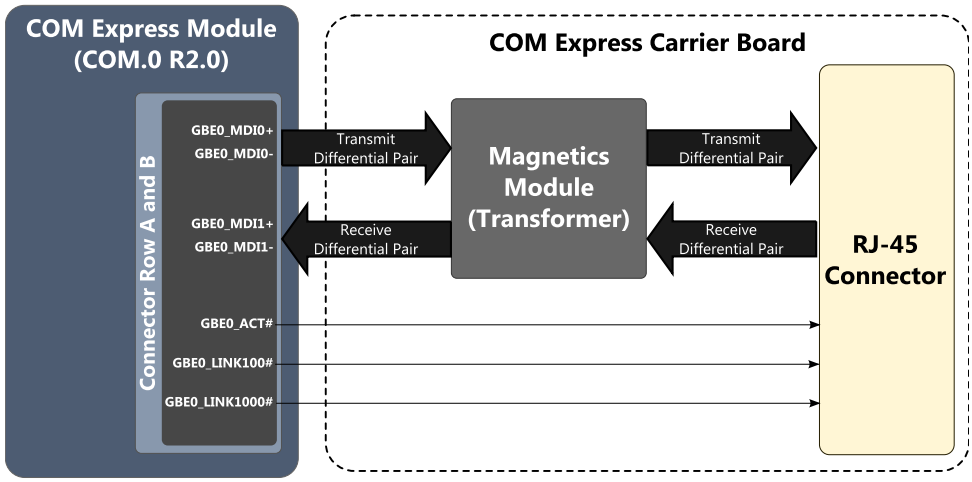


Figure 66: 10/100 Ethernet Layout Recommendation (external magnetic module)

Notes:

1. It is recommended to use termination circuits for the unused pin at the RJ-45 connector and for wire-side center-taps of the magnetic module. Improper usage (or lack of usage) of the termination circuits for those unused pins at the RJ-45 connector wire-side center taps of the transformer will cause emissions and long cable noise problems related to other IEEE conformance issues.
2. The LAN magnetic should be placed on the carrier board.

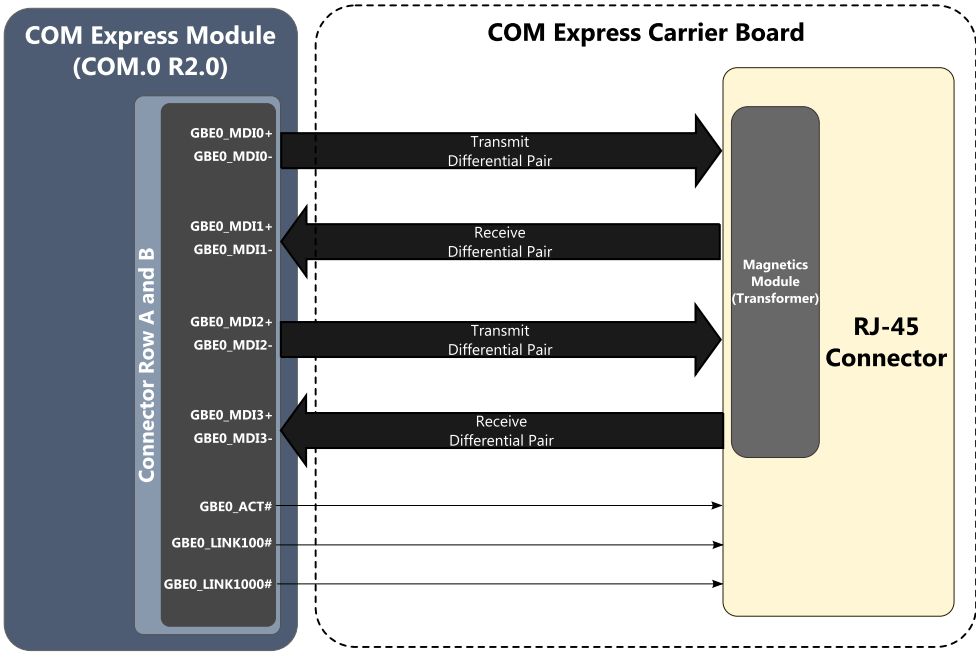


Figure 67: Gigabit Ethernet Layout Recommendations (integrated magnetic module)

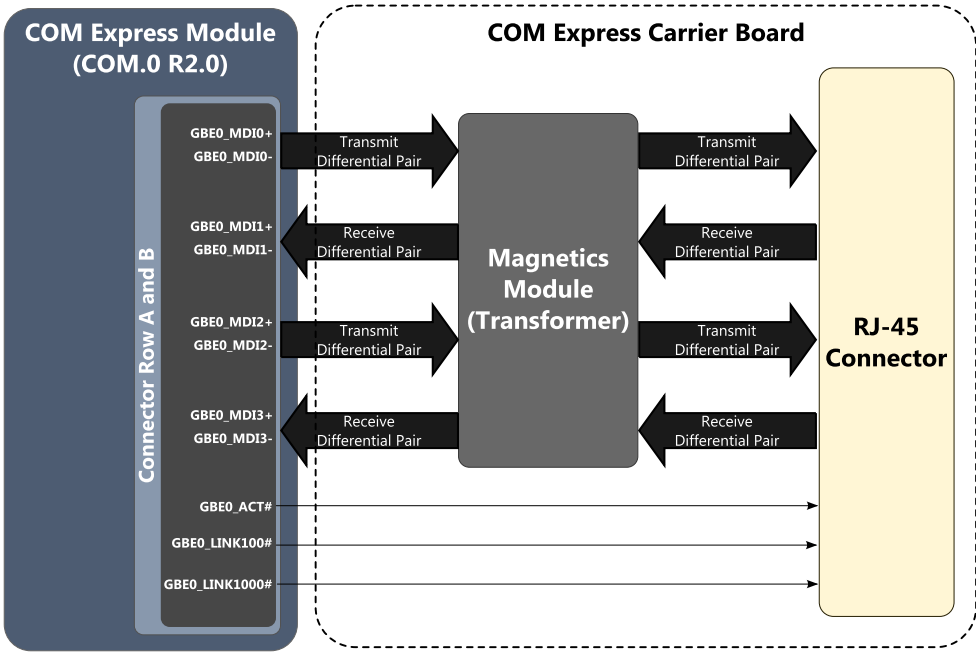


Figure 68: Gigabit Ethernet Layout Recommendations (external magnetic module)

Note:

If the Gigabit Ethernet implementation is not being use, the pins GBE_MDI02+, GBE_MDI02-, GBE_MDI03+ and GBE_MDI03- should not be connected.

4.16.3. LAN Layout and Routing Recommendations

- Route differential pairs close together and away from other signals.
- Route any other trace parallel to one of the differential trace.
- Keep trace length within each differential pair equal.
- Keep proper impedance between two traces within a differential pair.
- Each differential pair of signals is required to be paralleled to each other with the same trace length (Tolerance ±50 mil) on the component (top) layer and to be paralleled to a respective ground plane. The length difference between the shortest and longest pairs should be less than 200 mil.
- The accumulated trace length of differential signals pair between the VIA COM Express module pin-out connector and magnetic module should be less than 7".
- The accumulated trace length of differential signals pair between the external magnetic module and RJ-45 connector should be less than 1". Isolate ground plane and connect to chassis earth.
- Keep each differential pair on the same plane.
- To prevent any noise from injecting into the differential pairs, be sure to keep digital signals or other signals away from the differential signals.
- The external magnetic module should be placed close to the RJ-45 connector to limit EMI emissions.

Signal Grouping	Signal Name	Trace Impedance	Trace (Width : Spacing)	Note
Differential Pair	GBE0_MDI0+	100Ω ± 15% differential	20 : 5 : 8 : 5 : 20	Route traces as short as possible
	GBE0_MDI0-			
	GBE0_MDI1+	100Ω ± 15% differential	20 : 5 : 8 : 5 : 20	
	GBE0_MDI1-			
	GBE0_MDI2+	100Ω ± 15% differential	20 : 5 : 8 : 5 : 20	
	GBE0_MDI2-			
	GBE0_MDI3+	100Ω ± 15% differential	20 : 5 : 8 : 5 : 20	
	GBE0_MDI3-			
Single-ended	GBE0_LINK100#	55Ω ± 10%	5 : 10	
	GBE0_LINK1000#	55Ω ± 10%	5 : 10	
	GBE0_ACT#	55Ω ± 10%	5 : 10	

Table 69: Trace Properties for LAN Interface

Signal Grouping	Signal Name	Routing Layer	Topology	Accumulated Trace Length
Differential Pair	GBE0_MDI0+	Top Layer	Point to Point	< 8"
	GBE0_MDI0-			
	GBE0_MDI1+			
	GBE0_MDI1-			
	GBE0_MDI2+			
	GBE0_MDI2-			
	GBE0_MDI3+			
	GBE0_MDI3-			
Single-ended	GBE0_LINK100#	Top Layer	Point to Point	< 8"
	GBE0_LINK1000#			
	GBE0_ACT#			

Table 70: Topology and Layout Routing Guidelines for LAN Interface

Appendix A. Video Combinations and Display Device Support

The video combinations and the supported display devices listed below are only for COM.0 R1.0. These combinations are supported when using a VIA COM Express Type 2 module such as COMe-8X80.

Display Device Configurations

Request Priority	DACs Connection	Integrated LVDS Connection	DVP1 Connection
Configuration 1	CRT	1-Ch LVDS or 2-Ch LVDS	DVI (VT1632A)
Configuration 2	CRT	NC	DVI (VT1632A)
Configuration 3	CRT	1-Ch LVDS or 2-Ch LVDS	HDMI (AD9389/AD9889)
Configuration 4	CRT	NC	HDMI (AD9389/AD9889)
Configuration 5	CRT	1-Ch LVDS or 2-Ch LVDS	TV (VT1625)
Configuration 6	CRT	NC	TV (VT1625)
Configuration 7	CRT	NC	18 bits TTL Panel

Note:
HDMI® cannot support interlace mode.

Two Panel Configurations

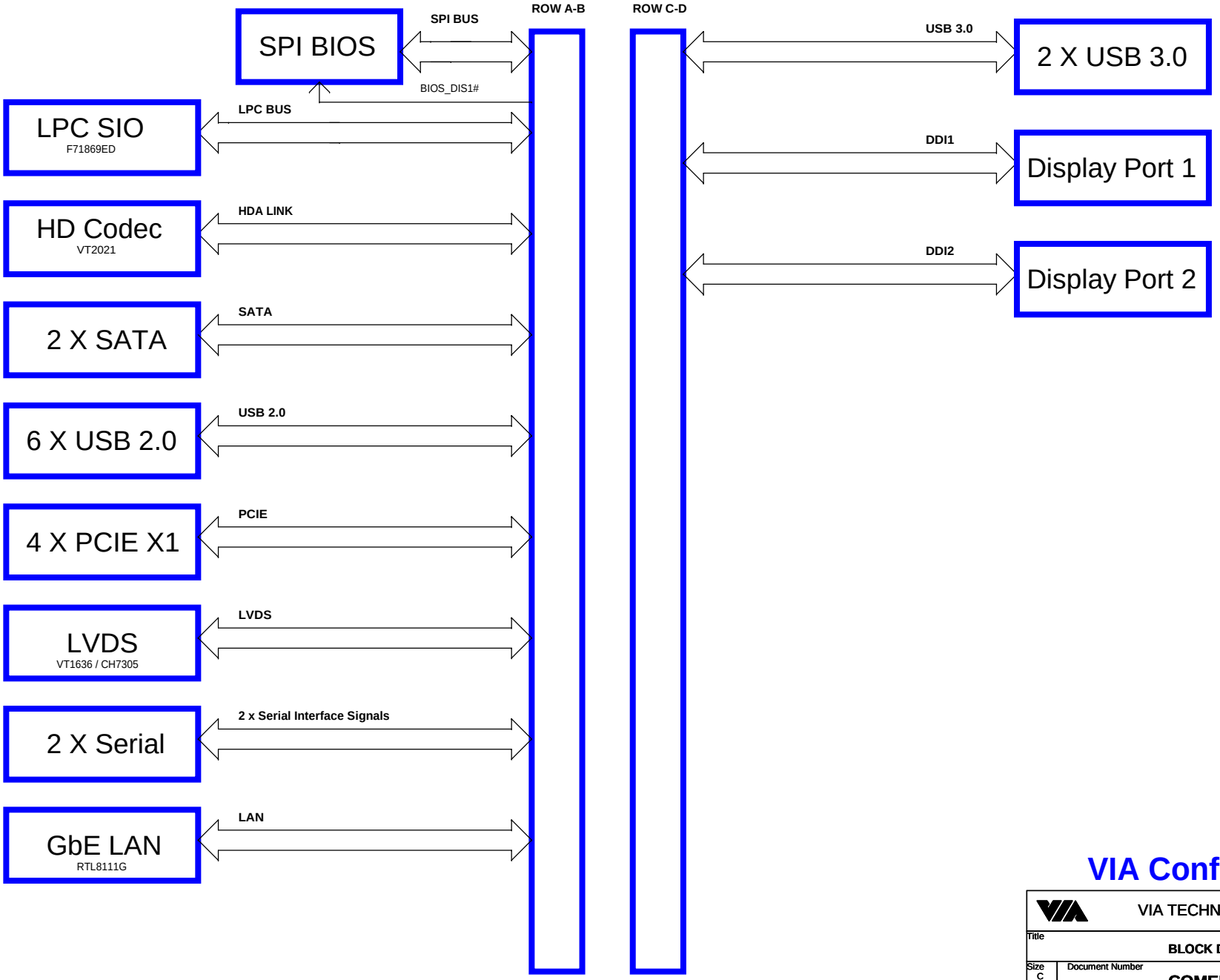
Request Priority	DACs Connection	Integrated LVDS Connection	DVP1 Connection
Configuration 8	CRT	1-Ch LVDS or 2-Ch LVDS	NC
Configuration 9	CRT	2-Ch LVDS	LVDS (VT1636)

Notes:
1. The two panels must share the same timing specification and resolution.
2. Only supports scaling on the primary LCD panel.

Appendix B. COMEDB4, COMEDB2 and COMEDB1 Reference Schematics

The VIA COMEDB4, COMEDB2 and COMEDB1 are the carrier board reference schematics design using the VIA COMe-9X90, COMe-8X90 and COMe-8X80 COM Express modules.

COMEBD4 Block Diagram



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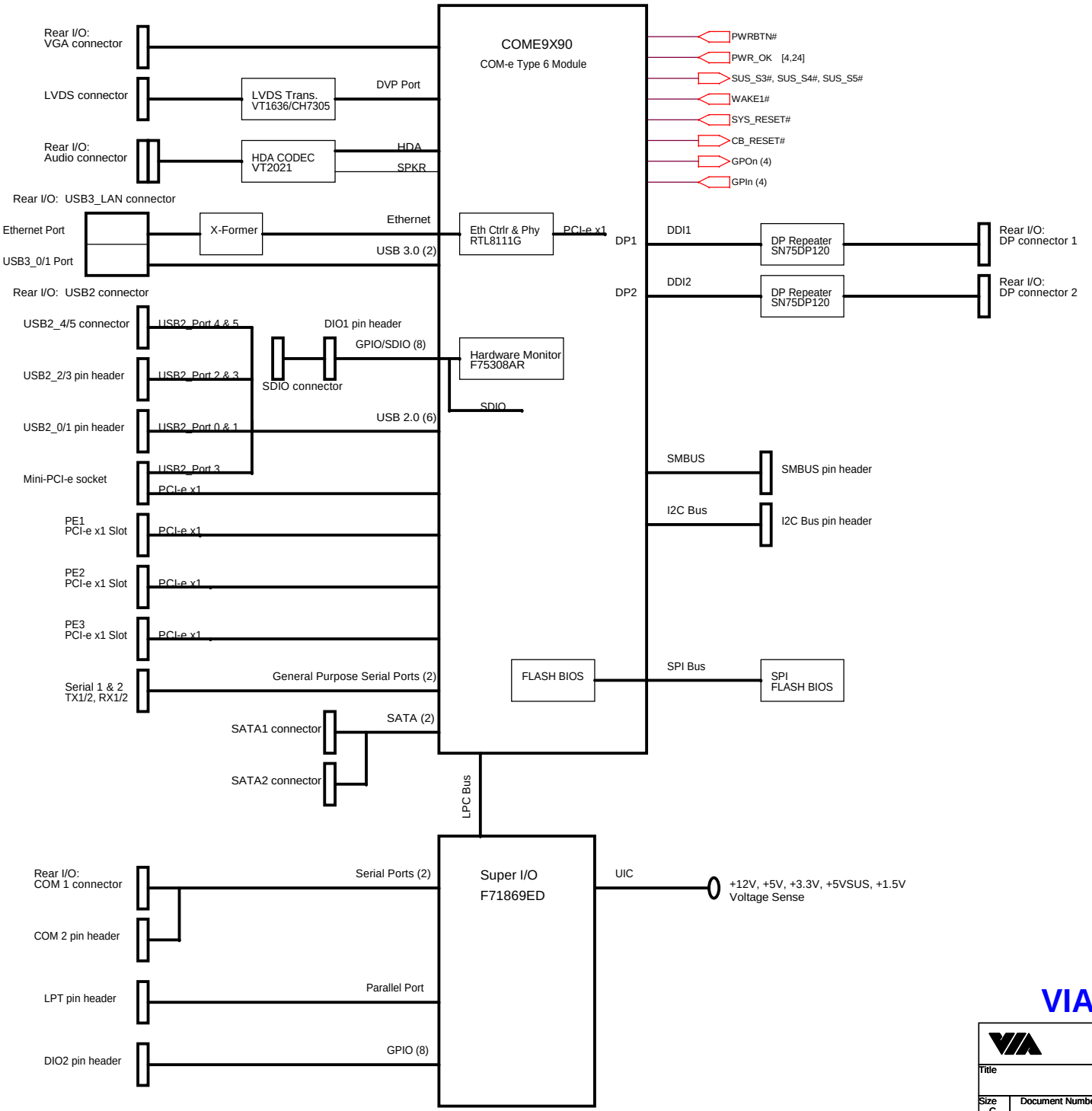

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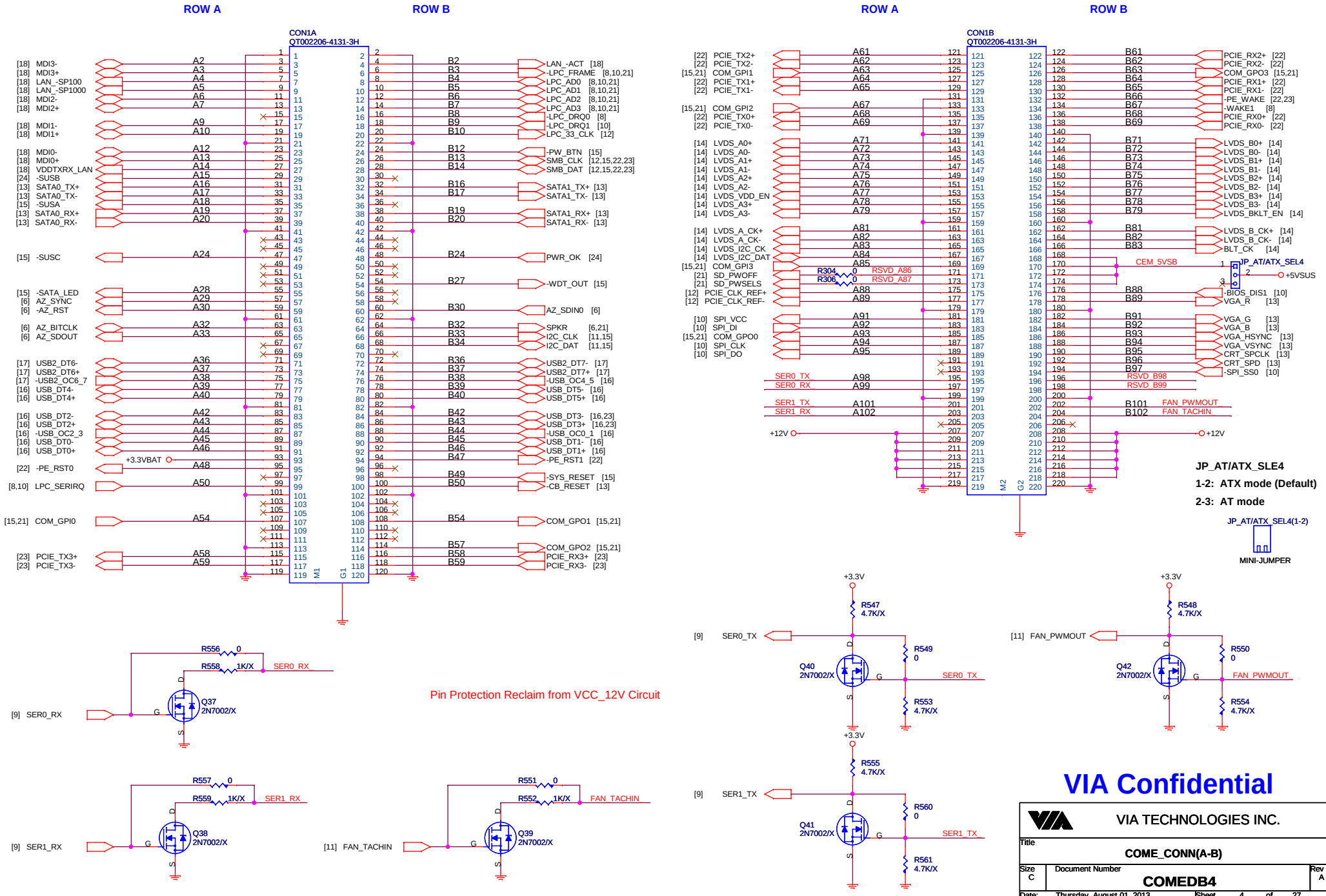
ROW A
ROW B
CON1A
QT002206-4131-3H
[18] MDI3-
[18] MDI3+
[18] LAN_-SP100
[18] LAN_-SP1000
[18] MDI2-
[18] MDI2+
[18] MDI1-
[18] MDI1+
[18] MDI0-
[18] MDI0+
[18] VDDTXRX_LAN
[24] -SUSB
[13] SATA0_TX+
[13] SATA0_TX-
[15] -SUSA
[13] SATA0_RX+
[13] SATA0_RX-
[15] -SUSC
[15] -SATA_LED
[6] AZ_SYNC
[6] -AZ_RST
[6] AZ_BITCLK
[6] AZ_SDOUT
[17] USB2_DT6-
[17] USB2_DT6+
[17] -USB2_OC6_7
[16] USB_DT4-
[16] USB_DT4+
[16] USB_DT2-
[16] USB_DT2+
[16] -USB_OC2_3
[16] USB_DT0-
[16] USB_DT0+
+3.3VBAT
[22] -PE_RST0
[8,10] LPC_SERIRQ
[15,21] COM_GPI0
[23] PCIE_TX3+
[23] PCIE_TX3-
LAN_-ACT [18]
-LPC_FRAME [8,10,21]
LPC_AD0 [8,10,21]
LPC_AD1 [8,10,21]
LPC_AD2 [8,10,21]
LPC_AD3 [8,10,21]
-LPC_DRQ0 [8]
-LPC_DRQ1 [10]
LPC_33_CLK [12]
-PW_BTN [15]
SMB_CLK [12,15,22,23]
SMB_DAT [12,15,22,23]
SATA1_TX+ [13]
SATA1_TX- [13]
SATA1_RX+ [13]
SATA1_RX- [13]
PWR_OK [24]
-WDT_OUT [15]
AZ_SDIN0 [6]
SPKR [6,21]
I2C_CLK [11,15]
I2C_DAT [11,15]
USB2_DT7- [17]
USB2_DT7+ [17]
-USB_OC4_5 [16]
USB_DT5- [16]
USB_DT5+ [16]
USB_DT3- [16,23]
USB_DT3+ [16,23]
-USB_OC0_1 [16]
USB_DT1- [16]
USB_DT1+ [16]
-PE_RST1 [22]
-SYS_RESET [15]
-CB_RESET [13]
COM_GPO1 [15,21]
COM_GPO2 [15,21]
PCIE_RX3+ [23]
PCIE_RX3- [23]
M1
G1
R556 0
R558 1K/X
SER0_RX
Q37
2N7002/X
[9] SER0_RX
R557 0
R559 1K/X
SER1_RX
Q38
2N7002/X
[9] SER1_RX
Pin Protection Reclaim from VCC_12V Circuit
R551 0
R552 1K/X
FAN_TACHIN
Q39
2N7002/X
[11] FAN_TACHIN
ROW A
ROW B
CON1B
QT002206-4131-3H
[22] PCIE_TX2+
[22] PCIE_TX2-
[15,21] COM_GPI1
[22] PCIE_TX1+
[22] PCIE_TX1-
[15,21] COM_GPI2
[22] PCIE_TX0+
[22] PCIE_TX0-
[14] LVDS_A0+
[14] LVDS_A0-
[14] LVDS_A1+
[14] LVDS_A1-
[14] LVDS_A2+
[14] LVDS_A2-
[14] LVDS_VDD_EN
[14] LVDS_A3+
[14] LVDS_A3-
[14] LVDS_A_CK+
[14] LVDS_A_CK-
[14] LVDS_I2C_CK
[14] LVDS_I2C_DAT
[15,21] COM_GPI3
[21] SD_PWOFF
[21] SD_PWSELS
[12] PCIE_CLK_REF+
[12] PCIE_CLK_REF-
[10] SPI_VCC
[10] SPI_DI
[15,21] COM_GPO0
[10] SPI_CLK
[10] SPI_DO
SER0_TX
SER0_RX
SER1_TX
SER1_RX
+12V
R304 0 RSVD_A86
R306 0 RSVD_A87
PCIE_RX2+ [22]
PCIE_RX2- [22]
COM_GPO3 [15,21]
PCIE_RX1+ [22]
PCIE_RX1- [22]
-PE_WAKE [22,23]
-WAKE1 [8]
PCIE_RX0+ [22]
PCIE_RX0- [22]
LVDS_B0+ [14]
LVDS_B0- [14]
LVDS_B1+ [14]
LVDS_B1- [14]
LVDS_B2+ [14]
LVDS_B2- [14]
LVDS_B3+ [14]
LVDS_B3- [14]
LVDS_BKLT_EN [14]
LVDS_B_CK+ [14]
LVDS_B_CK- [14]
BLT_CK [14]
CEM_5VSB
JP_AT/ATX_SEL4
+5VSUS
-BIOS_DIS1 [10]
VGA_R [13]
VGA_G [13]
VGA_B [13]
VGA_HSYNC [13]
VGA_VSYNC [13]
CRT_SPCLK [13]
CRT_SPD [13]
-SPI_SS0 [10]
RSVD_B98
RSVD_B99
FAN_PWMOUT
FAN_TACHIN
M2
G2
JP_AT/ATX_SLE4
1-2: ATX mode (Default)
2-3: AT mode
JP_AT/ATX_SEL4(1-2)
MINI-JUMPER
+3.3V
R547 4.7K/X
[9] SER0_TX
Q40
2N7002/X
R549 0
SER0_TX
R553 4.7K/X
R555 4.7K/X
[9] SER1_TX
Q41
2N7002/X
R560 0
SER1_TX
R561 4.7K/X
R548 4.7K/X
[11] FAN_PWMOUT
Q42
2N7002/X
R550 0
FAN_PWMOUT
R554 4.7K/X
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VIA TECHNOLOGIES INC.
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COME_CONN(A-B)
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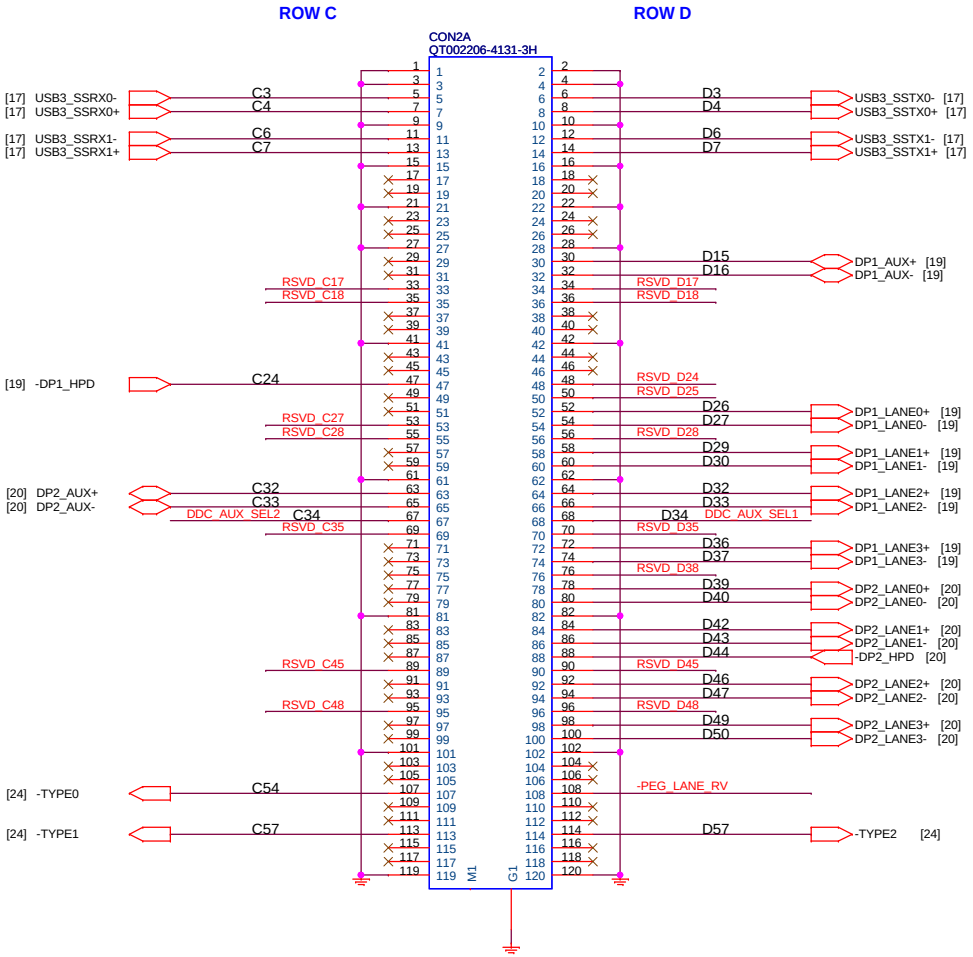

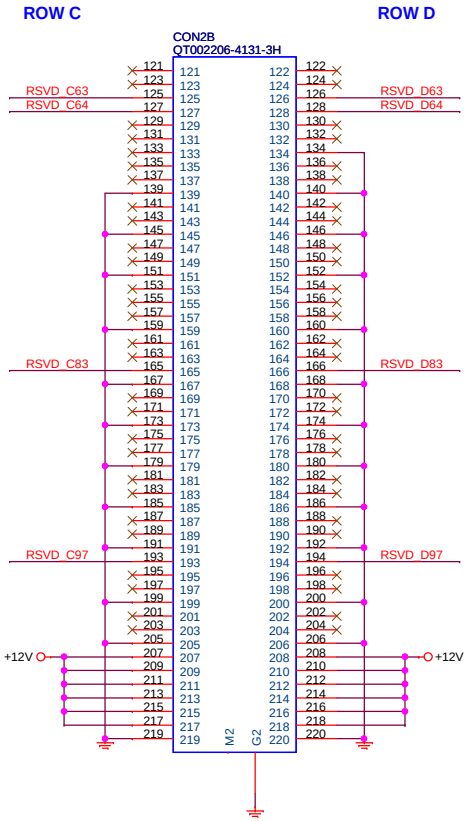

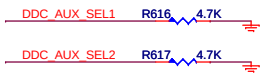

DDI Configuration:

DDI 1: DISPLAY PORT
DDI 2: DISPLAY PORT

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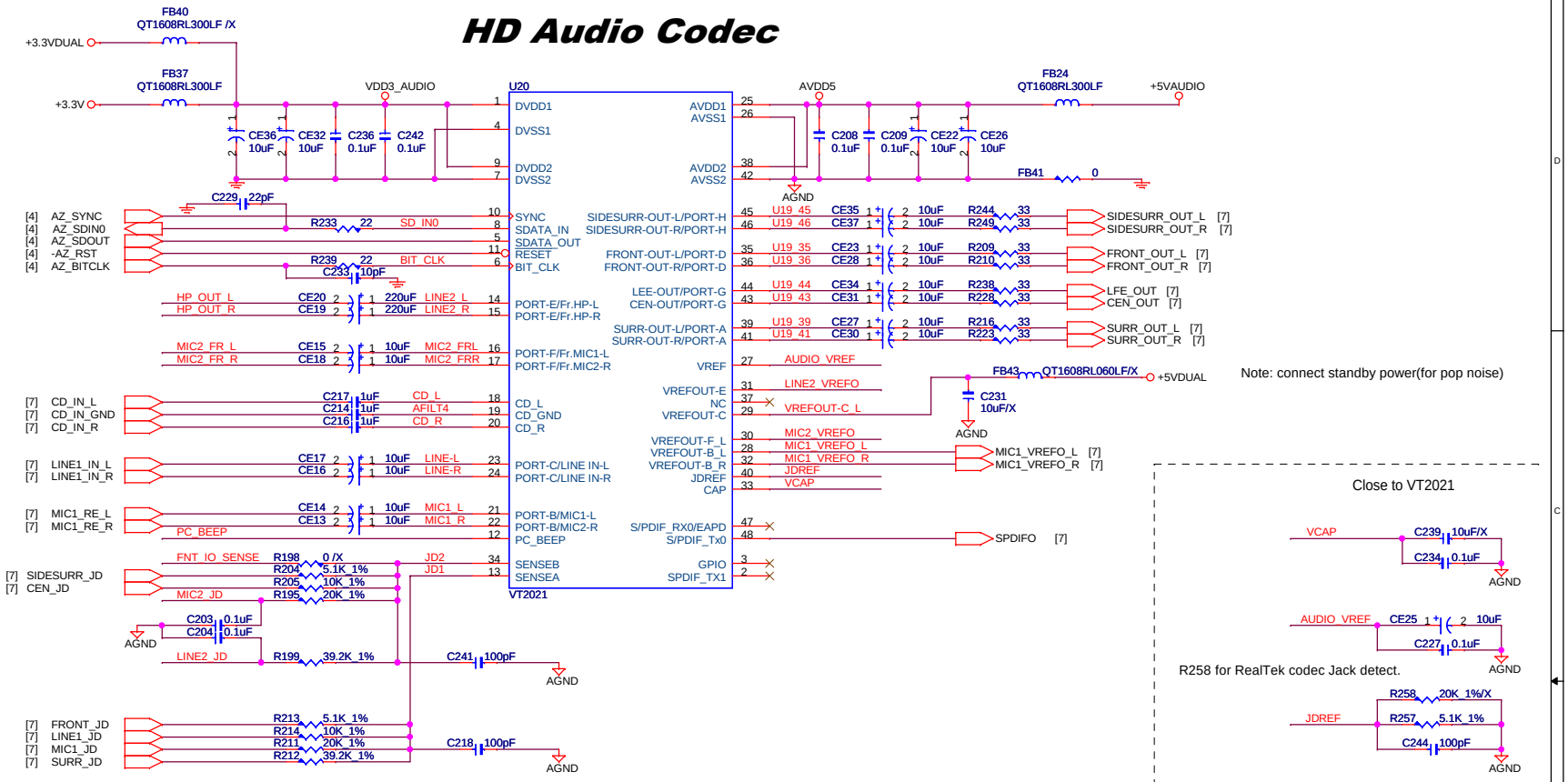
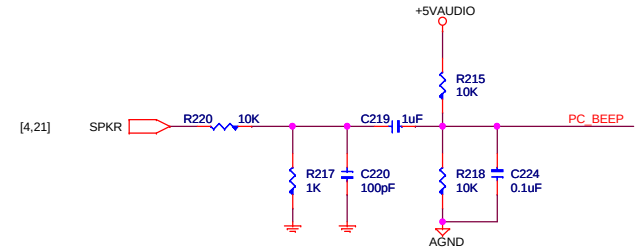
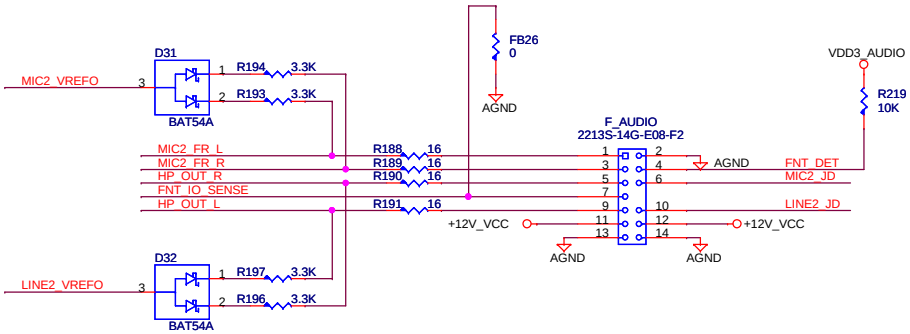
HD Audio Codec

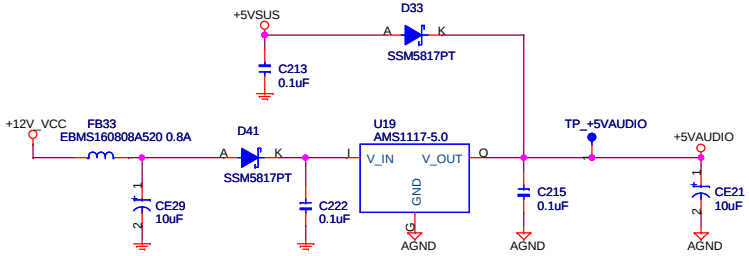


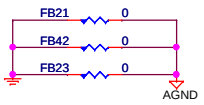


FRONT AUDIO



+5VAUDIO





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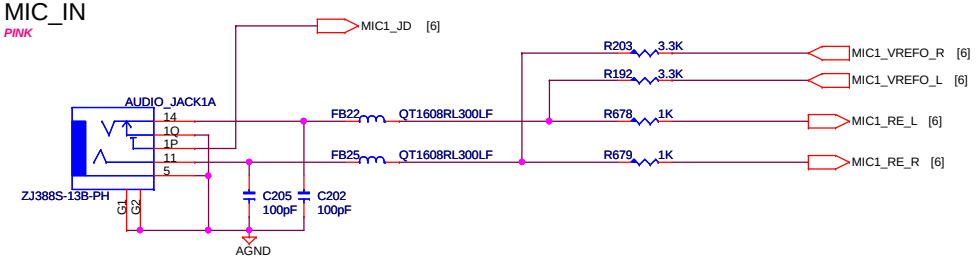
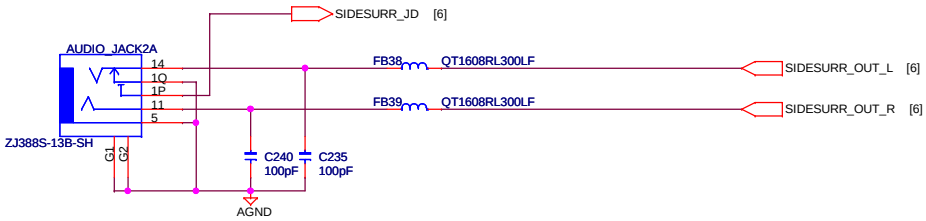
MIC_IN

PINK



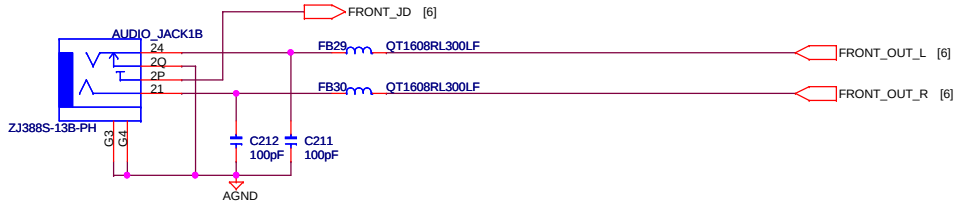
SIDESURR_OUT

GREY



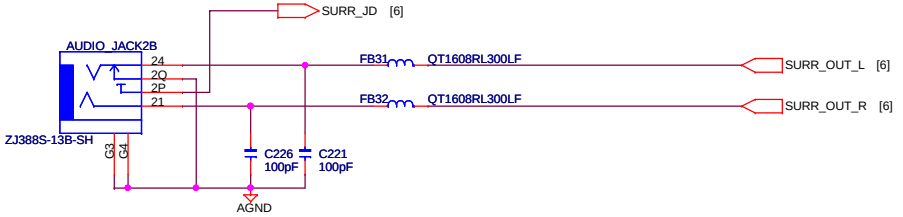
FRONT_OUT

GREEN



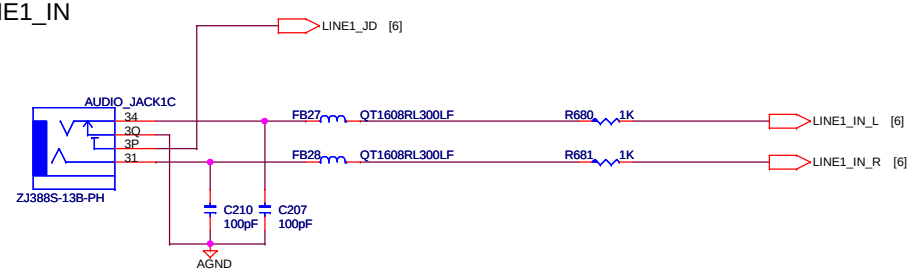
SURR_OUT

BLACK



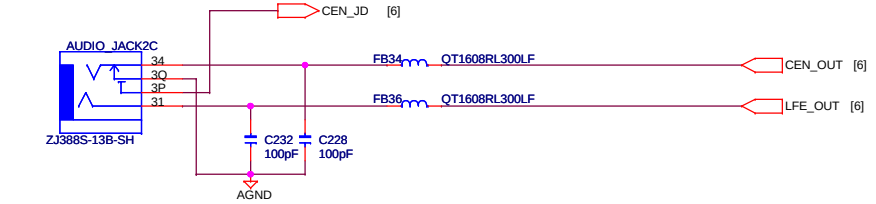
LINE1_IN

BLUE

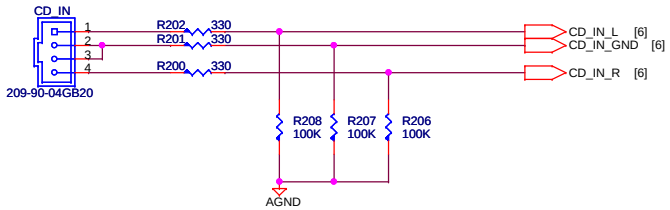


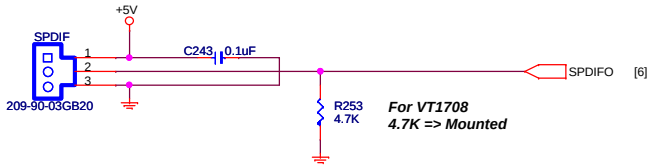
CENTER/LFE

ORANGE



CD_IN





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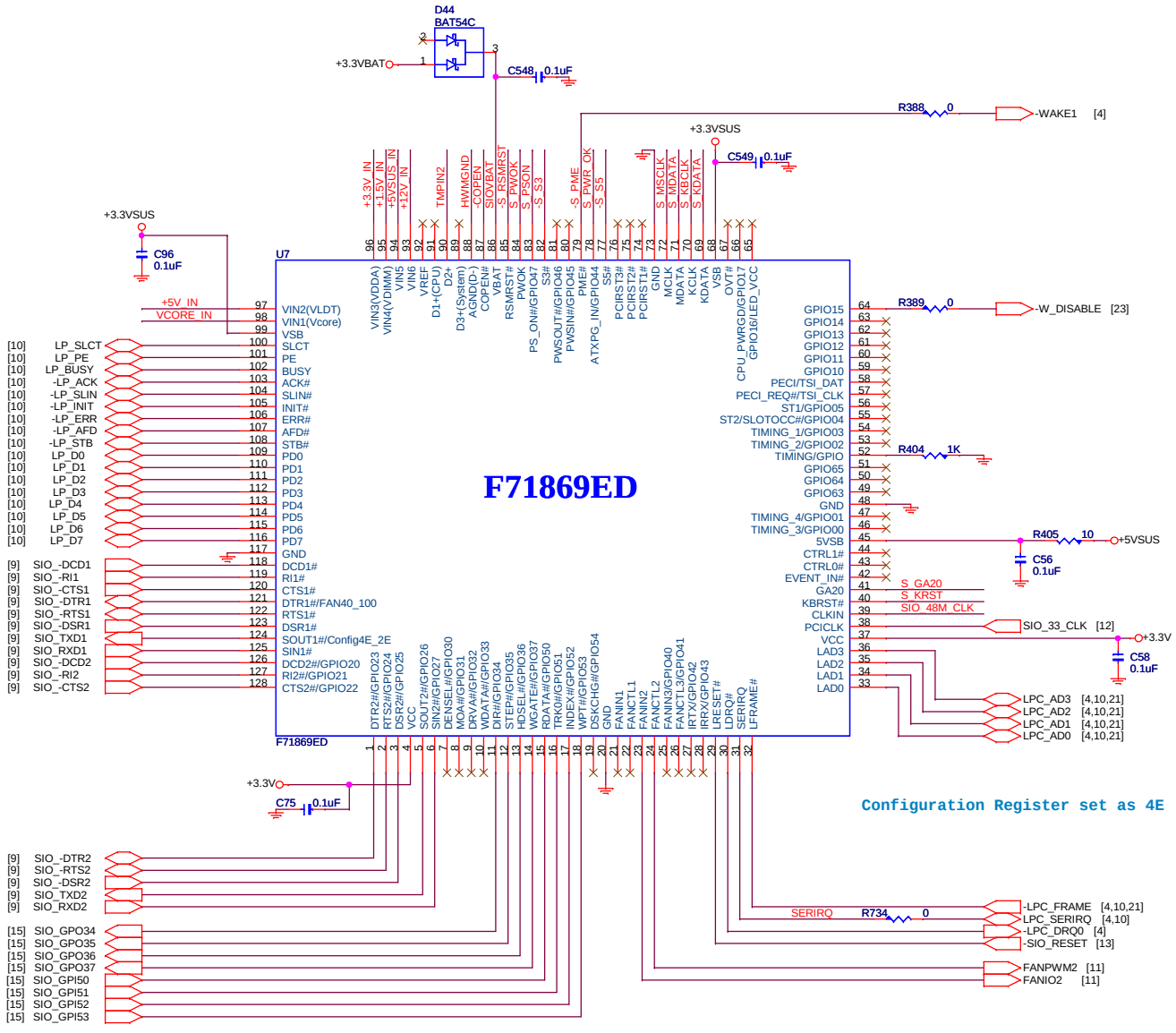
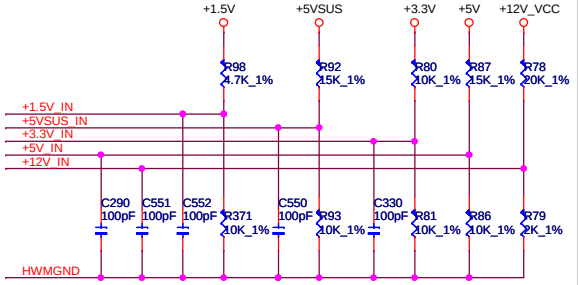
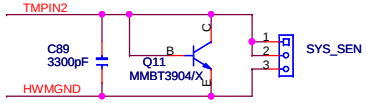
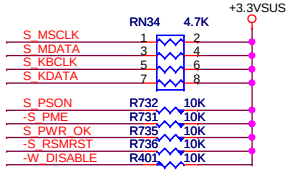
F71869ED

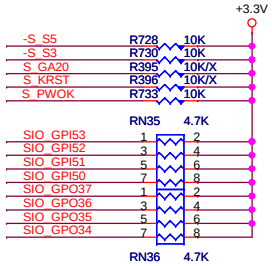




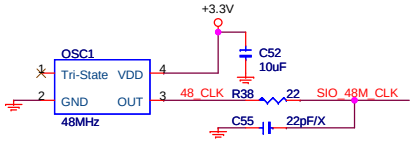


C400,C403 close to SIO
Q13 places on top side





SOUT1 pull low for 2E



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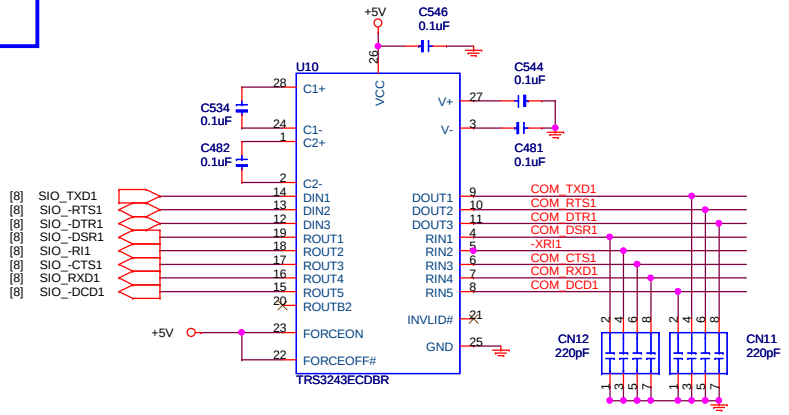
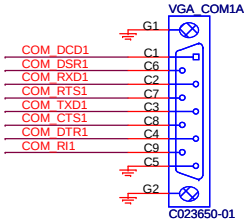
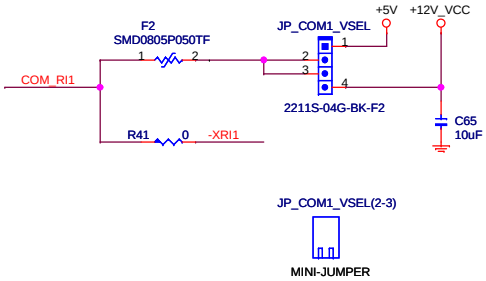
COM 1

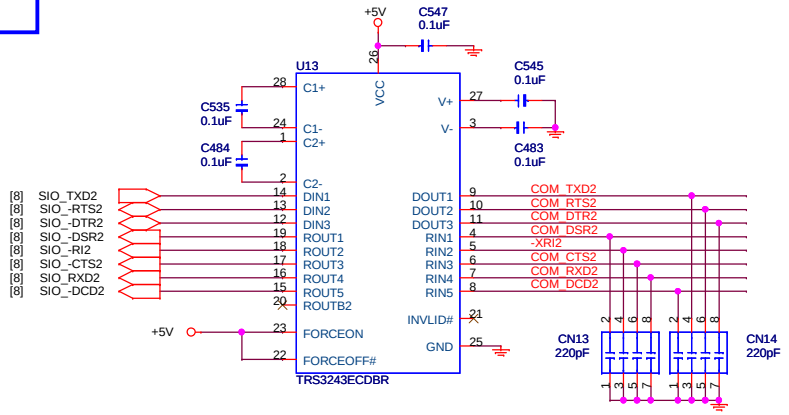


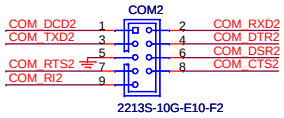


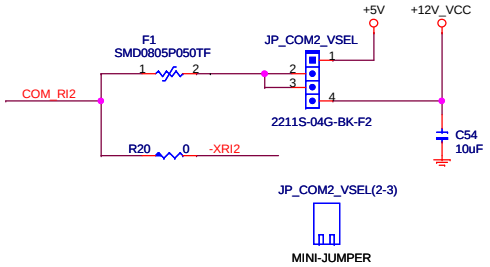


JP_COM1_VSEL	VOLTAGE
1-2	+5V
2-3	Normal *
3-4	+12V

COM 2

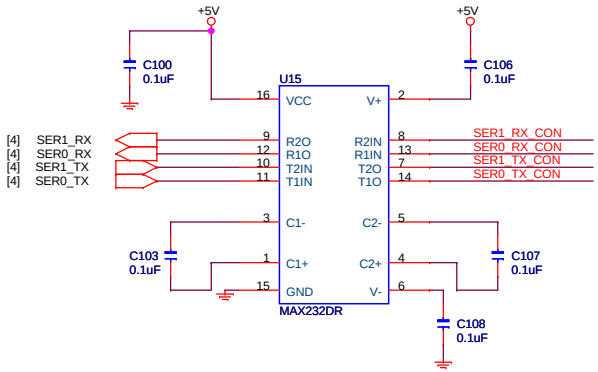


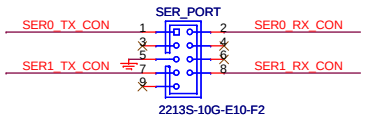




JP_COM2_VSEL	VOLTAGE
1-2	+5V
2-3	Normal *
3-4	+12V

General Purpose Serial Ports





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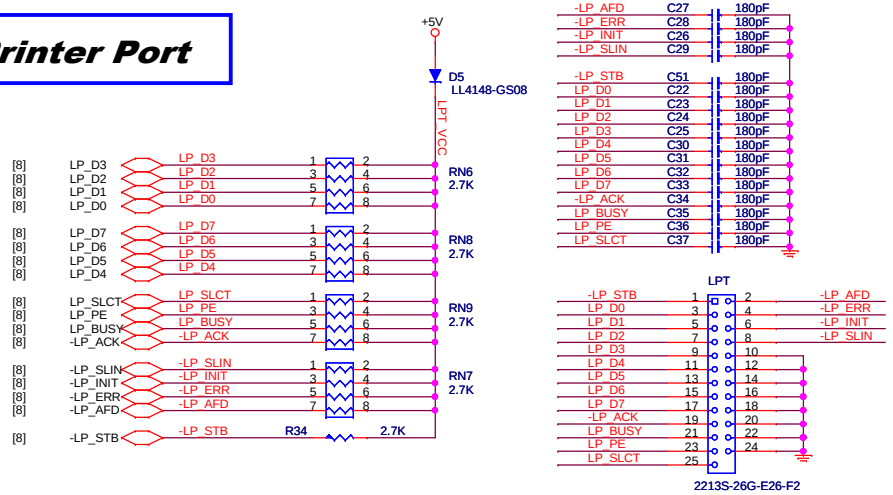
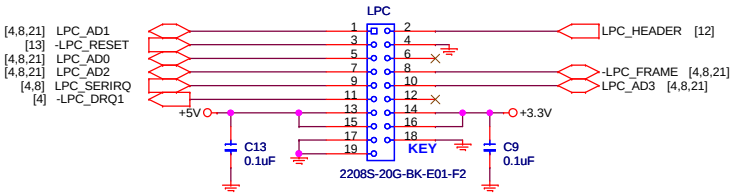
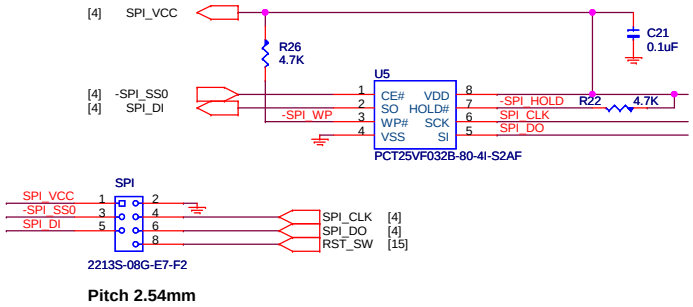
Printer Port



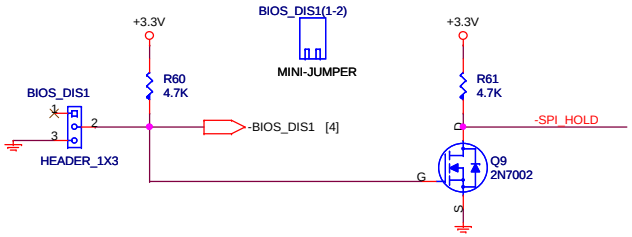
LPC HEADER



SPI ROM



BIOS DISABLE



BIOS Selection Table

BIOS_DISABLE	BIOS_DIS1
MODULE SPI BIOS	1 - 2 *
CARRIER SPI BIOS	2 - 3

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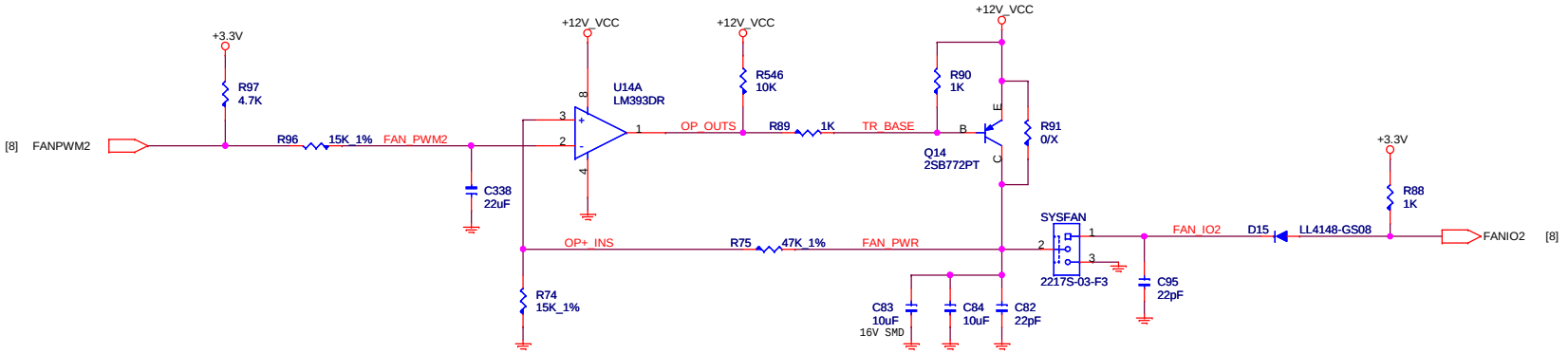
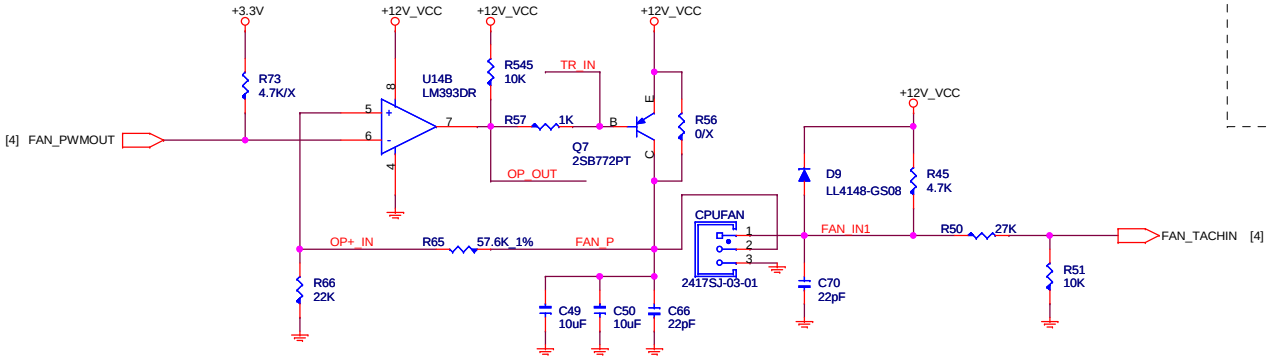
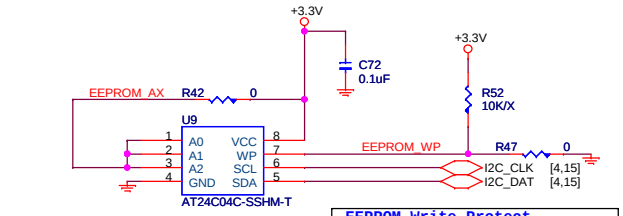
SYSTEM FAN



CPU FAN



EEPROM



EEPROM Write Protect	
GND	Normal Operation *
+3.3V	Write Protect

Device Address = 0x57(0xAE)

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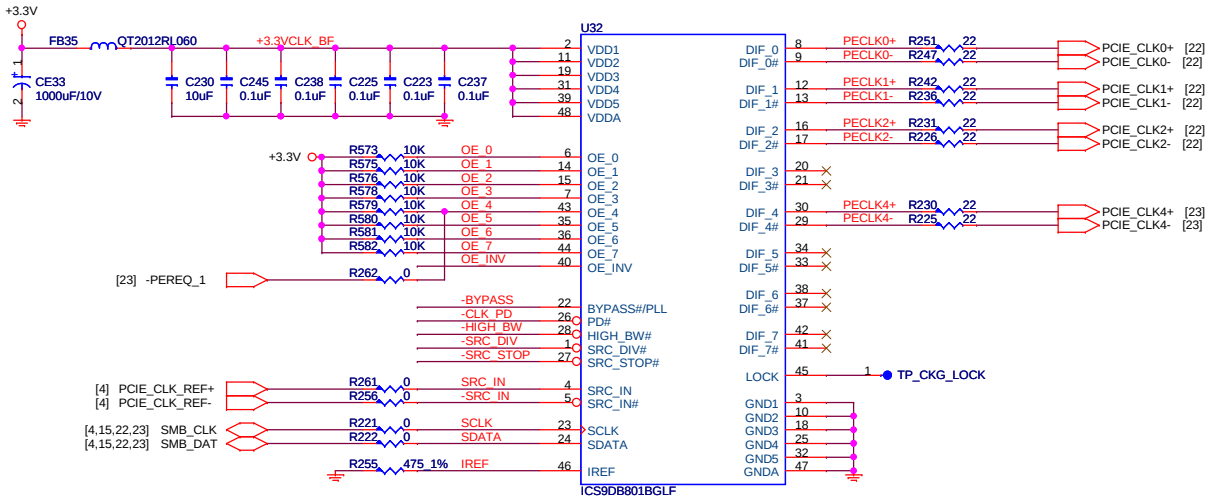
PCIE CLOCK BUFFER

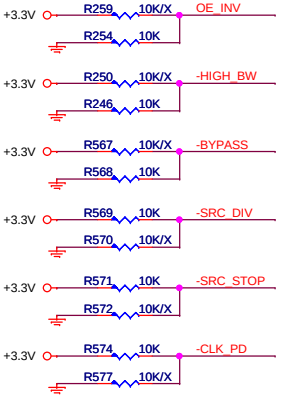


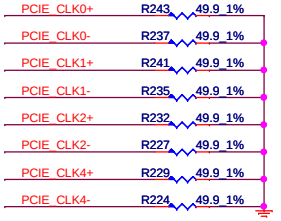
TO PE1 SLOT

TO PE2 SLOT

TO PE3 SLOT

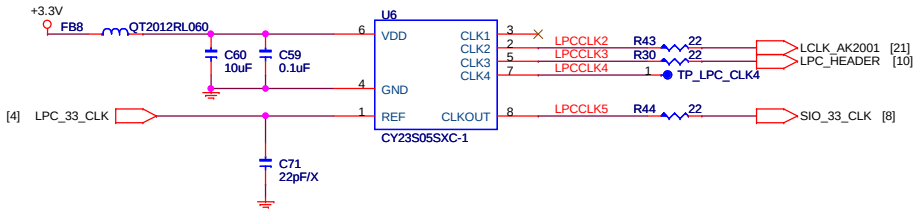
TO Mini PCI-e

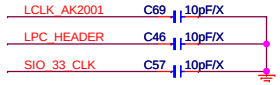




meet Zdif=49.9 ohm

LPC CLOCK BUFFER





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VIA TECHNOLOGIES INC.

Title	PCIE/ PCI Clock Buffer	
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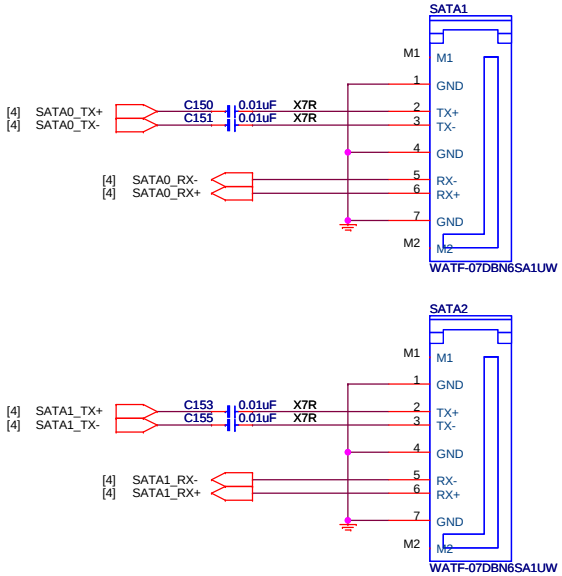
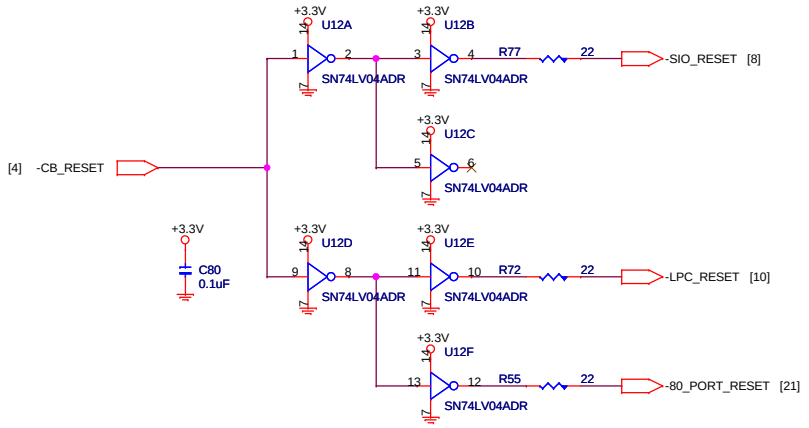
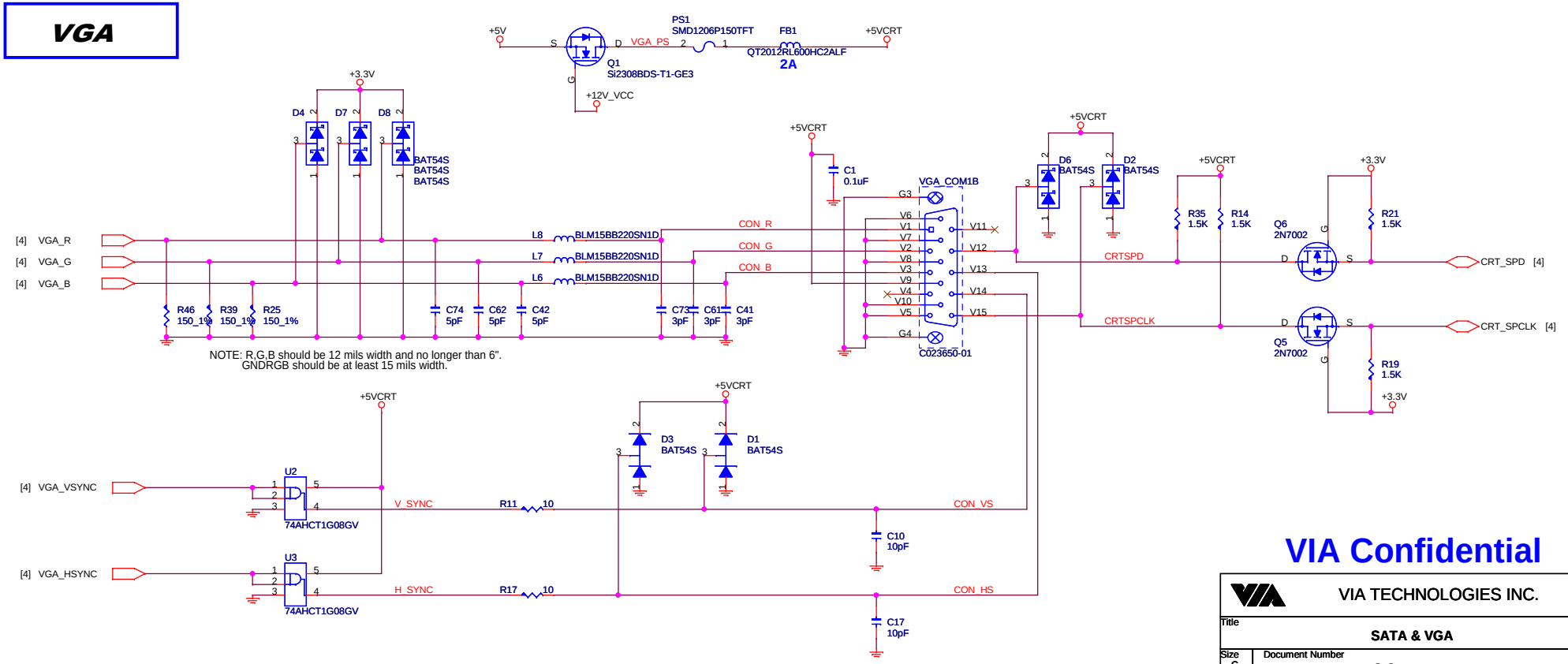
SATA





VGA



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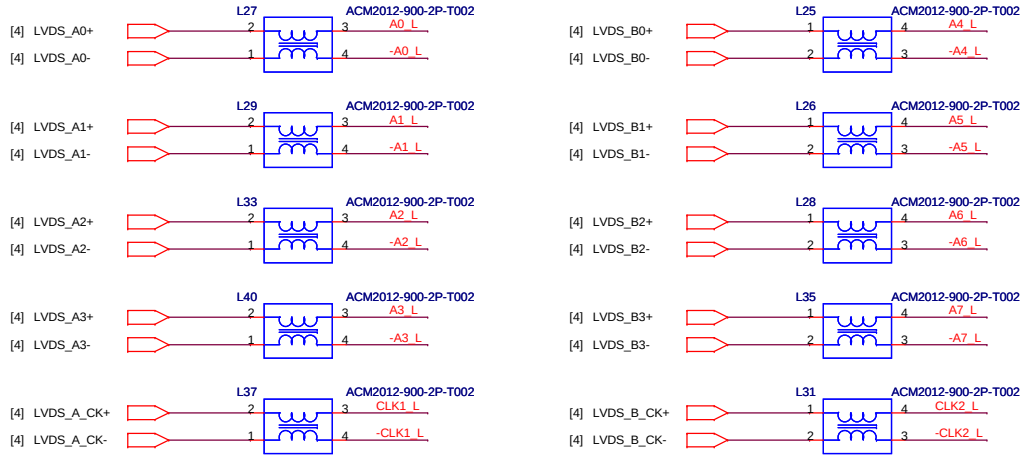
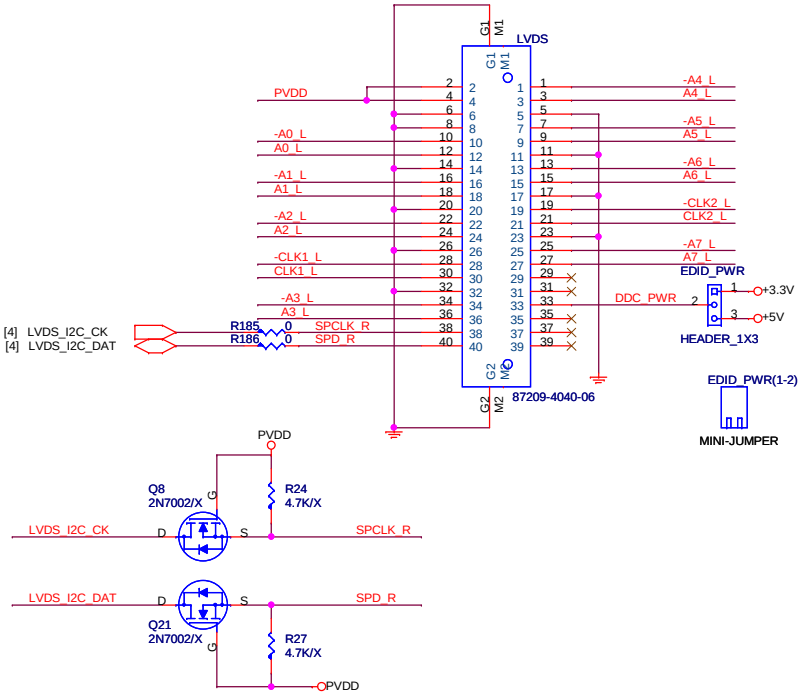
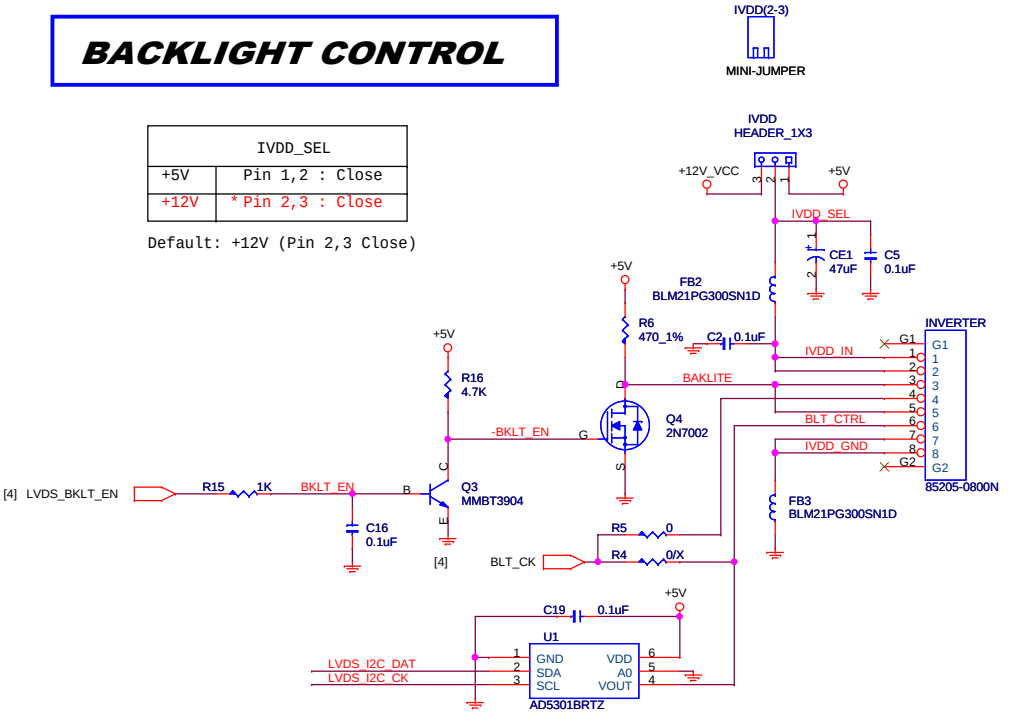
LVDS CONNECTOR





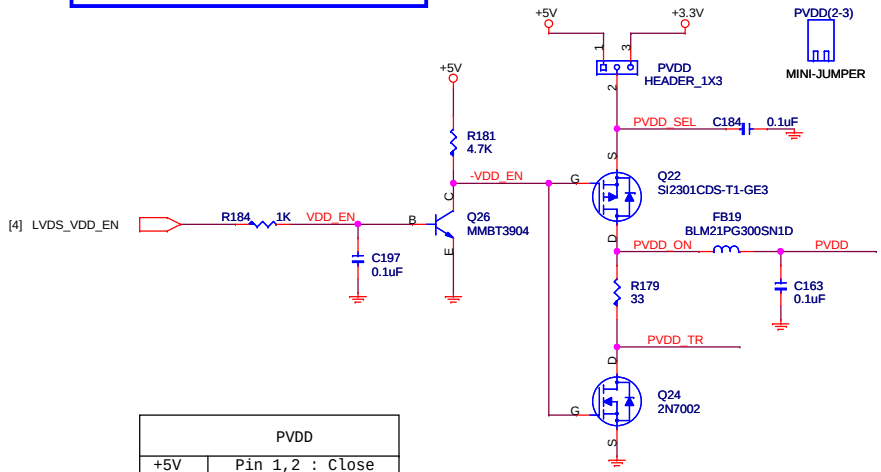
BACKLIGHT CONTROL



IVDD_SEL	
+5V	Pin 1,2 : Close
+12V	* Pin 2,3 : Close

Default: +12V (Pin 2,3 Close)

PANEL POWER



PVDD	
+5V	Pin 1,2 : Close
+3.3V	* Pin 2,3 : Close

Default: +3.3V (Pin 2,3 Close)

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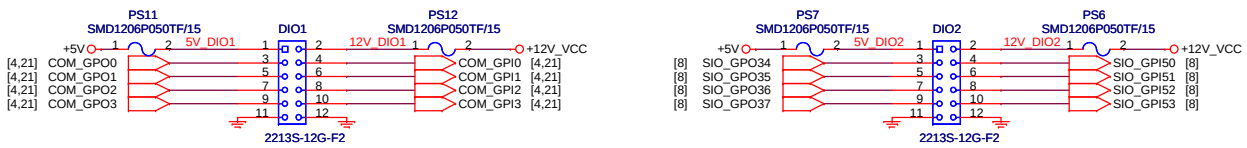
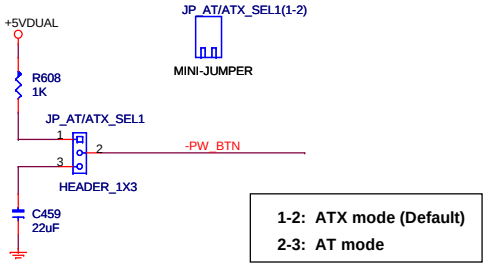
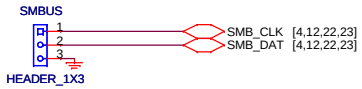
Digital I/O



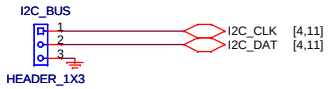
AT/ATX Mode Select



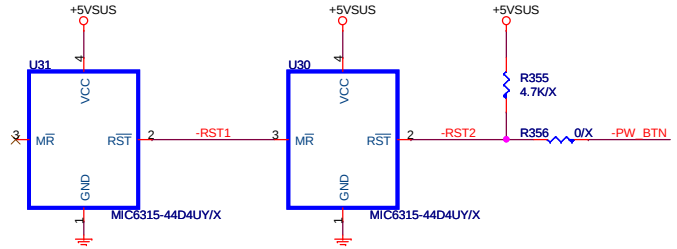
SMBUS



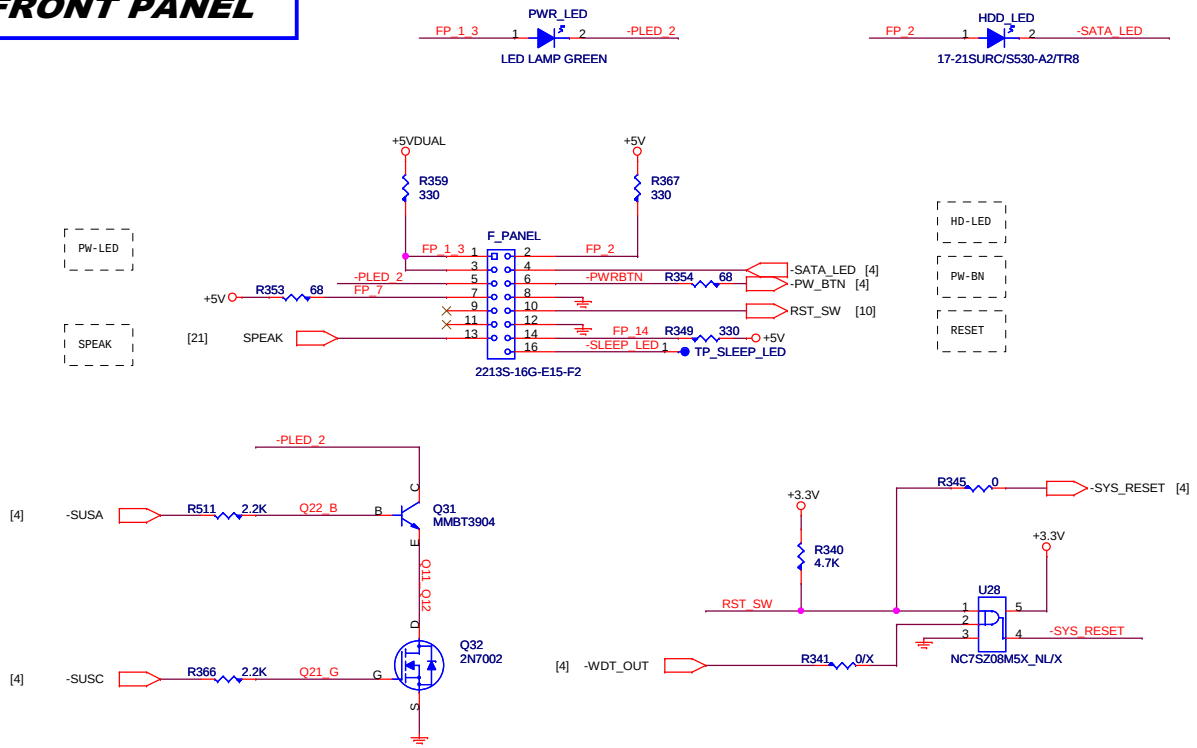
I2C_BUS



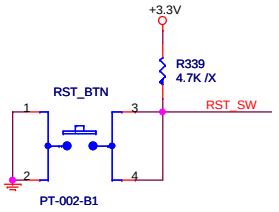
RESET_IC



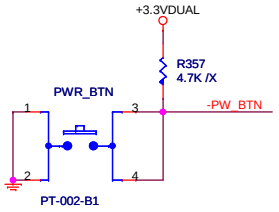
FRONT PANEL



RESET_BTN



PWRBTN



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Title: FPNL, DIO, SMBUS, I2C		
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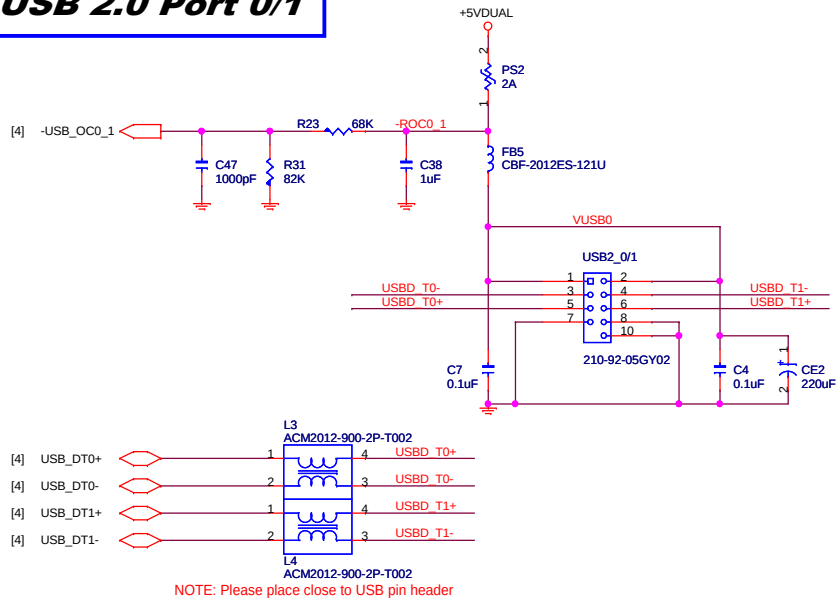
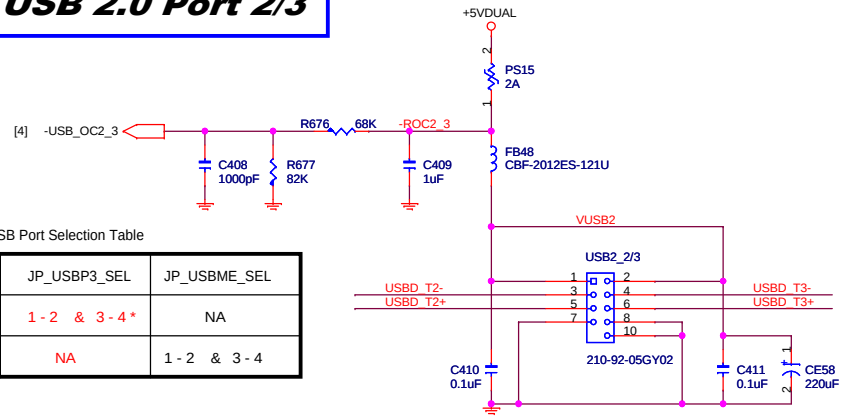
USB 2.0 Port 0/1



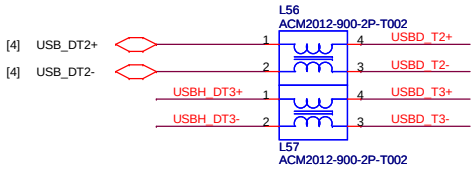
NOTE: Please place close to USB pin header

USB 2.0 Port 2/3

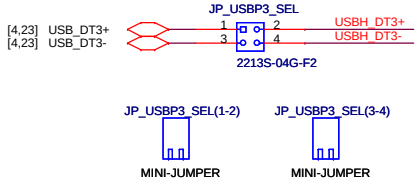


USB Port Selection Table

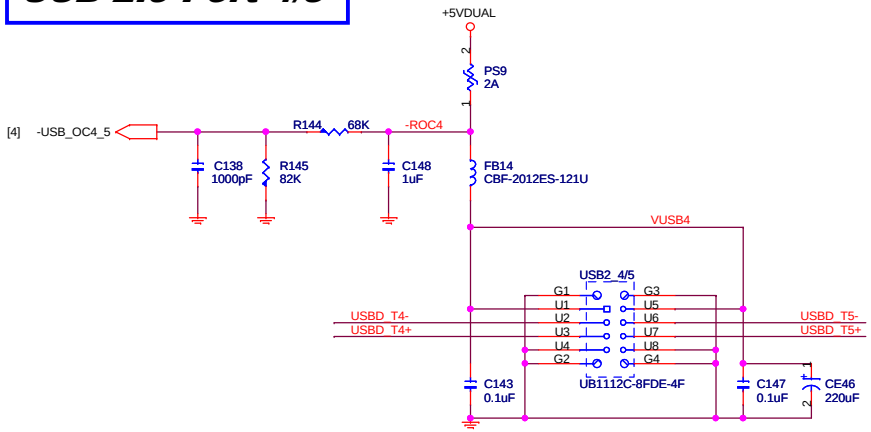
USB Port Select	JP_USBP3_SEL	JP_USBME_SEL
USB Port 3	1 - 2 & 3 - 4 *	NA
Mini PCIE USB	NA	1 - 2 & 3 - 4

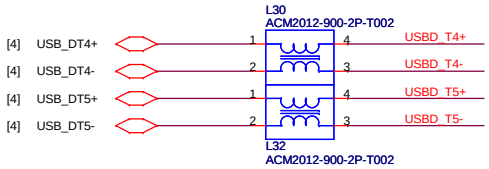


NOTE: Please place close to USB pin header



USB 2.0 Port 4/5





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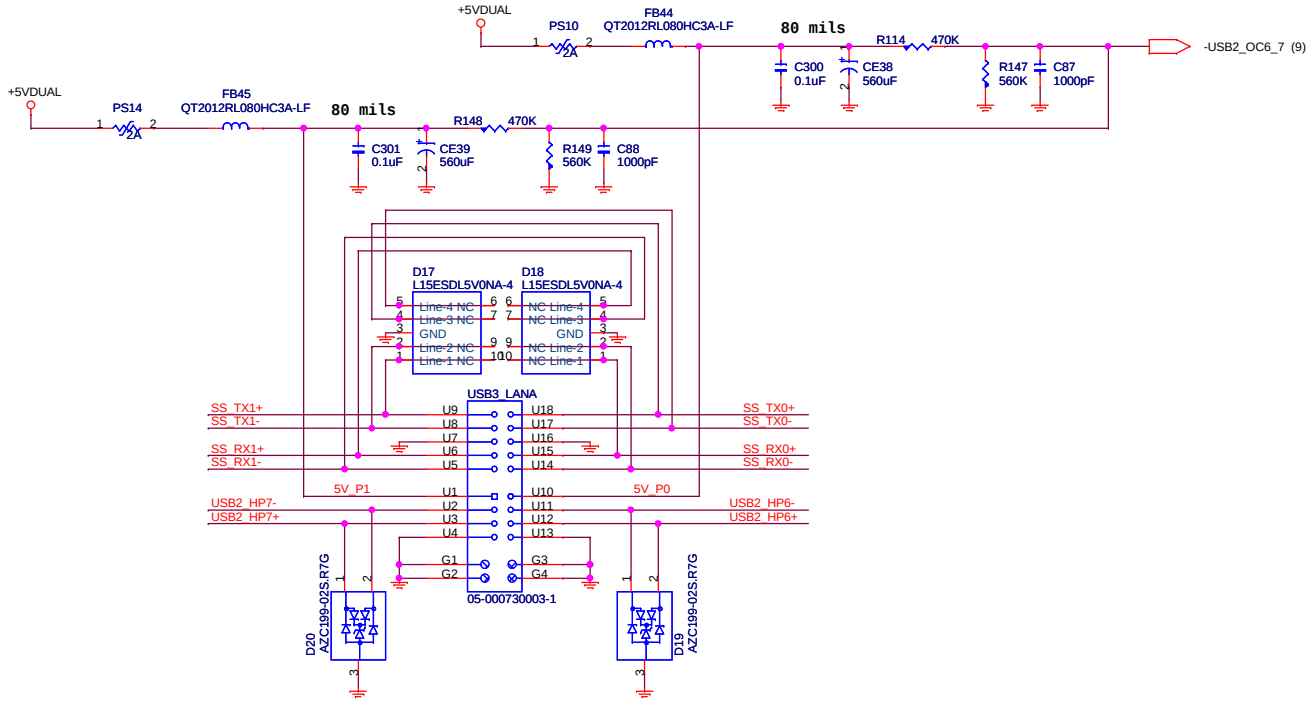
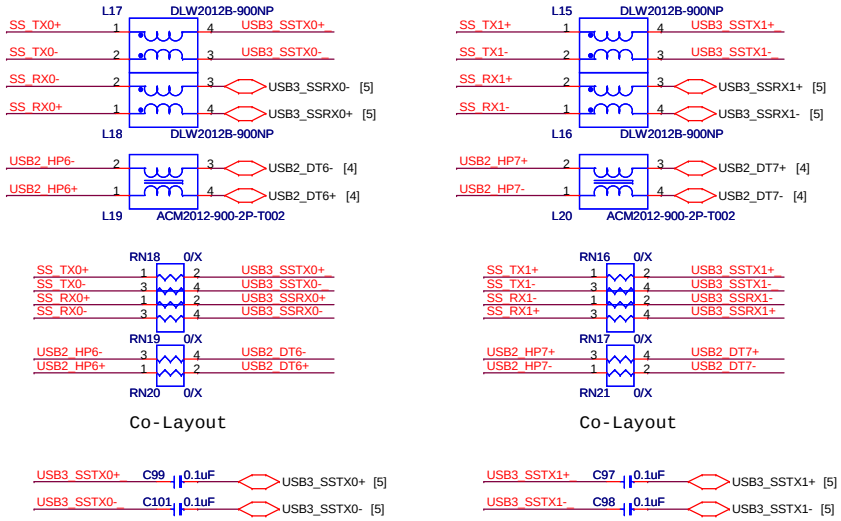
USB 3.0 Port 0 & 1





Note: Please place those parts close to USB Connector

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Title	USB 3.0 Ports	
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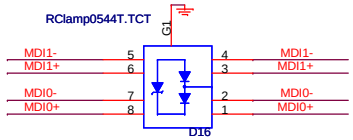
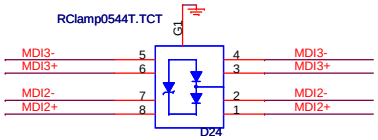
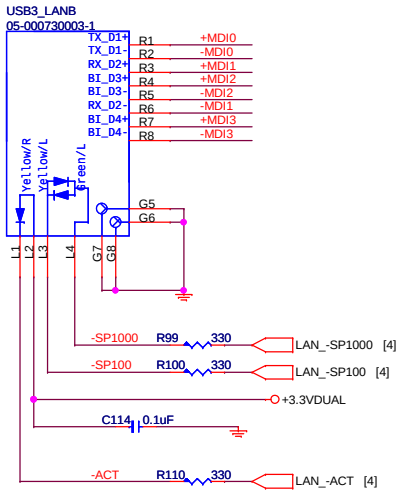
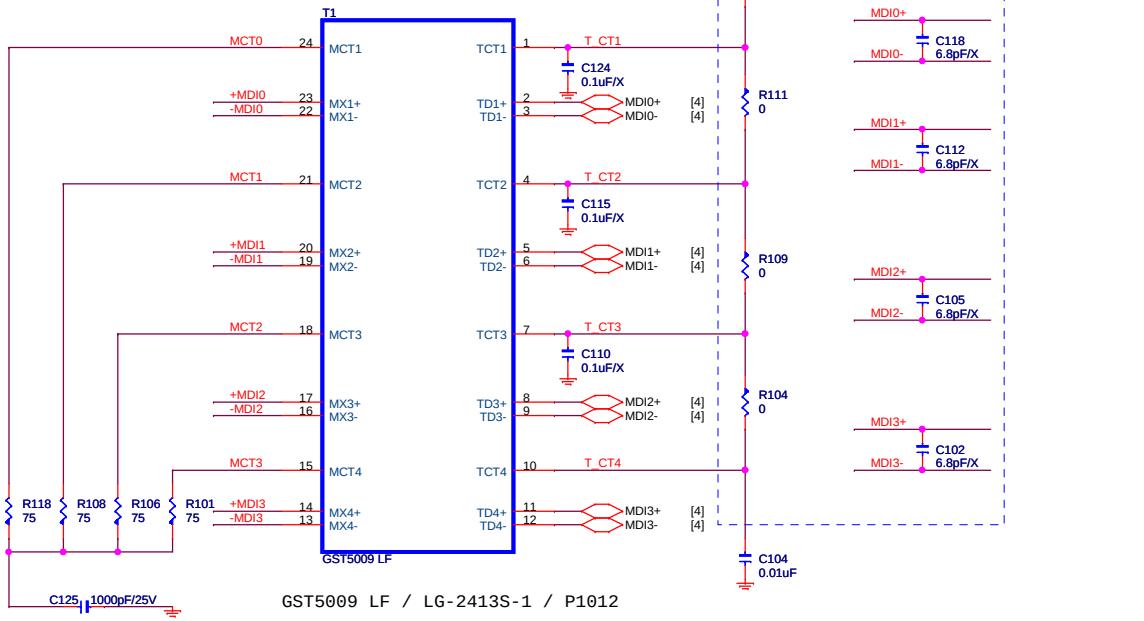
RJ45









GST5009 LF / LG-2413S-1 / P1012

RJ45 Link status GMTI_05-000730003-1 for RTL8111G

LED Selection	LEDCFG (0F, 42)	
	Link	Active
LAN Connector not Plug	Black	Black
10M Bits	Black	Orange (Blinking)
100M Bits	Green	Orange (Blinking)
1000M Bits	Orange	Orange (Blinking)

Note: Link: LED on

VT6107 T1 install TST1284A LF
VT6122 / VT6130 / RTL8111G T1 install GST5009 LF

T1	VT6107	RTL8111G / VT6122 / VT6130
Bothhand	TST1284A LF 99G26-070542	GST5009 LF 99G26-070532
LANKOM	LF-H6442S-1 99G26-07055F	LG-2413S-1 99G26-07056F
UDE	P1212(007-00) 99G26-07058J	P1012(001-00) 99G26-07053J

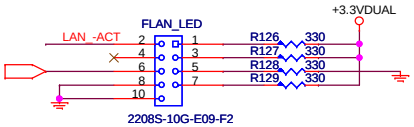
	T1	C124,C115	C110	C104	FB17	R111	R104, R109	C118,C112,C105,C102(6.8pFx4)
RTL8111G	GST5009 LF 99G26-070532	X	X	0.01uF	X	0	0	X
VT6107	TST1284A LF 99G26-070542	0	X	X	0	0	X	X
VT6122	GST5009 LF 99G26-070532	0	0	0.1uF	X	X	X	0
VT6130	GST5009 LF 99G26-070532	0	0	0.1uF	0	0	0	X

O:mount X:unmount

FRONT LAN LED

1st _:_LAN LED_
Wireless LAN LED
Standby PW LED(optional)

[23] W_LESS_LED



	NEW_1
LED0	SP100
LED1	SP1000
LED2	ACT

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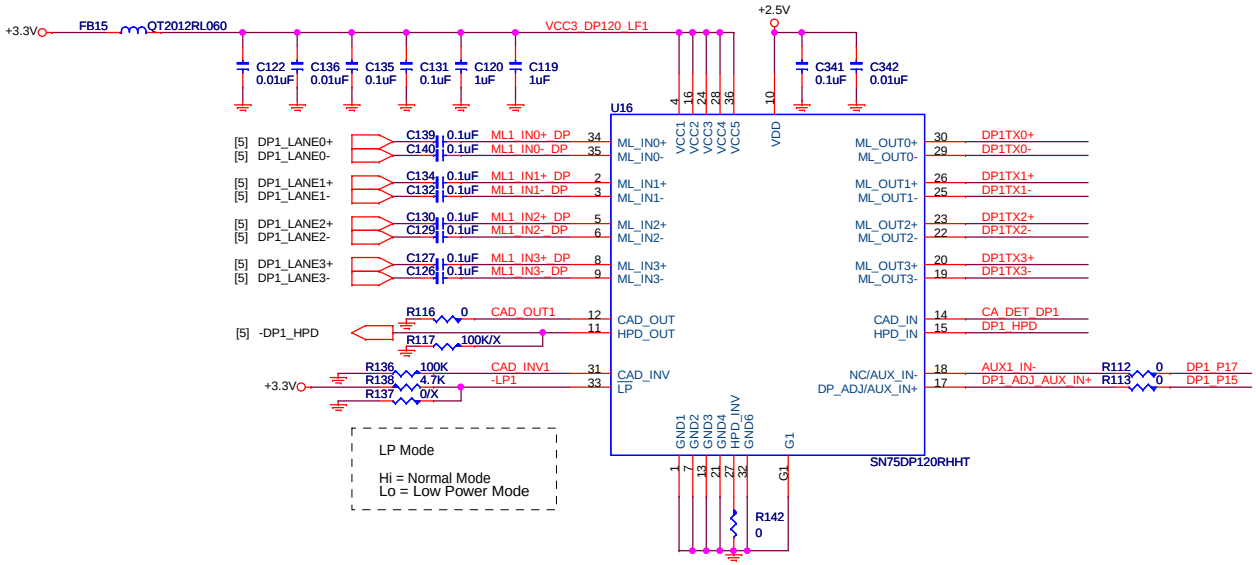
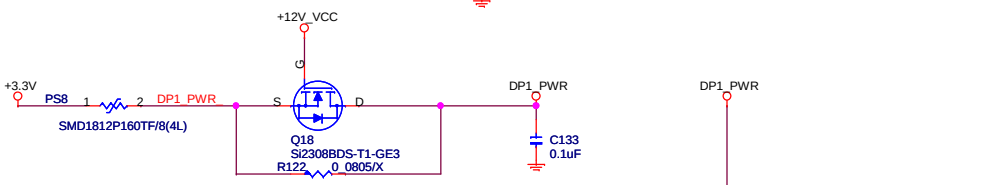
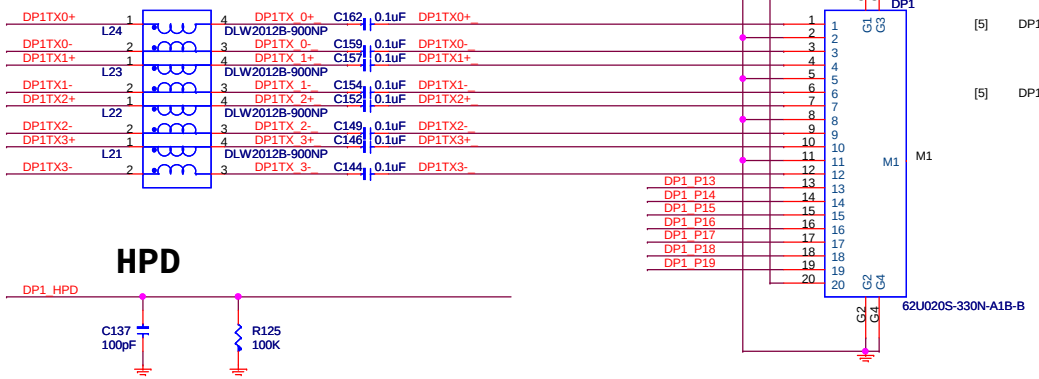
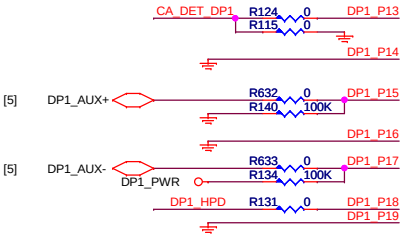
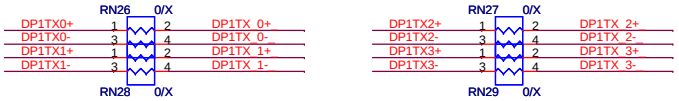
DP reDriver



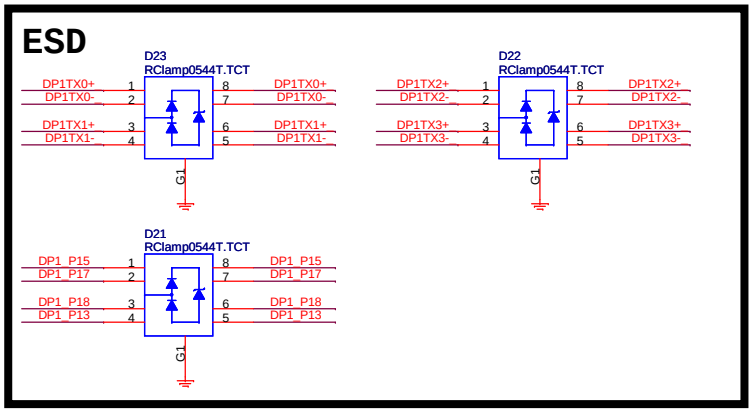








ESD Rcalmp
RCLAMP0524P(Package:GSLP2510P8)
RCLAMP0544T(Package:GSLP2010P8T)



	DisplayPort
1	ML_Lane0+
2	GND
3	ML_Lane0-
4	ML_Lane1+
5	GND
6	ML_Lane1-
7	ML_Lane2+
8	GND
9	ML_Lane2-
10	ML_Lane3+
11	GND
12	ML_Lane3-
13	GND
14	GND
15	AUX_CH+
16	GND
17	AUX_CH-
18	H.P. Detect
19	DP_PWR_Return
20	DP_PWR

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Title: DP1 ReDriver SN75DP120

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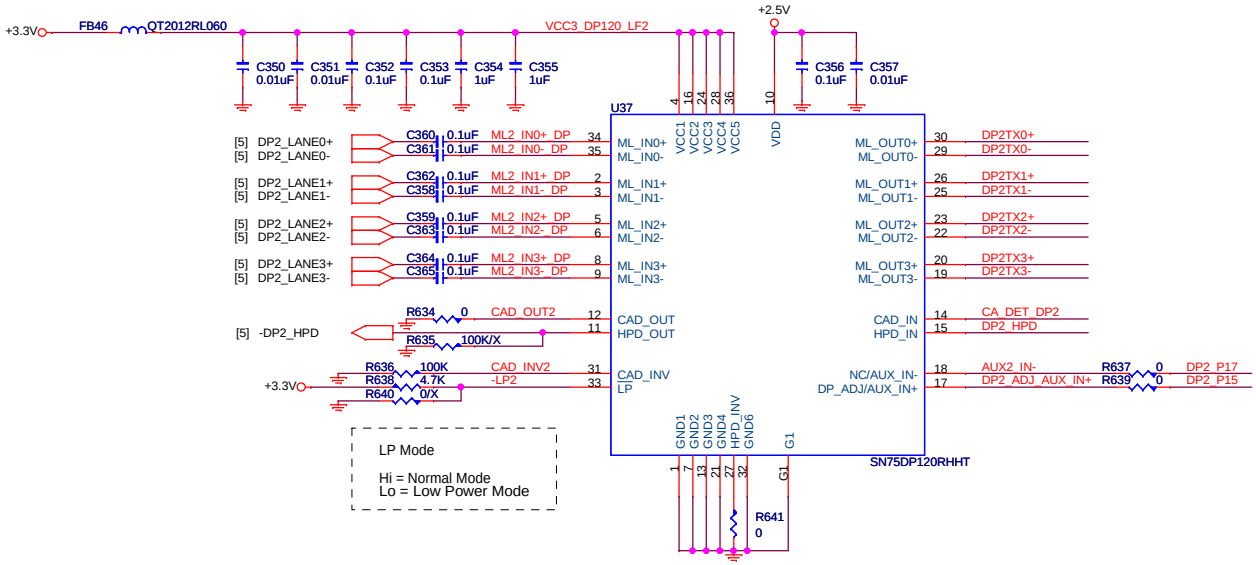
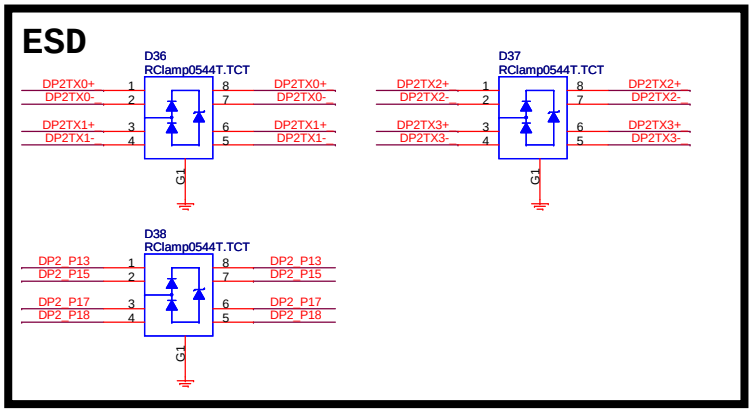
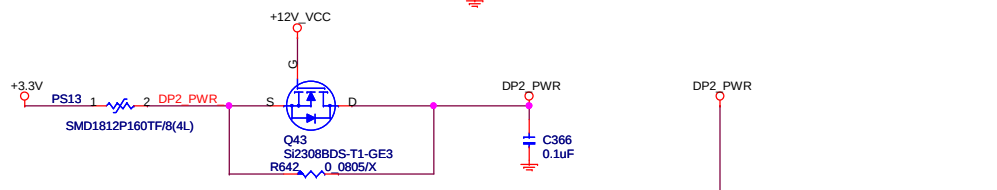
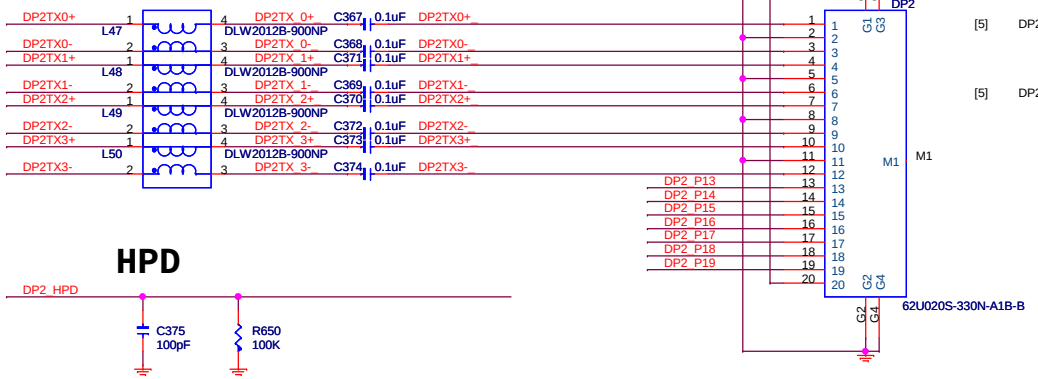
DP reDriver

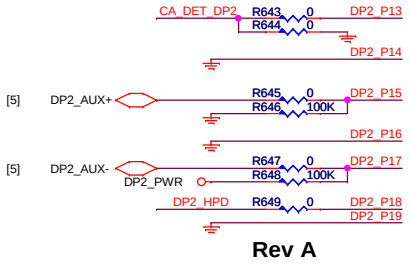


ESD Rcalmp
RCLAMP0524P(Package:GSLP2510P8)
RCLAMP0544T(Package:GSLP2010P8T)



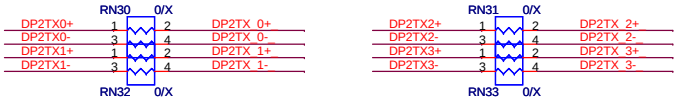






Rev A

HPD



	DisplayPort
1	ML_Lane0+
2	GND
3	ML_Lane0-
4	ML_Lane1+
5	GND
6	ML_Lane1-
7	ML_Lane2+
8	GND
9	ML_Lane2-
10	ML_Lane3+
11	GND
12	ML_Lane3-
13	GND
14	GND
15	AUX_CH+
16	GND
17	AUX_CH-
18	H.P. Detect
19	DP_PWR_Return
20	DP_PWR

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Title: DP2 ReDriver SN75DP120

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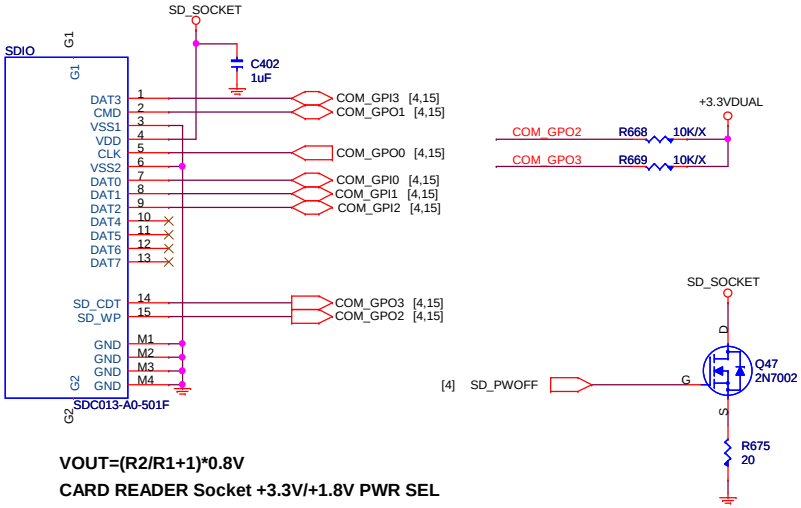
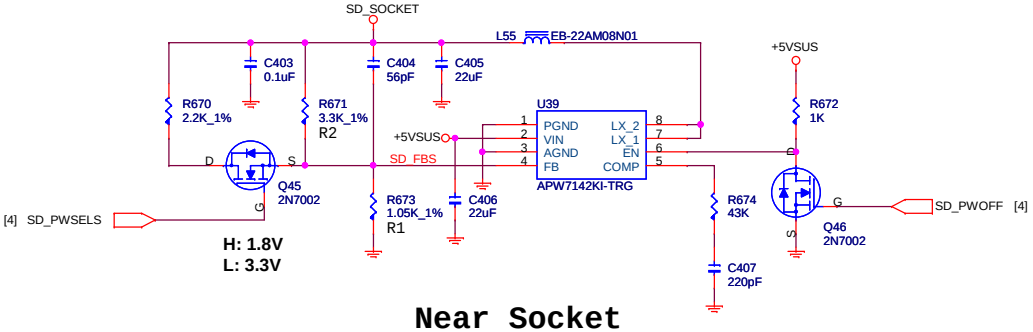
SD/MMC Socket



GPIO	SDIO
COM_GPI0	SD_D0
COM_GPI1	SD_D1
COM_GPI2	SD_D2
COM_GPI3	SD_D3
COM_GPO0	SD_CLK
COM_GPO1	SD_CMD
COM_GPO2	SD_WP
COM_GPO3	SD_CD#

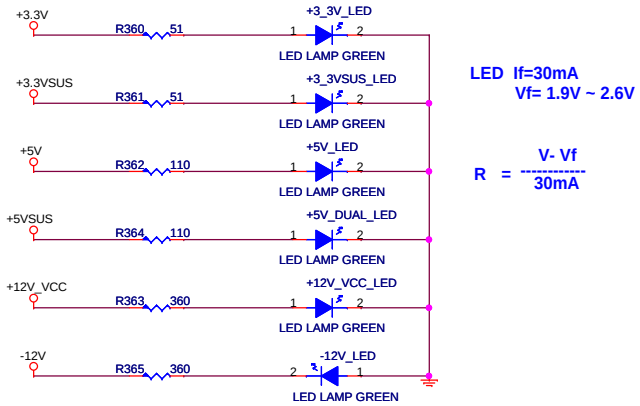


Near Socket

VOUT=(R2/R1+1)*0.8V

CARD READER Socket +3.3V/+1.8V PWR SEL

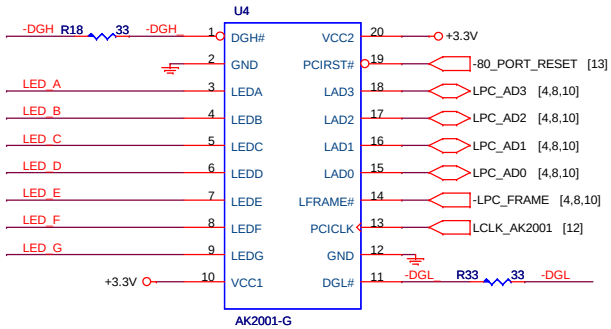
LED

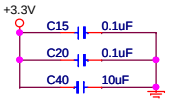


LED If=30mA
Vf= 1.9V ~ 2.6V

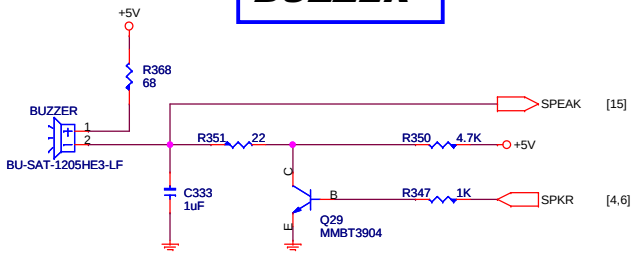
$$R = \frac{V - Vf}{30mA}$$

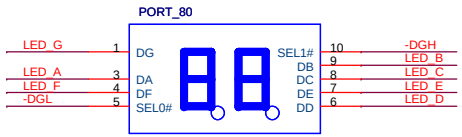
LPC DEBUG PORT





BUZZER





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Title	LPC Debug Port, SDIO, LED	
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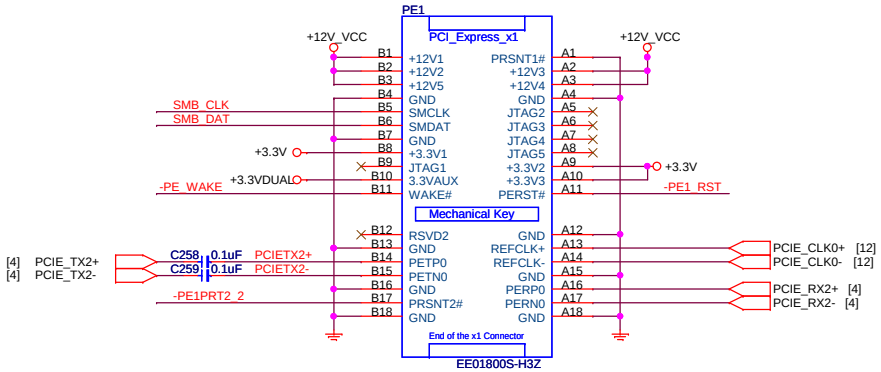
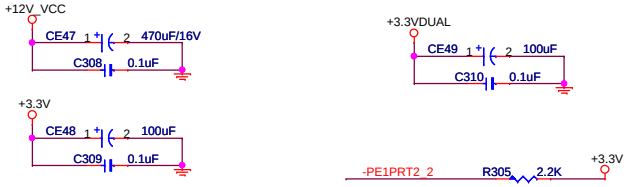
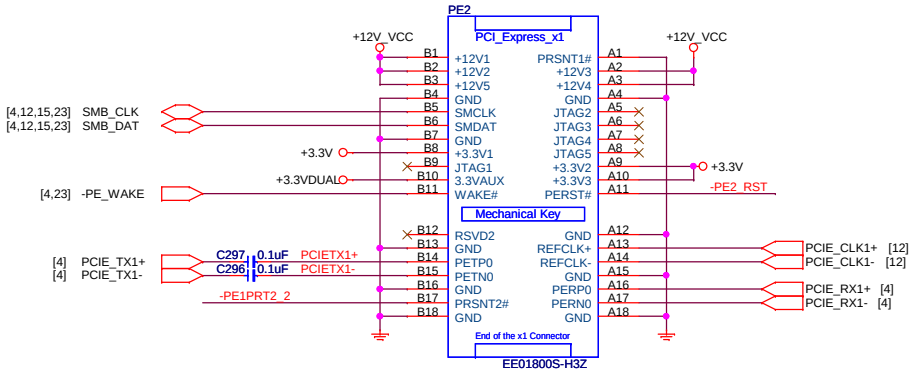
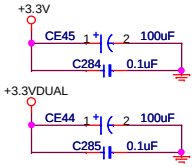
#1 PCIE X 1 SLOT

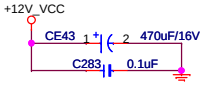




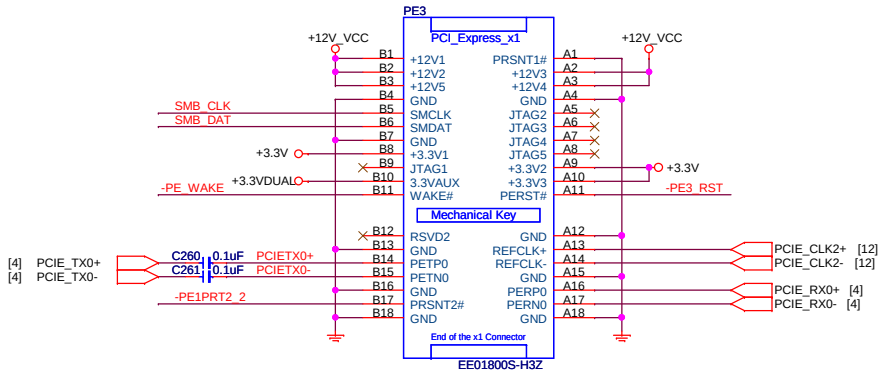
#2 PCIE X 1 SLOT

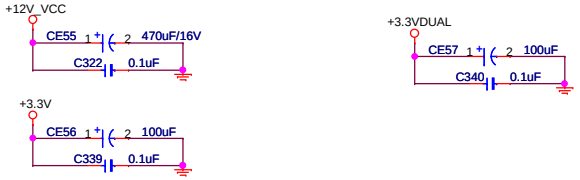


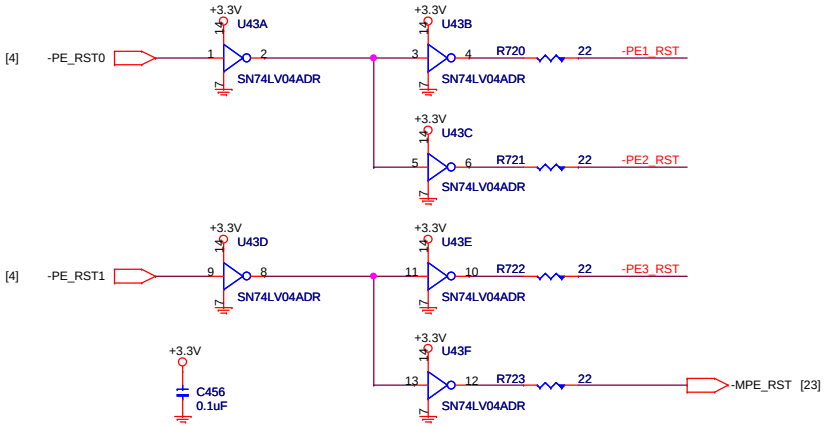




#3 PCIE X 1 SLOT







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Title	PCI Express x1 Slots
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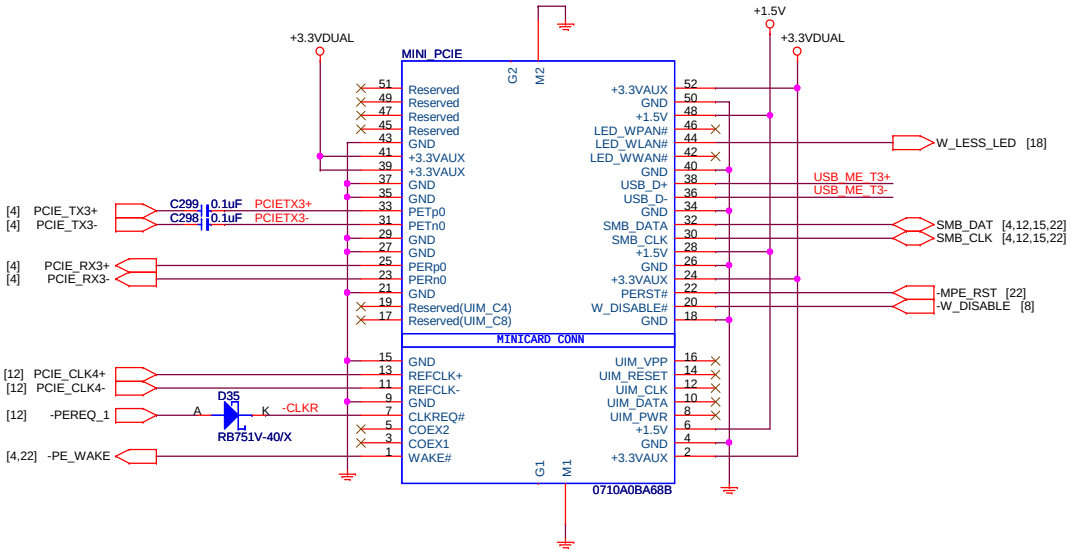
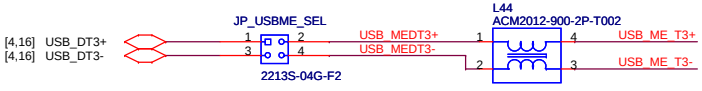
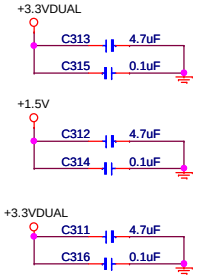
Mini PCIE Socket







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Title	Mini PCIe Slot	
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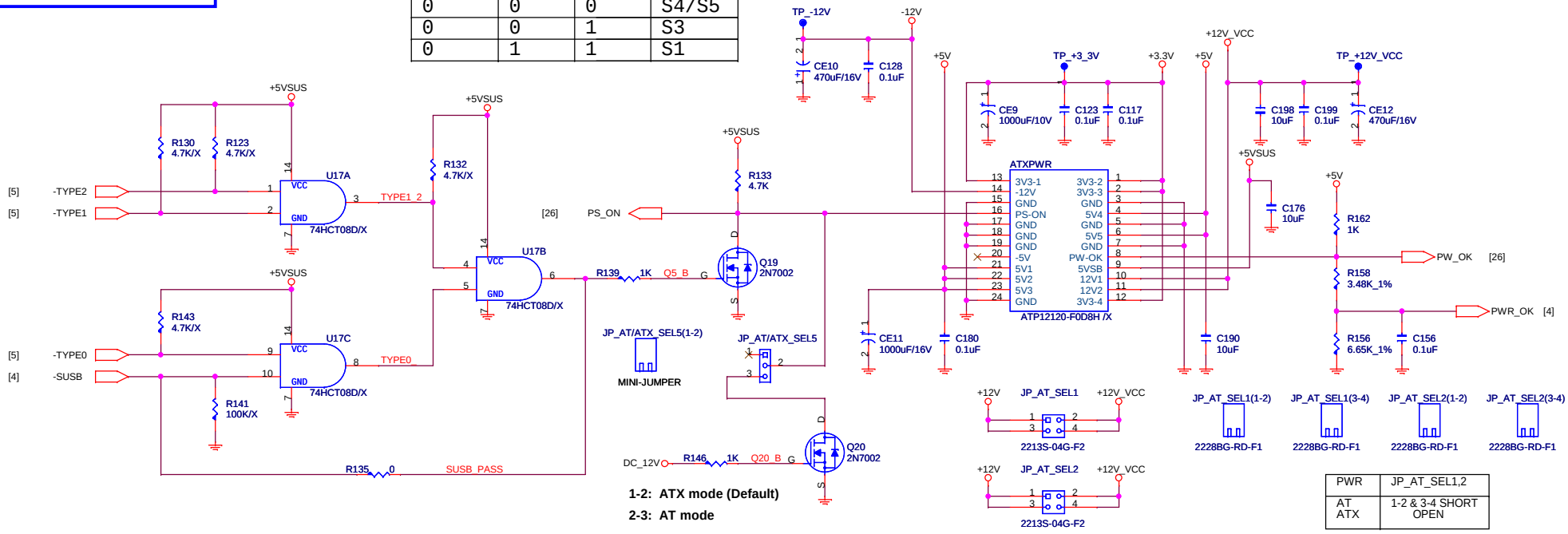
ATX POWER

-SUSA	-SUSB	-SUSC	Pstate
0	0	0	S4/S5
0	0	1	S3
0	1	1	S1

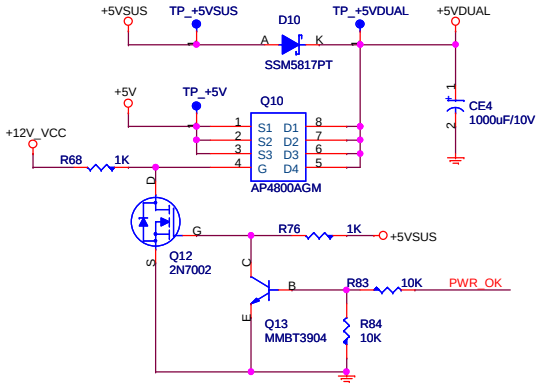


1-2: ATX mode (Default)

2-3: AT mode

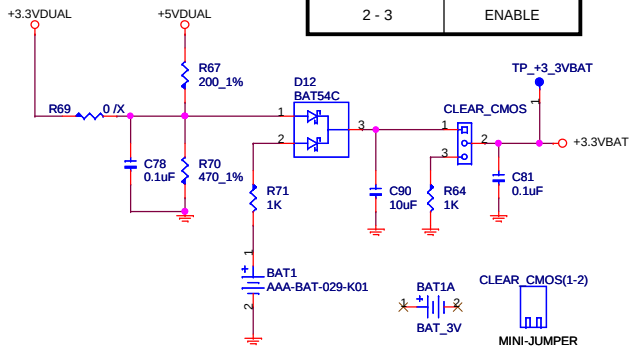
PWR	JP_AT_SEL1,2
AT ATX	1-2 & 3-4 SHORT OPEN

+5VDUAL

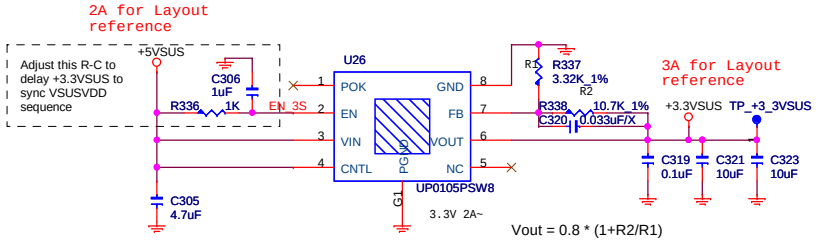


VCC_RTC

CLEAR_CMOS	FUNCTION
* 1 - 2	NORMAL
2 - 3	ENABLE

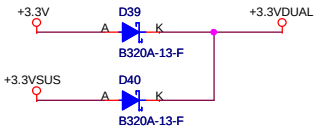


+3.3VSUS

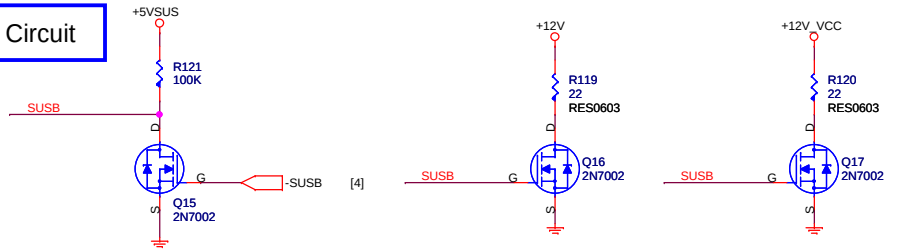


Iout Max = 2A

+3.3VDUAL



Discharge Circuit



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Title	ATX Power Connector	
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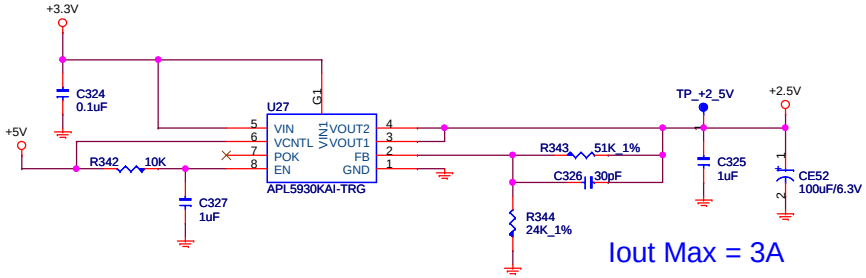
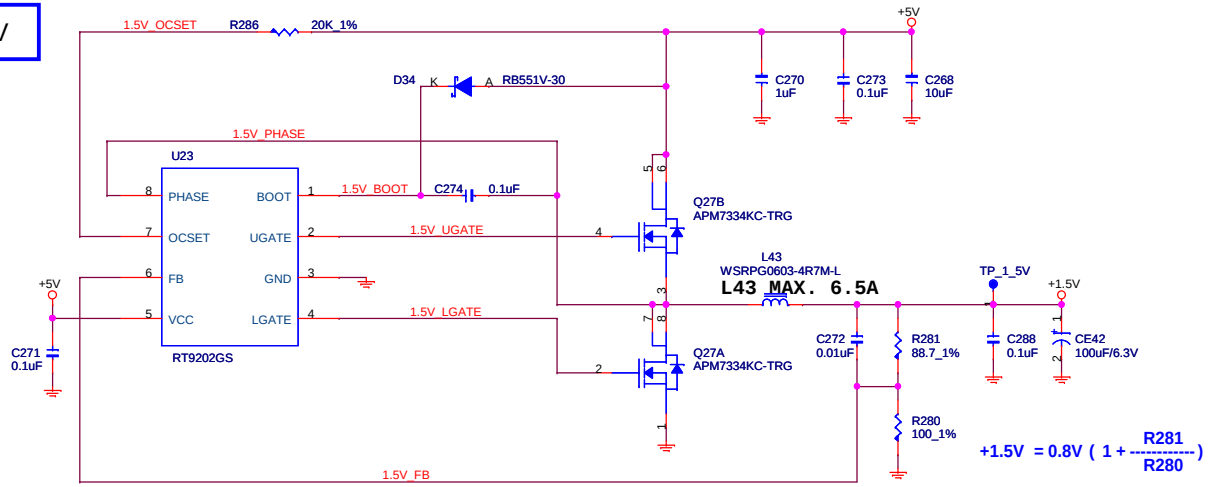
+2.5V



For SN75DP120 +2.5V

Iout Max = 3A

+1.5V



For Mini-PCIe Slot +1.5V

$$+1.5V = 0.8V \left(1 + \frac{R281}{R280}\right)$$

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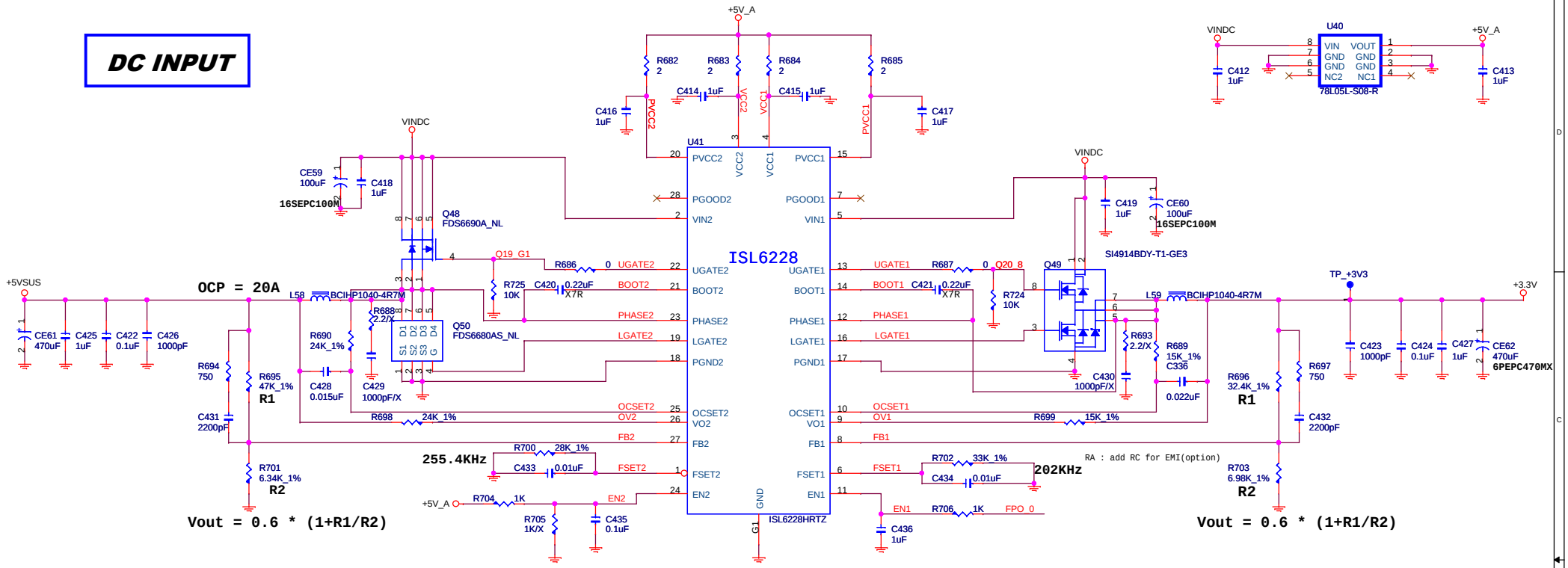
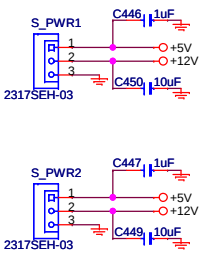
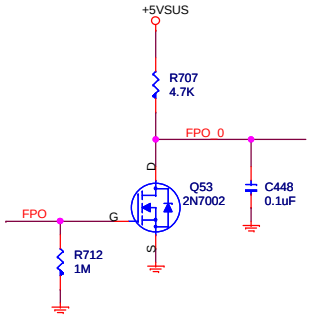
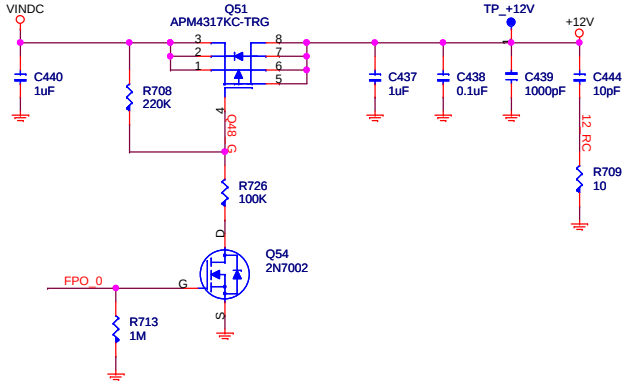
DC INPUT

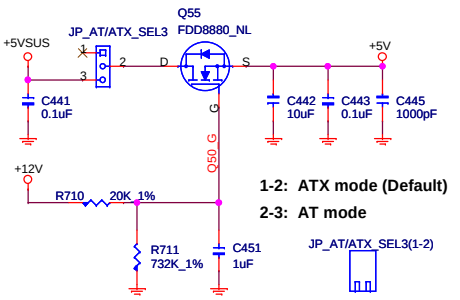


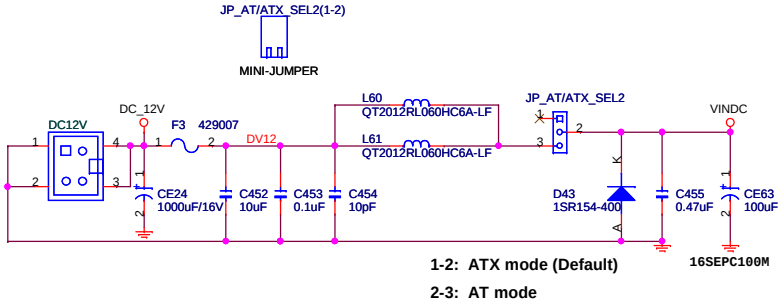
EXT SATA POWER

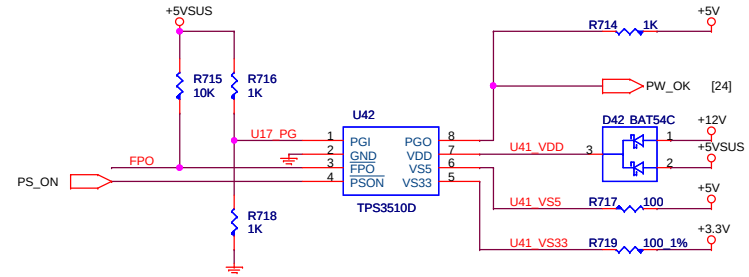


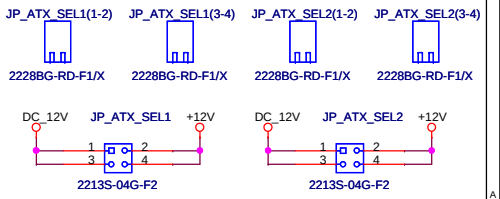












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Title: DC-In 12V/ AT_ATX		
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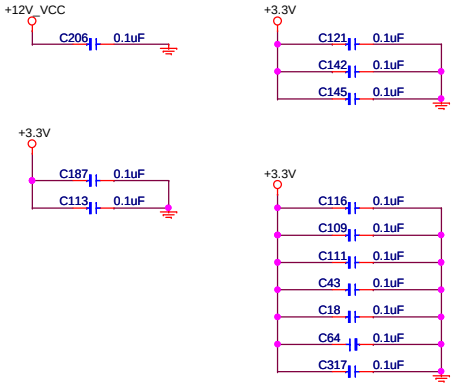
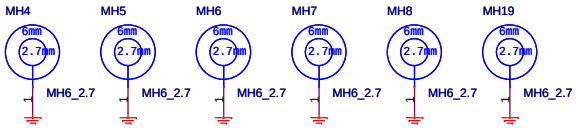
For EMI

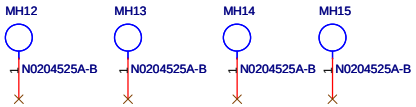


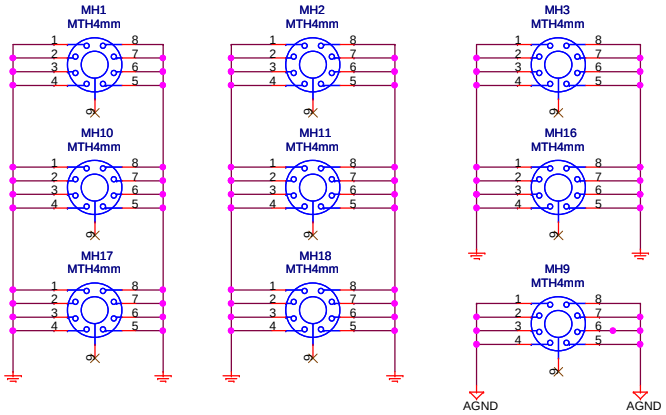
FIDUCIAL MARK

FOR COM EXPRESS MODULE



FOR Mini-PCIE MODULE





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Title: **Mounting Holes**

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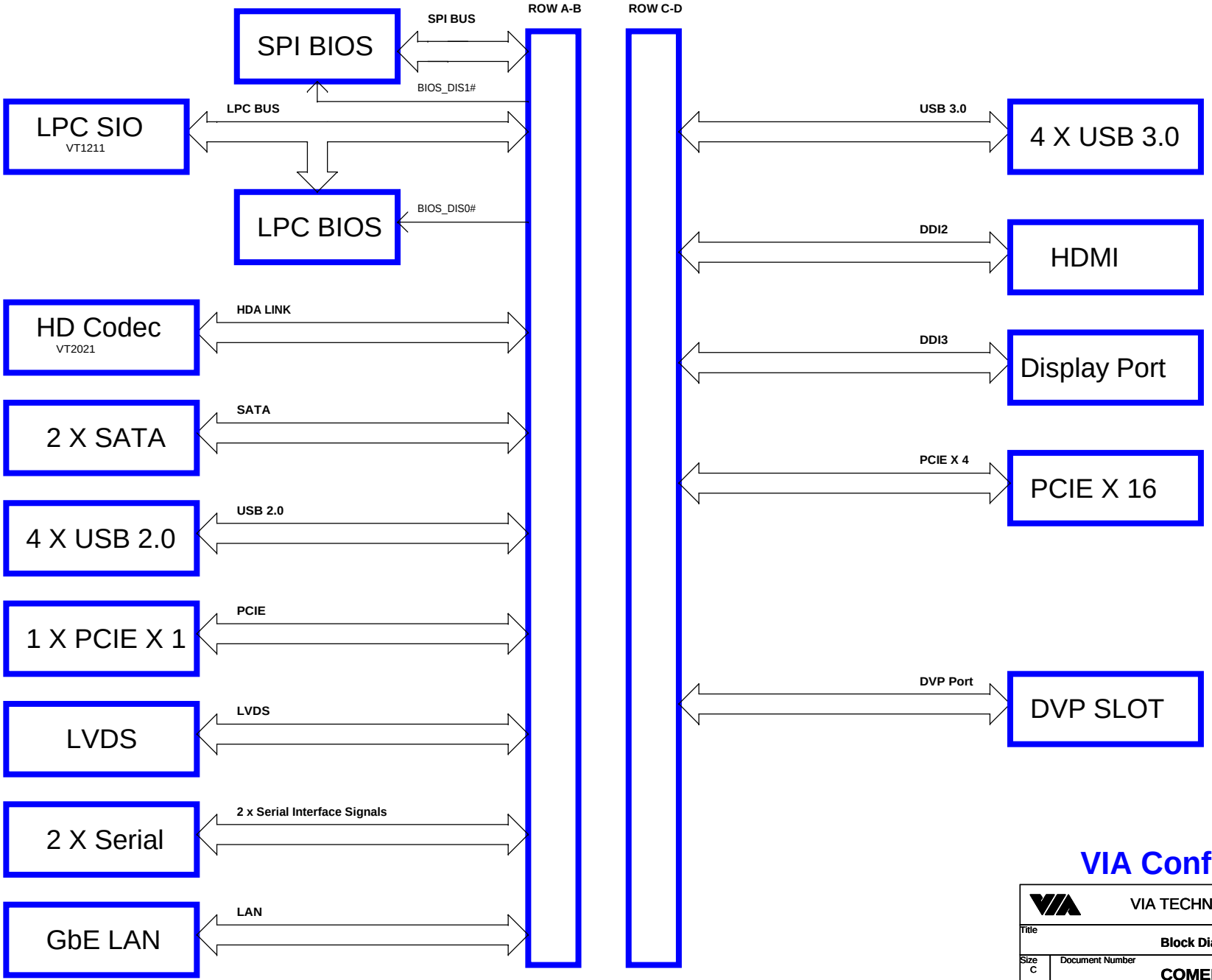
COMEBD2 Block Diagram



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Title: Block Diagram		
Size: C	Document Number: COMEBD2	Rev: A
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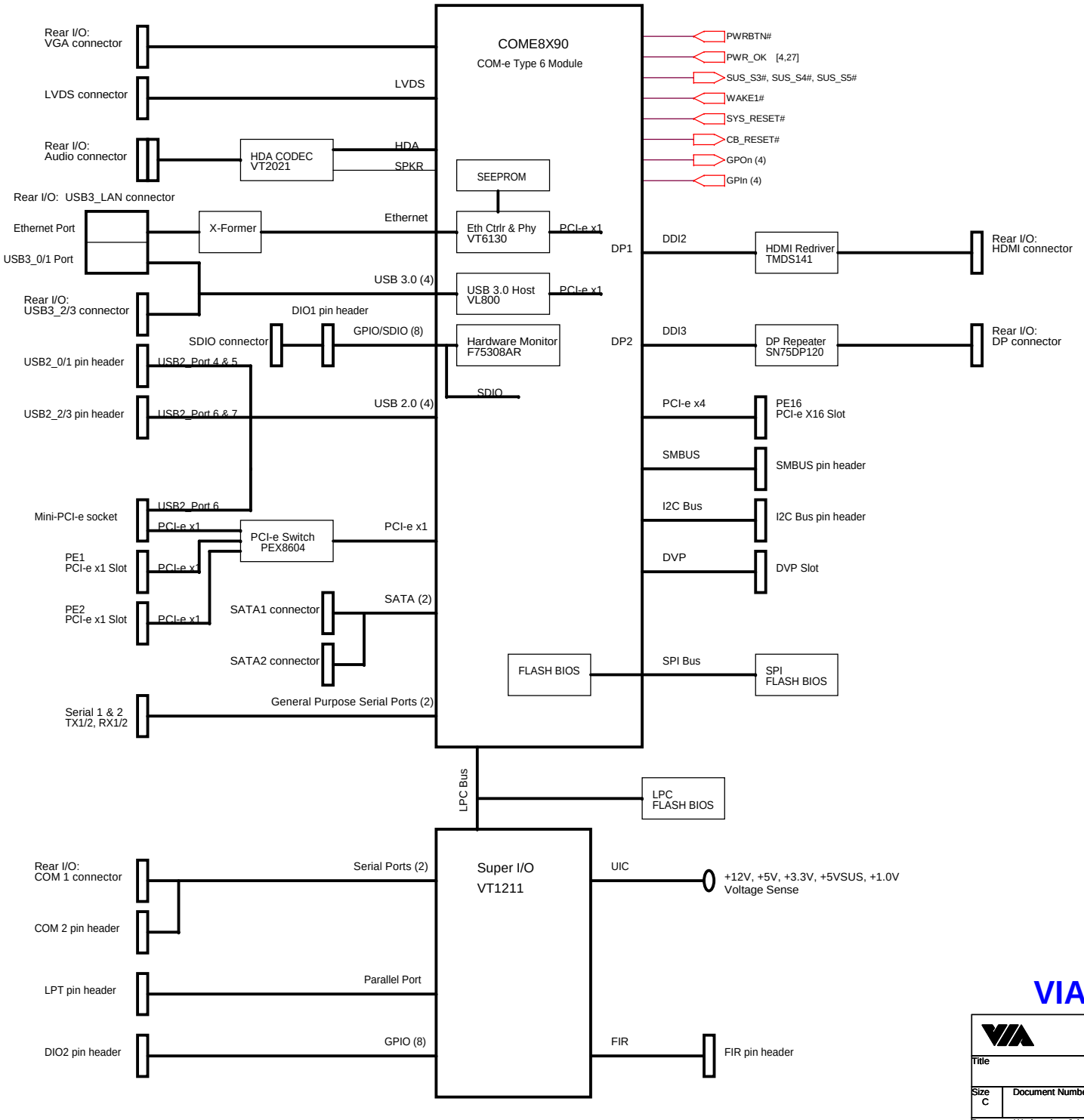

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Title: System Block Diagram

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COMEDB2

Revision A

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Title: COVER SHEET		
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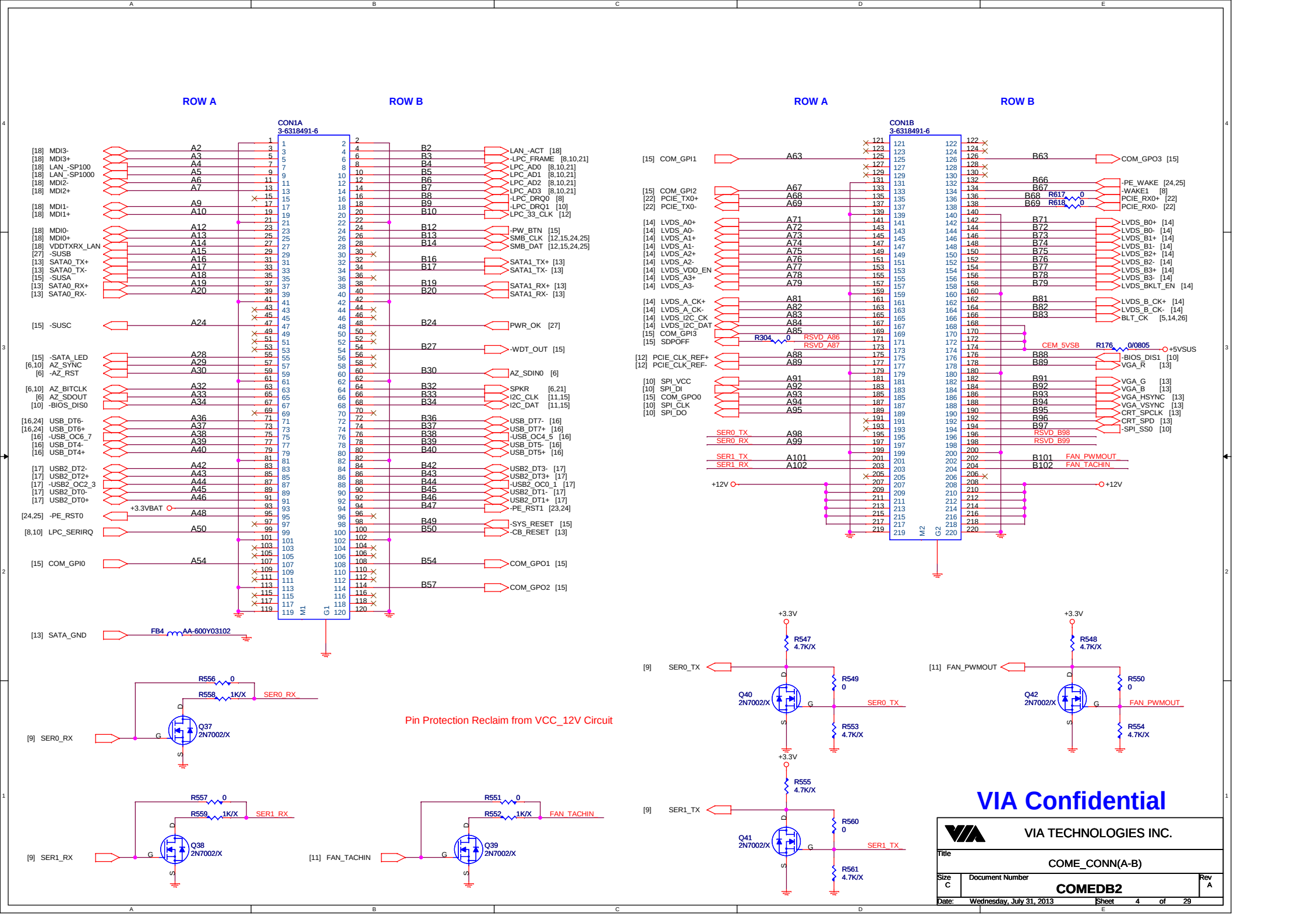
ROW A
ROW B
CON1A
3-6318491-6
[18] MDI3-
[18] MDI3+
[18] LAN_-SP100
[18] LAN_-SP1000
[18] MDI2-
[18] MDI2+
[18] MDI1-
[18] MDI1+
[18] MDI0-
[18] MDI0+
[18] VDDTXRX_LAN
[27] -SUSB
[13] SATA0_TX+
[13] SATA0_TX-
[15] -SUSA
[13] SATA0_RX+
[13] SATA0_RX-
[15] -SUSC
[15] -SATA_LED
[6,10] AZ_SYNC
[6] -AZ_RST
[6,10] AZ_BITCLK
[6] AZ_SDOUT
[10] -BIOS_DIS0
[16,24] USB_DT6-
[16,24] USB_DT6+
[16] -USB_OC6_7
[16] USB_DT4-
[16] USB_DT4+
[17] USB2_DT2-
[17] USB2_DT2+
[17] -USB2_OC2_3
[17] USB2_DT0-
[17] USB2_DT0+
+3.3VBAT
[24,25] -PE_RST0
[8,10] LPC_SERIRQ
[15] COM_GPI0
LAN_-ACT [18]
-LPC_FRAME [8,10,21]
LPC_AD0 [8,10,21]
LPC_AD1 [8,10,21]
LPC_AD2 [8,10,21]
LPC_AD3 [8,10,21]
-LPC_DRQ0 [8]
-LPC_DRQ1 [10]
LPC_33_CLK [12]
-PW_BTN [15]
SMB_CLK [12,15,24,25]
SMB_DAT [12,15,24,25]
SATA1_TX+ [13]
SATA1_TX- [13]
SATA1_RX+ [13]
SATA1_RX- [13]
PWR_OK [27]
-WDT_OUT [15]
AZ_SDIN0 [6]
SPKR [6,21]
I2C_CLK [11,15]
I2C_DAT [11,15]
USB_DT7- [16]
USB_DT7+ [16]
-USB_OC4_5 [16]
USB_DT5- [16]
USB_DT5+ [16]
USB2_DT3- [17]
USB2_DT3+ [17]
-USB2_OC0_1 [17]
USB2_DT1- [17]
USB2_DT1+ [17]
-PE_RST1 [23,24]
-SYS_RESET [15]
-CB_RESET [13]
COM_GPO1 [15]
COM_GPO2 [15]
[13] SATA_GND
FB4
AA-600Y03102
R556 0
R558 1K/X
SER0_RX
Q37
2N7002/X
[9] SER0_RX
R557 0
R559 1K/X
SER1_RX
Q38
2N7002/X
[9] SER1_RX
R551 0
R552 1K/X
FAN_TACHIN
Q39
2N7002/X
[11] FAN_TACHIN
Pin Protection Reclaim from VCC_12V Circuit
ROW A
ROW B
CON1B
3-6318491-6
[15] COM_GPI1
[15] COM_GPI2
[22] PCIE_TX0+
[22] PCIE_TX0-
[14] LVDS_A0+
[14] LVDS_A0-
[14] LVDS_A1+
[14] LVDS_A1-
[14] LVDS_A2+
[14] LVDS_A2-
[14] LVDS_VDD_EN
[14] LVDS_A3+
[14] LVDS_A3-
[14] LVDS_A_CK+
[14] LVDS_A_CK-
[14] LVDS_I2C_CK
[14] LVDS_I2C_DAT
[15] COM_GPI3
[15] SDPOFF
[12] PCIE_CLK_REF+
[12] PCIE_CLK_REF-
[10] SPI_VCC
[10] SPI_DI
[15] COM_GPO0
[10] SPI_CLK
[10] SPI_DO
R304 0
RSVD_A86
RSVD_A87
SER0_TX
SER0_RX
SER1_TX
SER1_RX
+12V
COM_GPO3 [15]
-PE_WAKE [24,25]
-WAKE1 [8]
PCIE_RX0+ [22]
PCIE_RX0- [22]
R617 0
R618 0
LVDS_B0+ [14]
LVDS_B0- [14]
LVDS_B1+ [14]
LVDS_B1- [14]
LVDS_B2+ [14]
LVDS_B2- [14]
LVDS_B3+ [14]
LVDS_B3- [14]
LVDS_BKLT_EN [14]
LVDS_B_CK+ [14]
LVDS_B_CK- [14]
BLT_CK [5,14,26]
CEM_5VSB
R176 0/0805
+5VSUS
-BIOS_DIS1 [10]
VGA_R [13]
VGA_G [13]
VGA_B [13]
VGA_HSYNC [13]
VGA_VSYNC [13]
CRT_SPCLK [13]
CRT_SPD [13]
-SPI_SS0 [10]
RSVD_B98
RSVD_B99
FAN_PWMOUT
FAN_TACHIN
+12V
+3.3V
R547 4.7K/X
[9] SER0_TX
R549 0
Q40
2N7002/X
SER0_TX
R553 4.7K/X
+3.3V
R555 4.7K/X
[9] SER1_TX
R560 0
Q41
2N7002/X
SER1_TX
R561 4.7K/X
+3.3V
R548 4.7K/X
[11] FAN_PWMOUT
R550 0
Q42
2N7002/X
FAN_PWMOUT
R554 4.7K/X
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VIA TECHNOLOGIES INC.
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COME_CONN(A-B)
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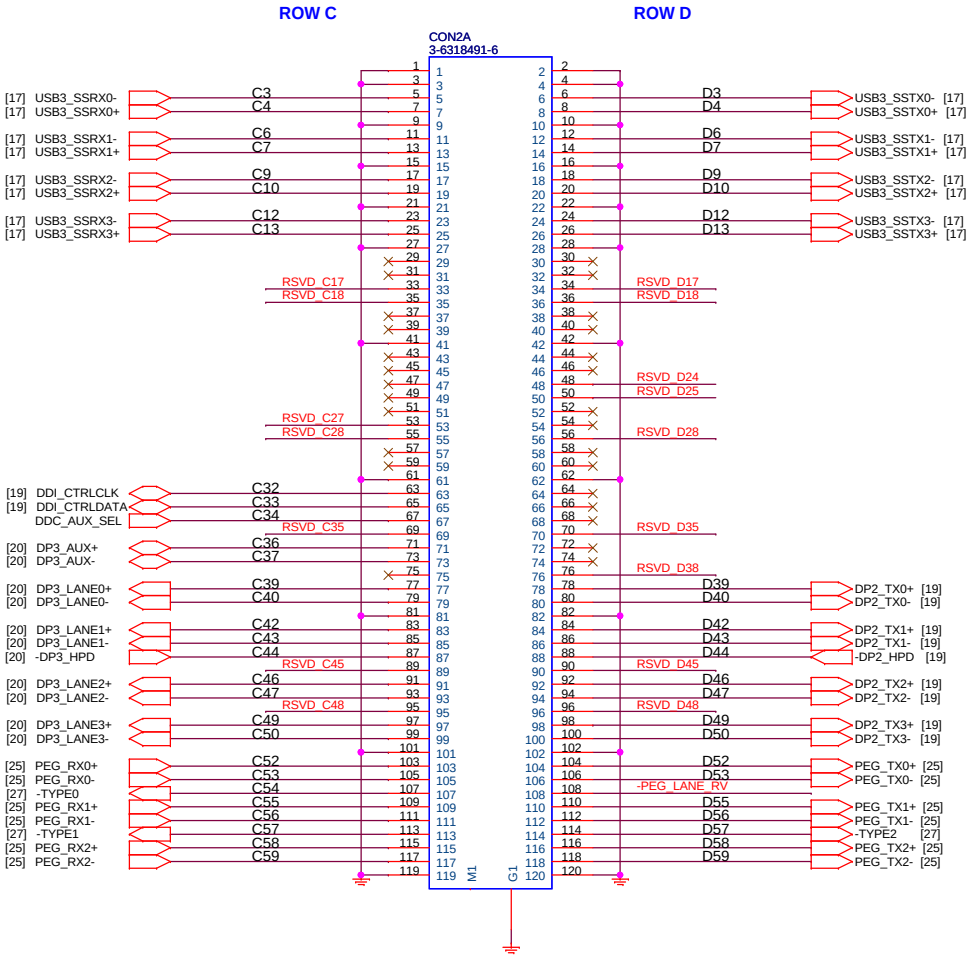
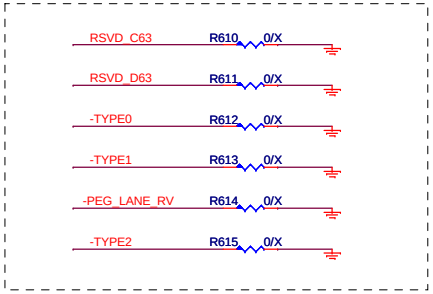


DDI Configuration:

DDI 1: NA
DDI 2: HDMI / DISPLAY PORT
DDI 3: DISPLAY PORT



Note: Reserved for PCIe SI Measurement

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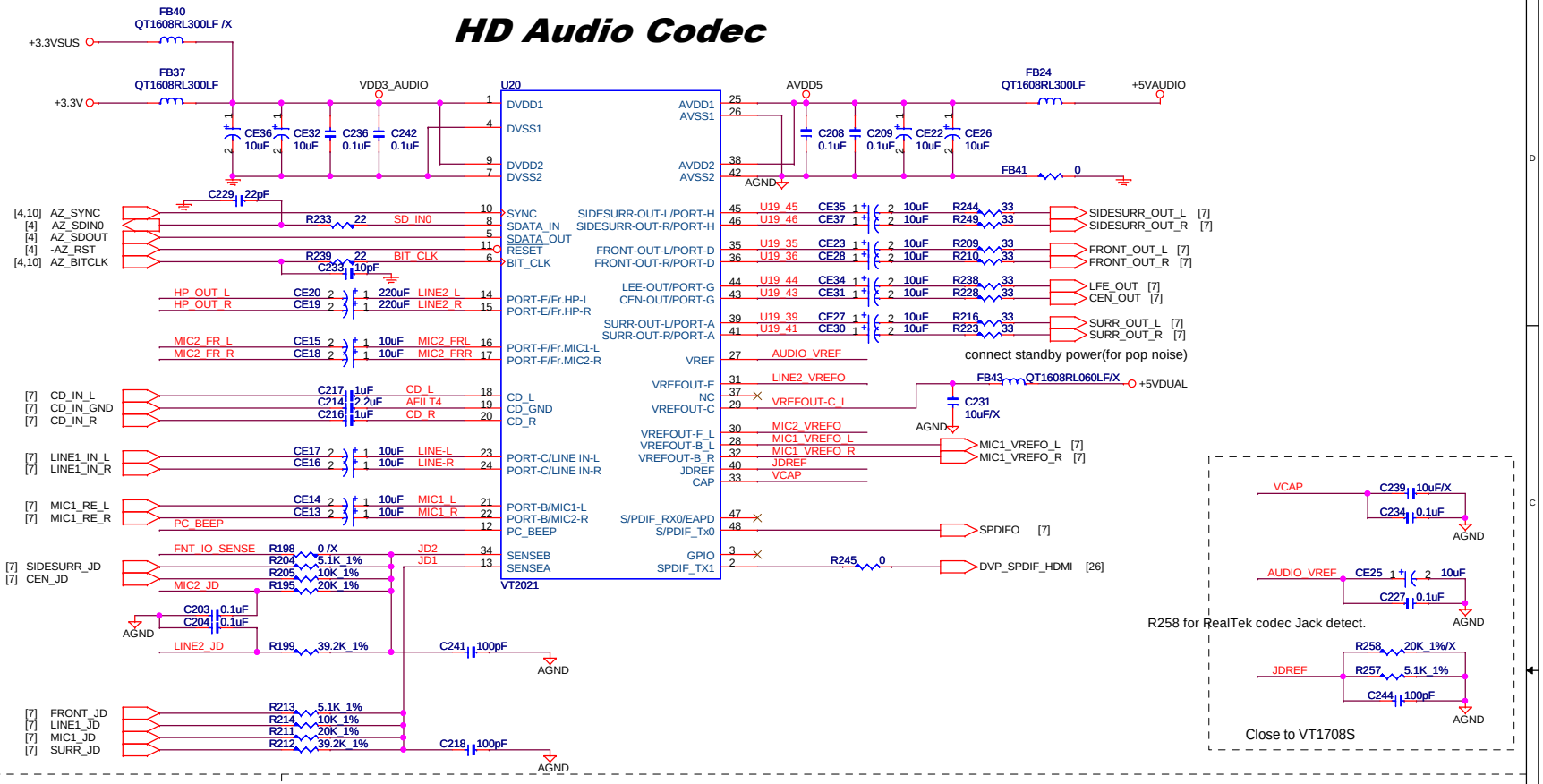
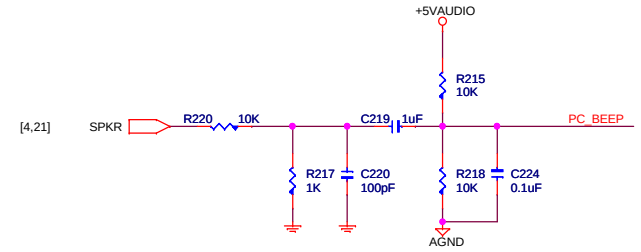
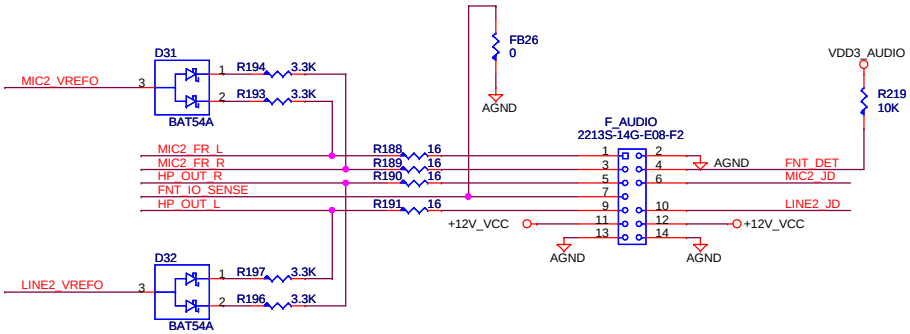
HD Audio Codec

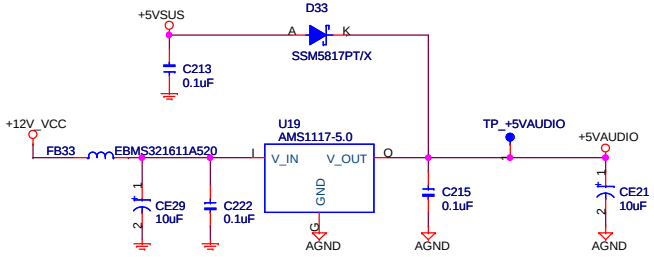


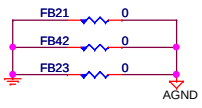


FRONT AUDIO



+5VAUDIO





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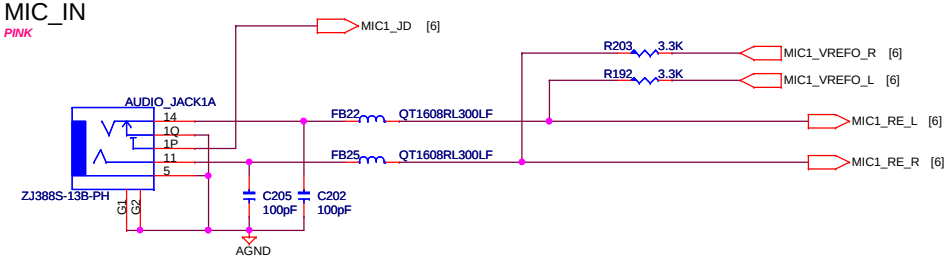
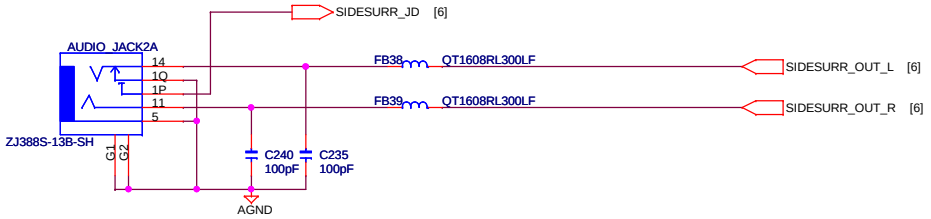
MIC_IN

PINK



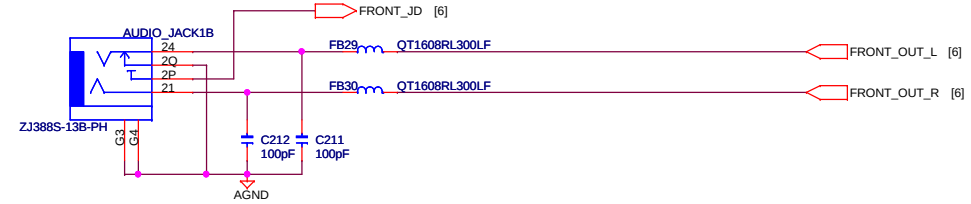
SIDESURR_OUT

GREY



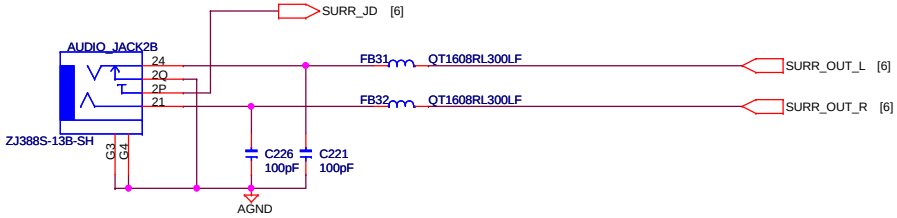
FRONT_OUT

GREEN



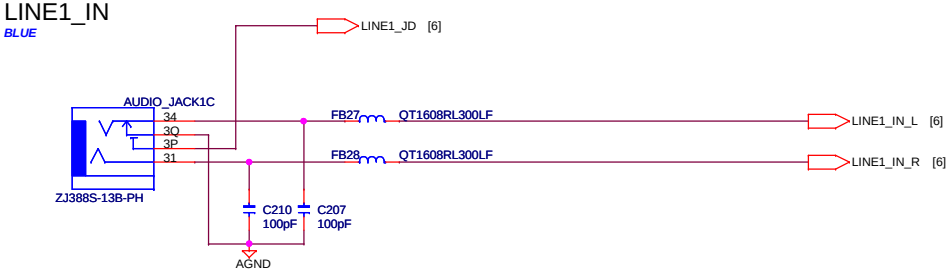
SURR_OUT

BLACK



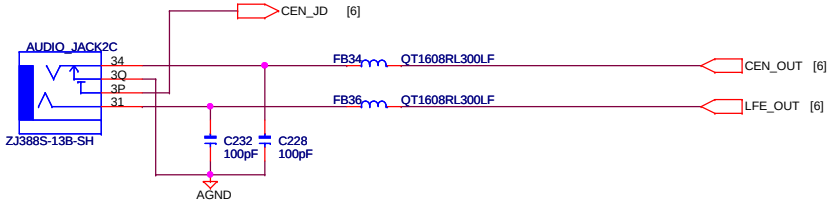
LINE1_IN

BLUE

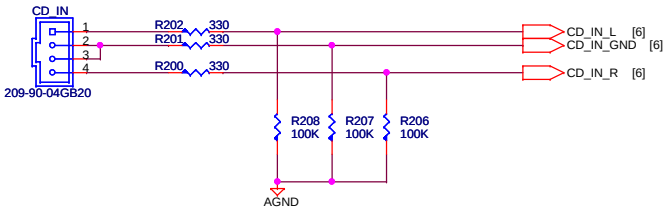


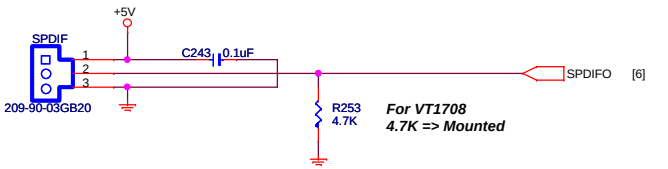
CENTER/LFE

ORANGE



CD_IN





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Title: AUDIO CONNECTORS		
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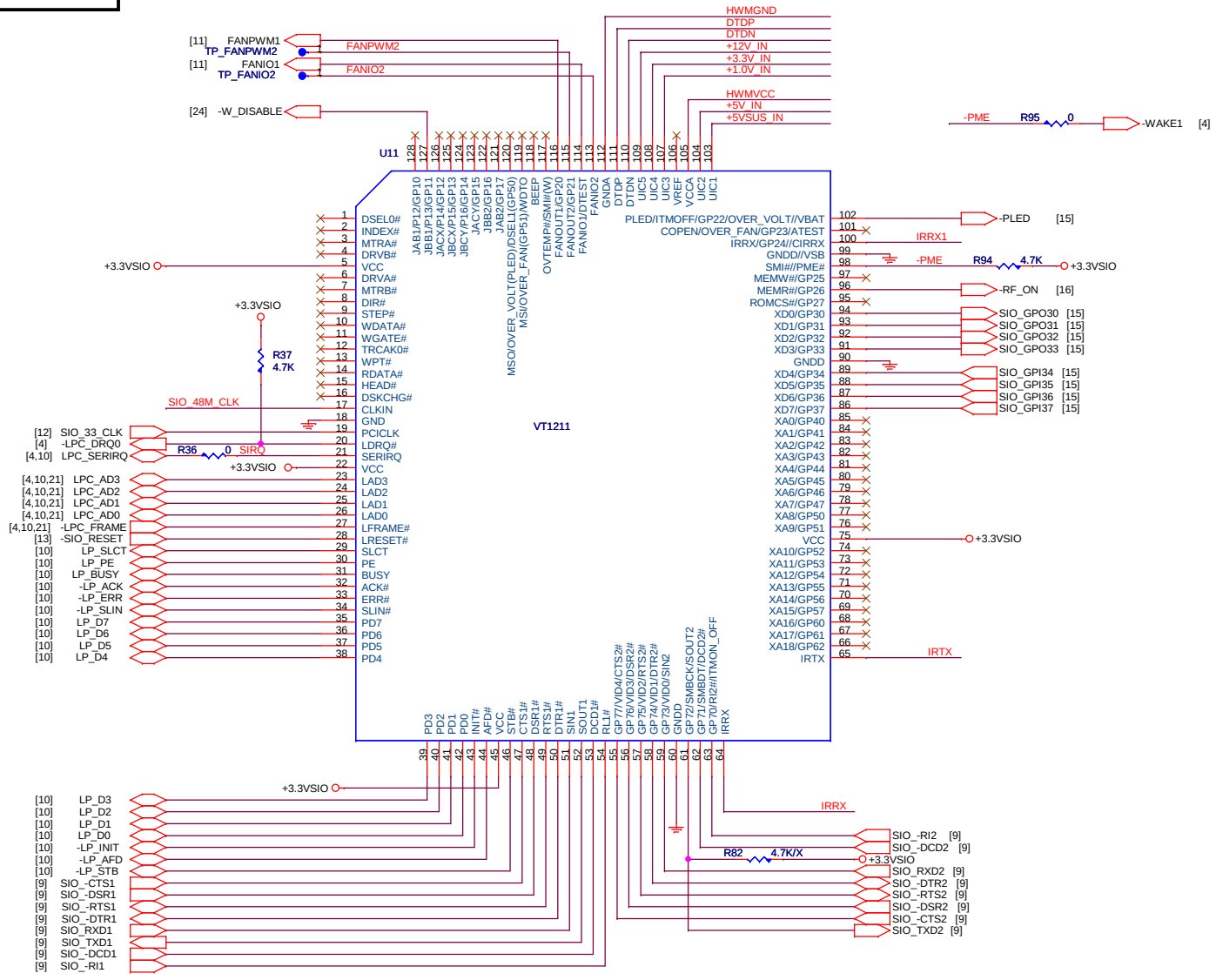
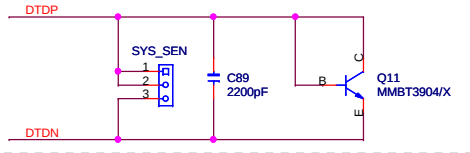
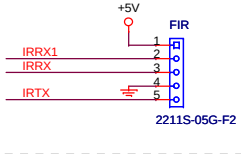
VT1211



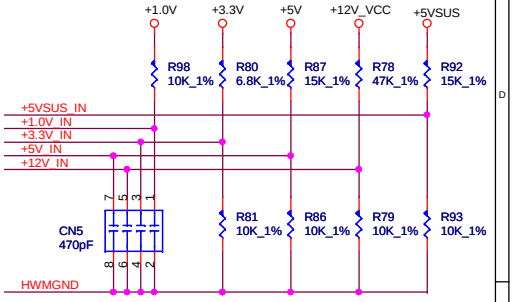
Thermal Sensor



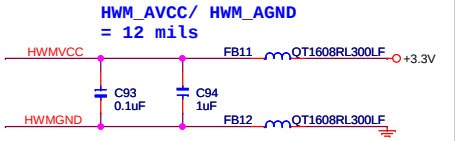
FIR

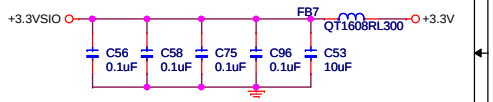


Voltage Sense

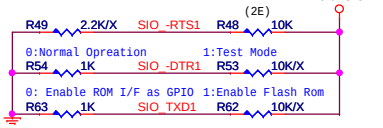


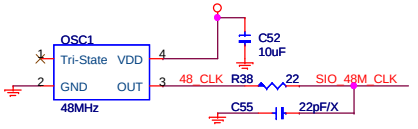
HWM_AVCC/ HWM_AGND = 12 mils





VT1211 Decoupling Caps.





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Title	VT1211 COM3/ COM4/ LPT/ HW monitor
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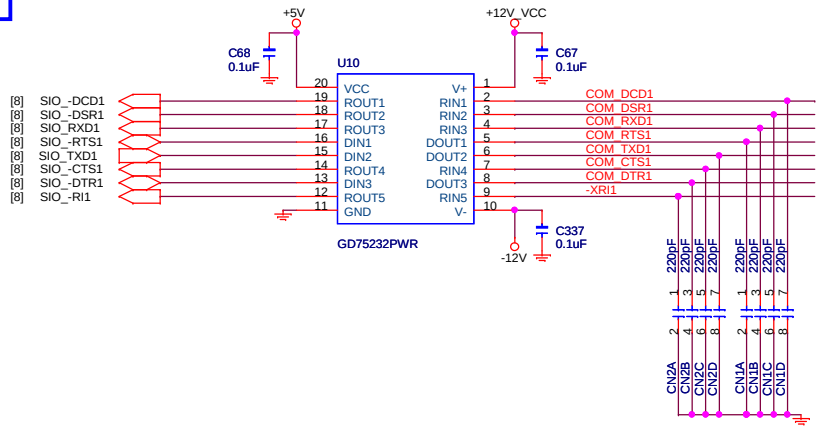
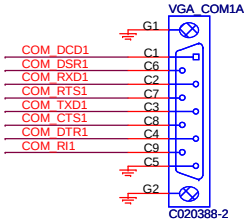
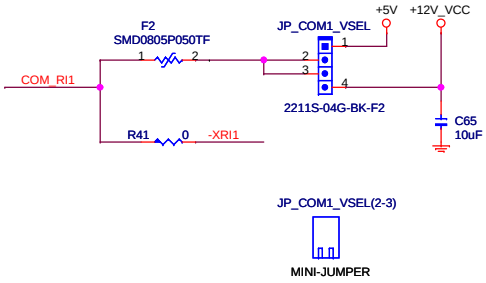
COM 1

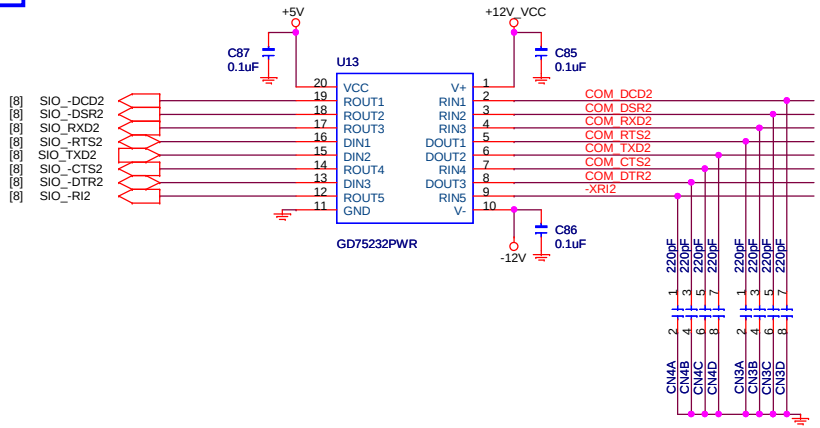


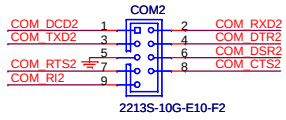


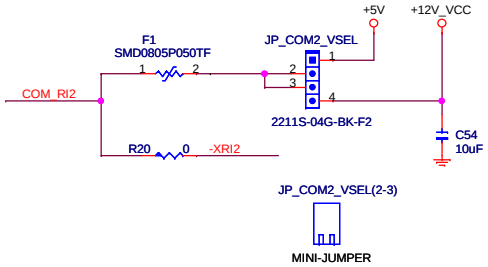


JP_COM1_VSEL	VOLTAGE
1-2	+5V
2-3	Normal *
3-4	+12V

COM 2

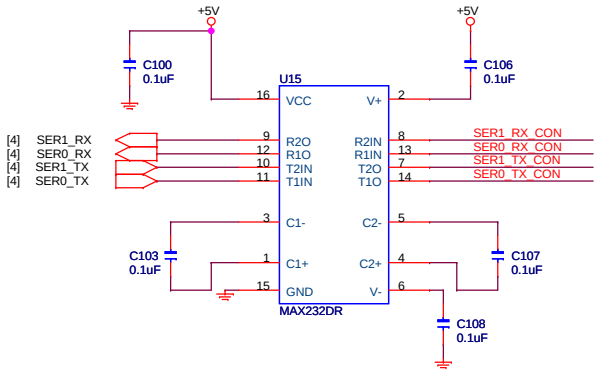


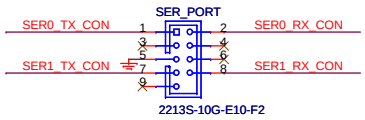




JP_COM2_VSEL	VOLTAGE
1-2	+5V
2-3	Normal *
3-4	+12V

General Purpose Serial Ports





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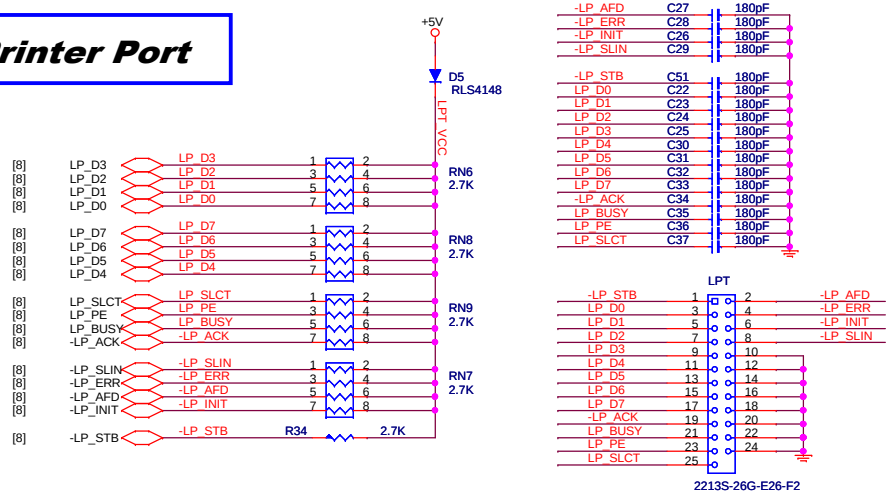
Printer Port

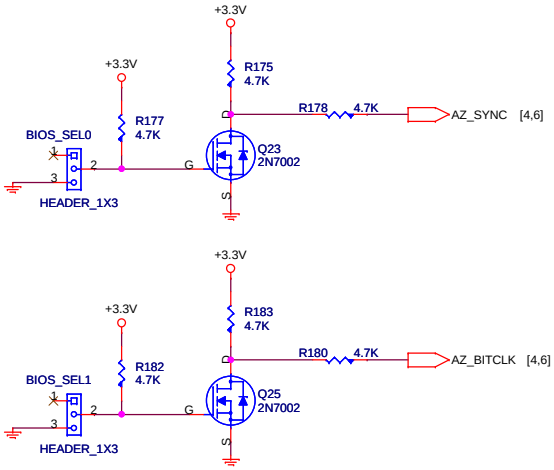


BIOS_SEL1(2-3) MINI-JUMPER

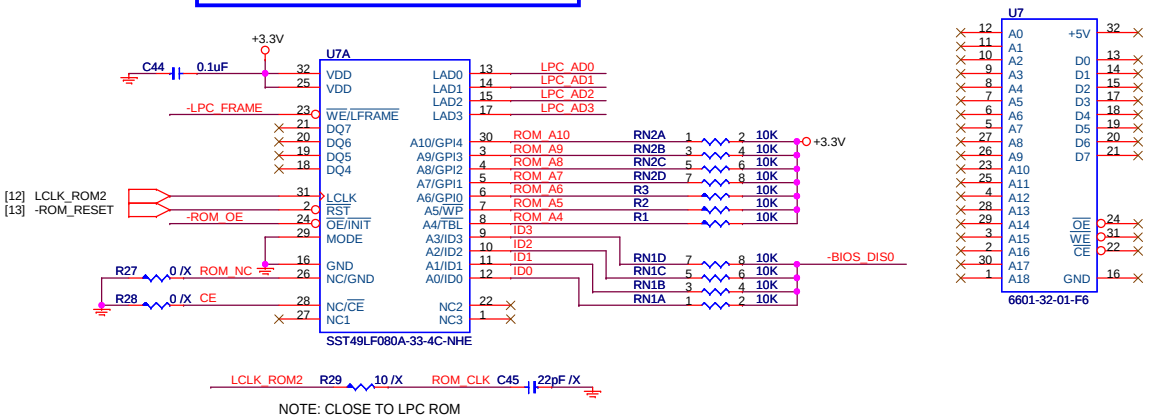
BIOS_SEL0(1-2) MINI-JUMPER

BIOS Type Selection Table

BIOS_Type	BIOS_SEL1 AZ_BITCLK	BIOS_SEL0 AZ_SYNC
SPI BIOS	2 - 3 *	1 - 2 *
LPC BIOS	1 - 2	2 - 3

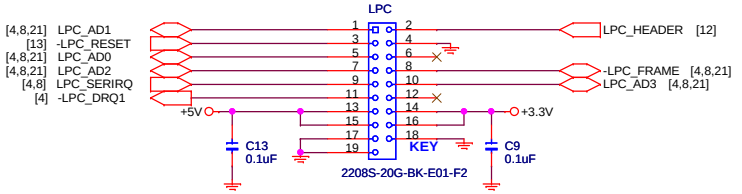


LPC FLASH ROM

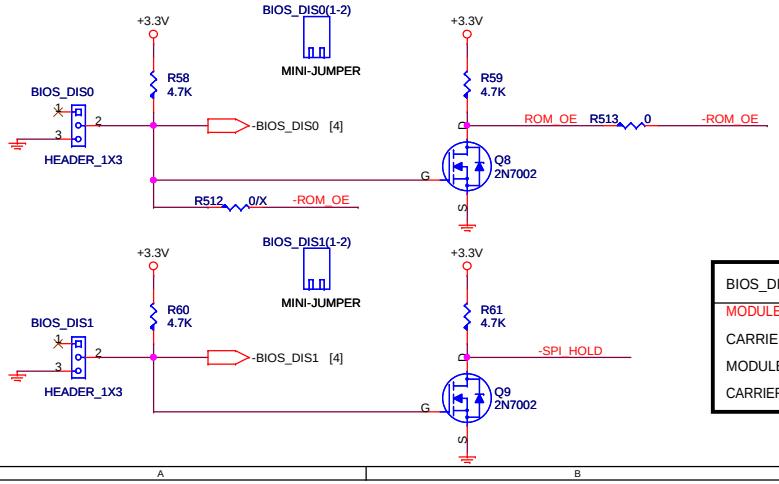


NOTE: CLOSE TO LPC ROM

LPC HEADER



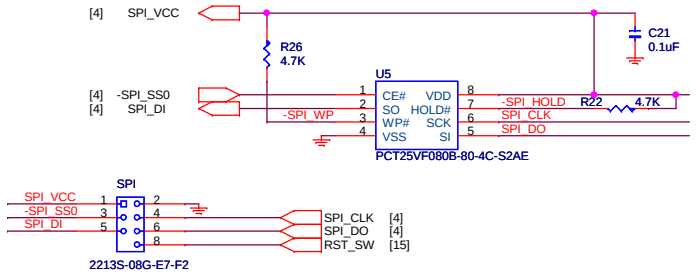
BIOS DISABLE



BIOS Selection Table

BIOS_DISABLE	BIOS_DIS1	BIOS_DIS0
MODULE SPI BIOS	1 - 2 *	1 - 2 *
CARRIER LPC BIOS	1 - 2	2 - 3
MODULE LPC BIOS	2 - 3	1 - 2
CARRIER SPI BIOS	2 - 3	2 - 3

SPI ROM



Pitch 2.54mm

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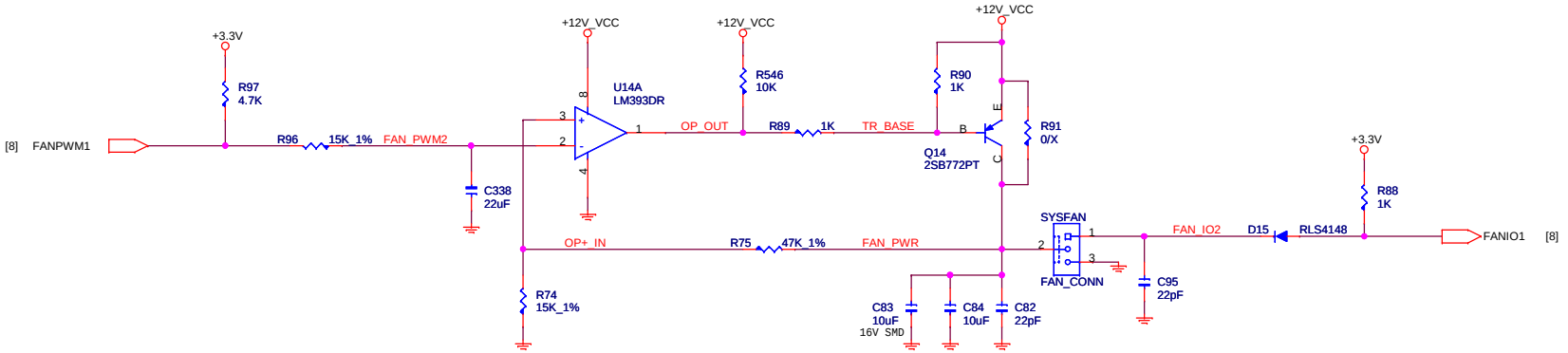
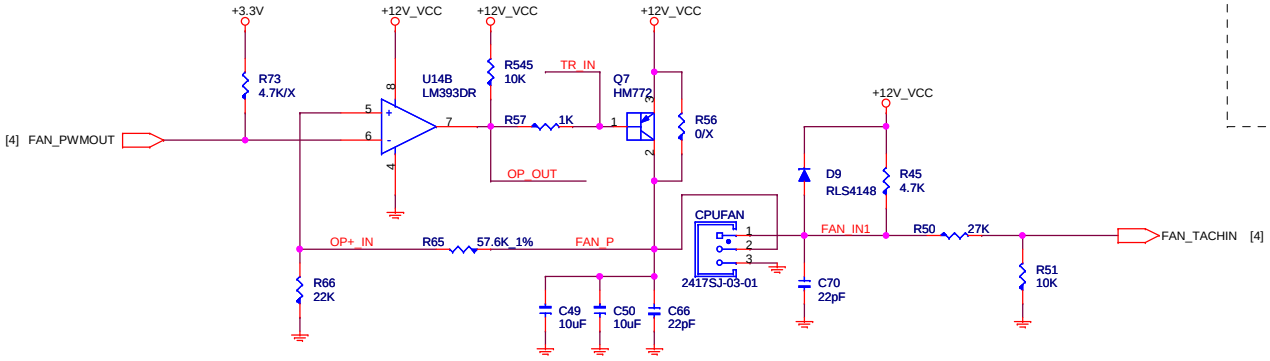
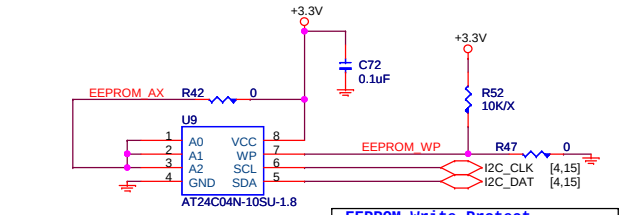
SYSTEM FAN



CPU FAN



EEPROM



Device Address = 0x57(0xAE)

EEPROM Write Protect	
GND	Normal Operation *
+3.3V	Write Protect

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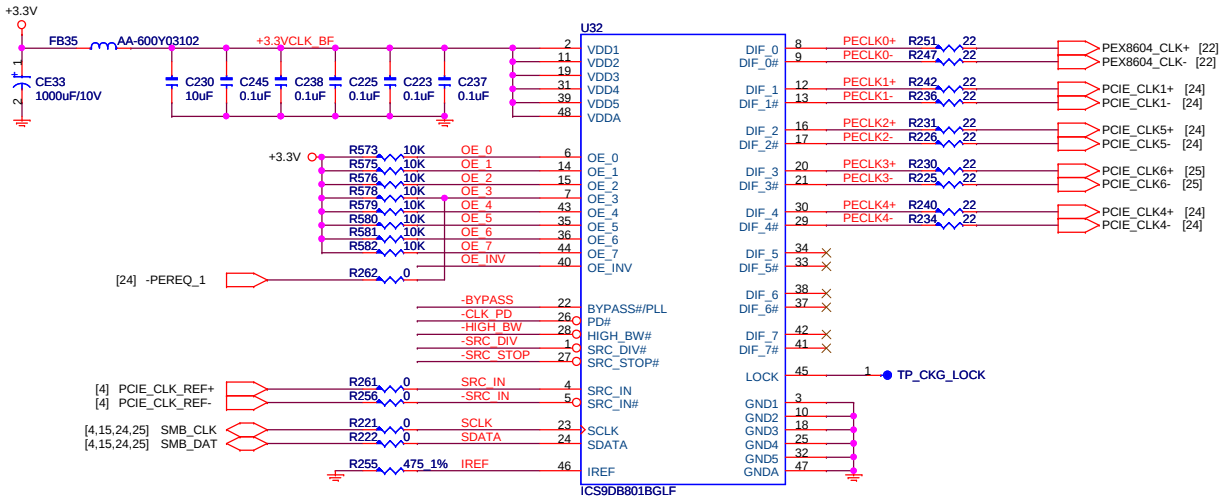
PCIE CLOCK BUFFER



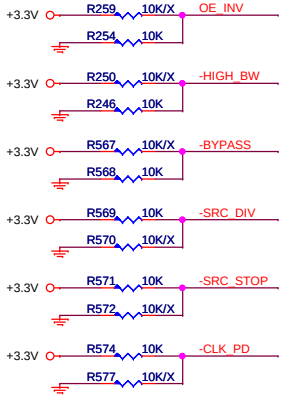
TO PEX8604

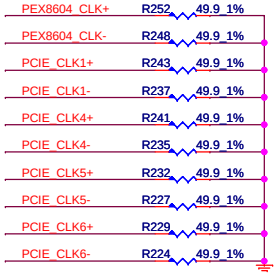
TO PE1 SLOT

TO PE2 SLOT

TO Mini PCI-e

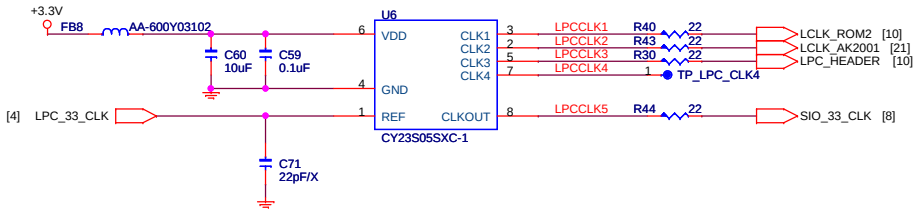
TO PE3 SLOT

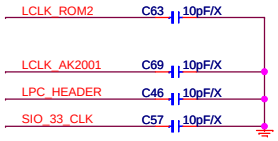




meet Zdif=49.9 ohm

LPC CLOCK BUFFER





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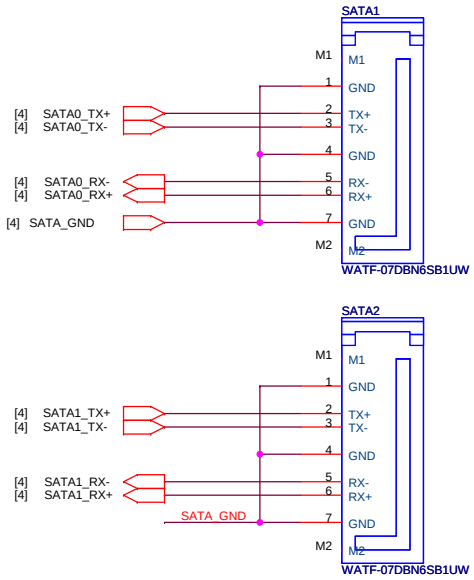
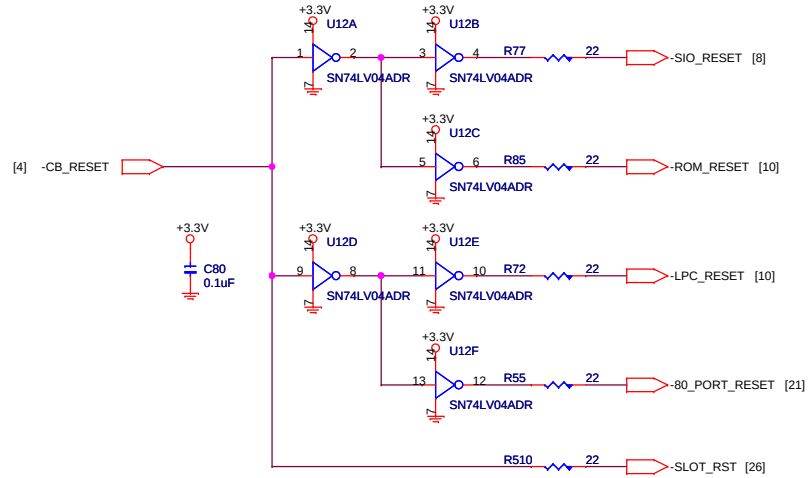
VIA TECHNOLOGIES INC.

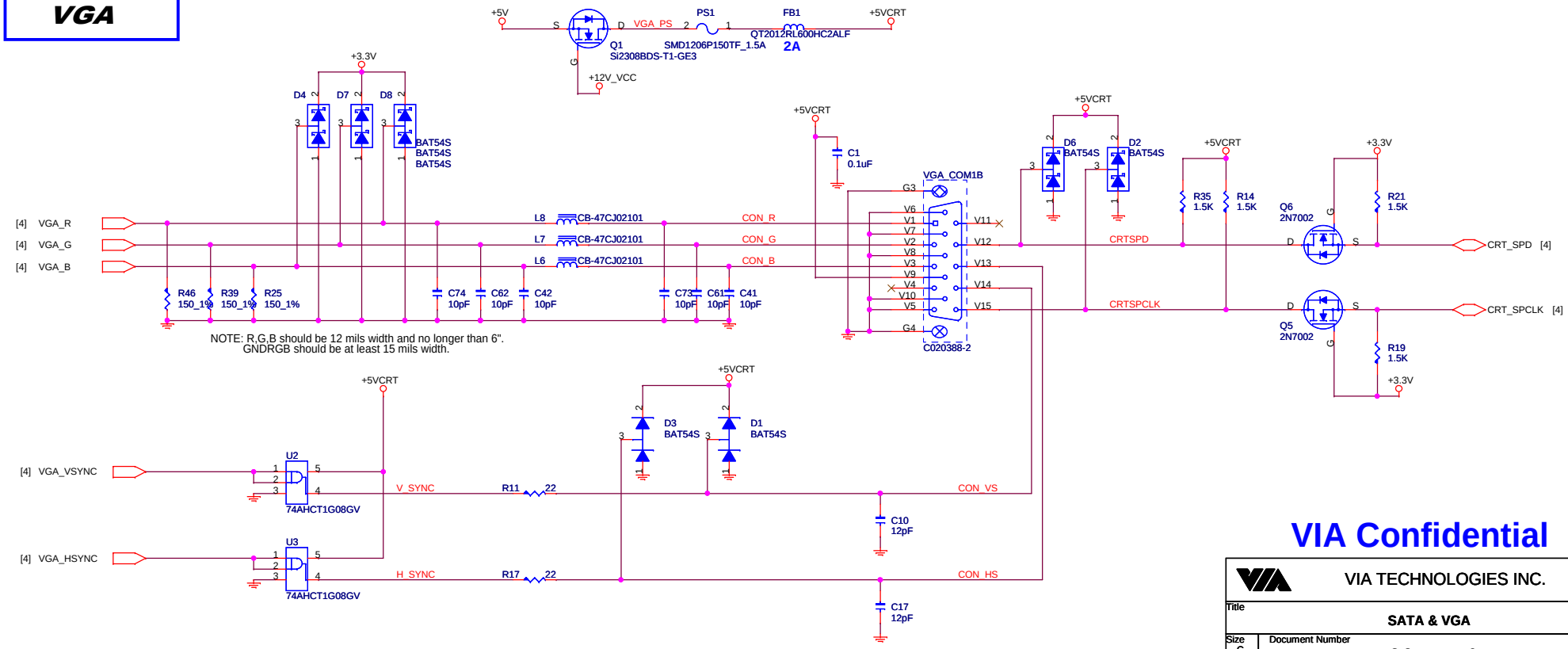
Title	PCIE / PCI Clock Buffer	
Size C	Document Number COMBED2	Rev A
Date: Wednesday, July 31, 2013	Sheet 12 of 29	

SATA





VGA



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Title	SATA & VGA
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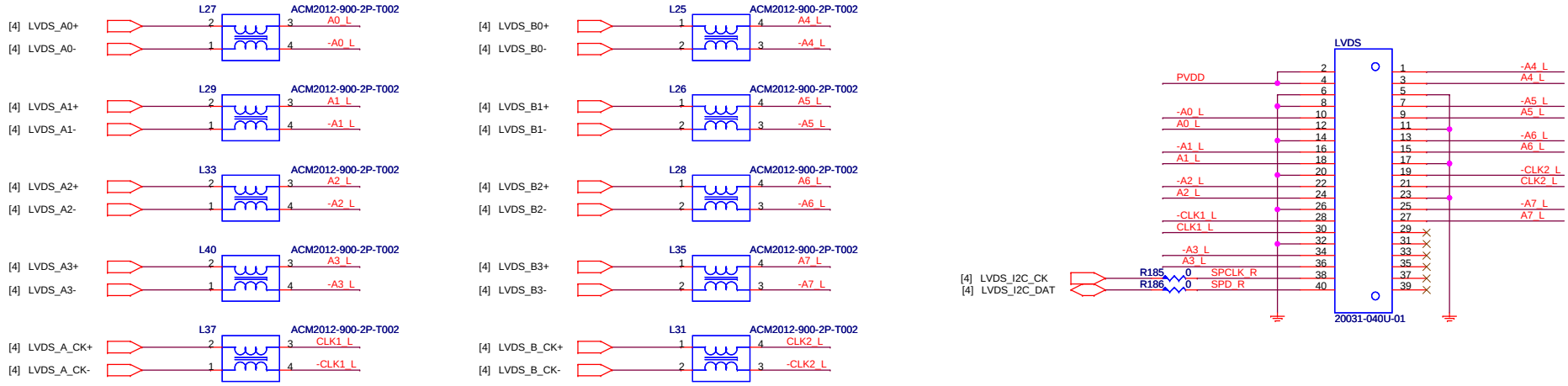
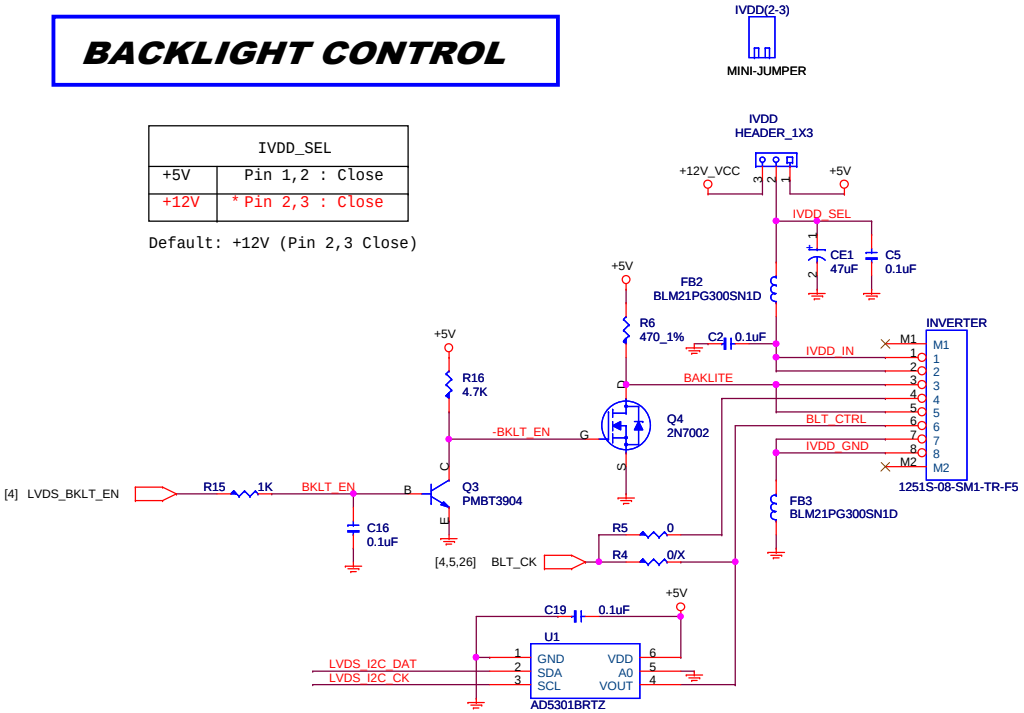
LVDS CONNECTOR



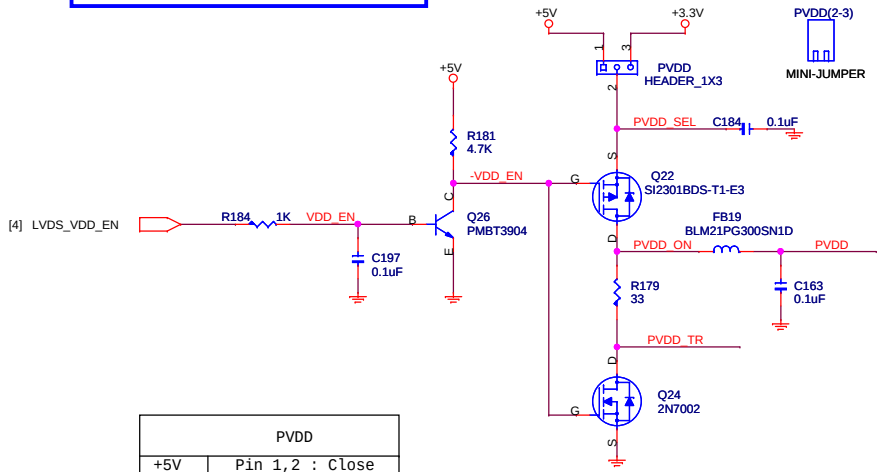
BACKLIGHT CONTROL

IVDD_SEL	
+5V	Pin 1,2 : Close
+12V	* Pin 2,3 : Close

Default: +12V (Pin 2,3 Close)



PANEL POWER



PVDD	
+5V	Pin 1,2 : Close
+3.3V	* Pin 2,3 : Close

Default: +3.3V (Pin 2,3 Close)

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VIA TECHNOLOGIES INC.

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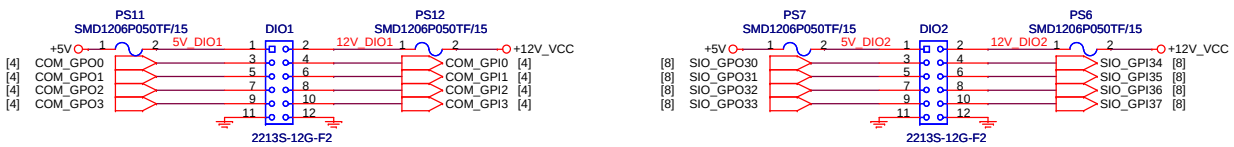
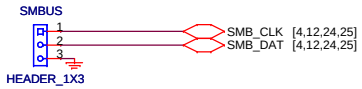
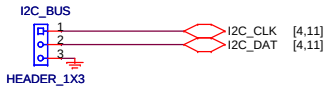
Digital I/O



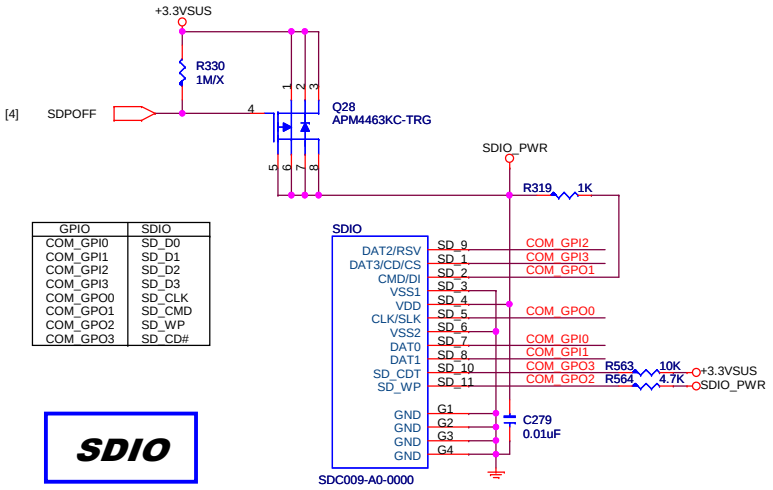
SMBUS



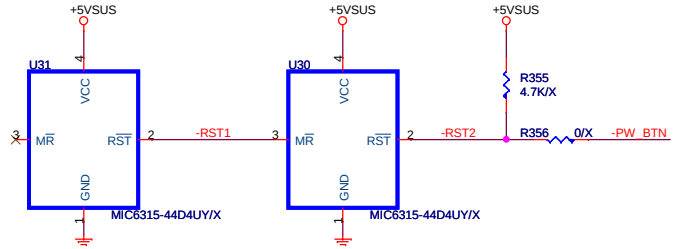
I2C_BUS



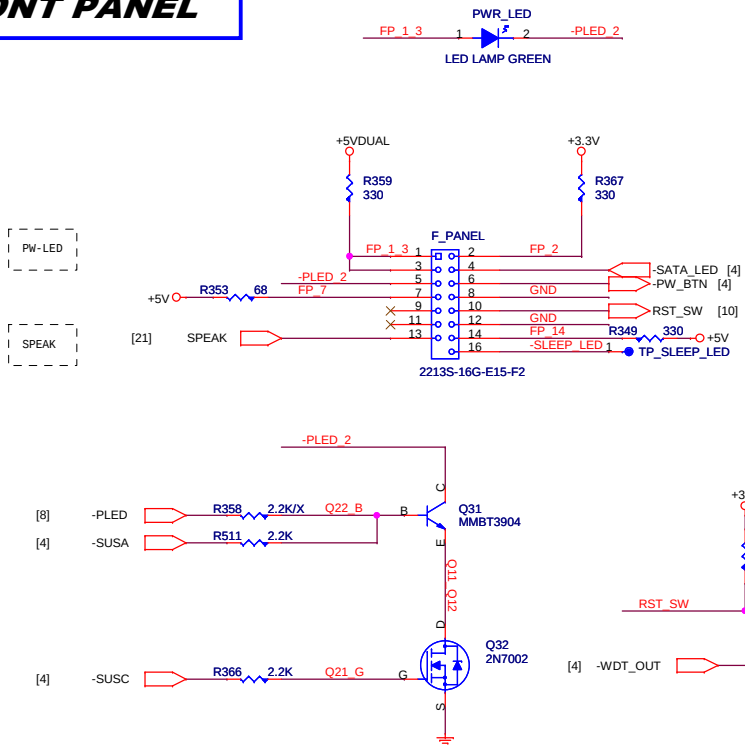
SDIO



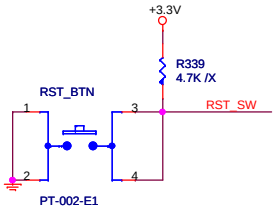
RESET_IC



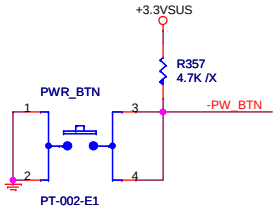
FRONT PANEL



RESET_BTN



PWRBTN



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VIA TECHNOLOGIES INC.		
Title: FPNL, DIO, SMBUS, I2C & MFX		
Size: C	Document Number: COMEBD2	Rev: A
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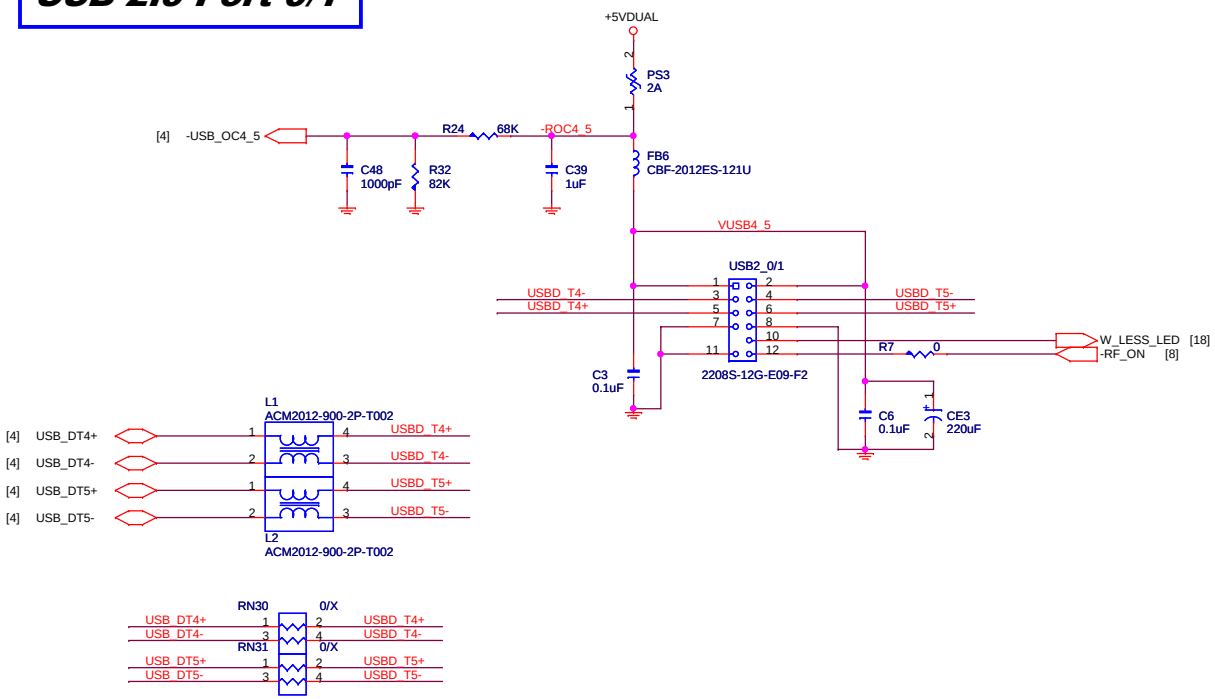
USB 2.0 Port 0/1



USB2 0/1

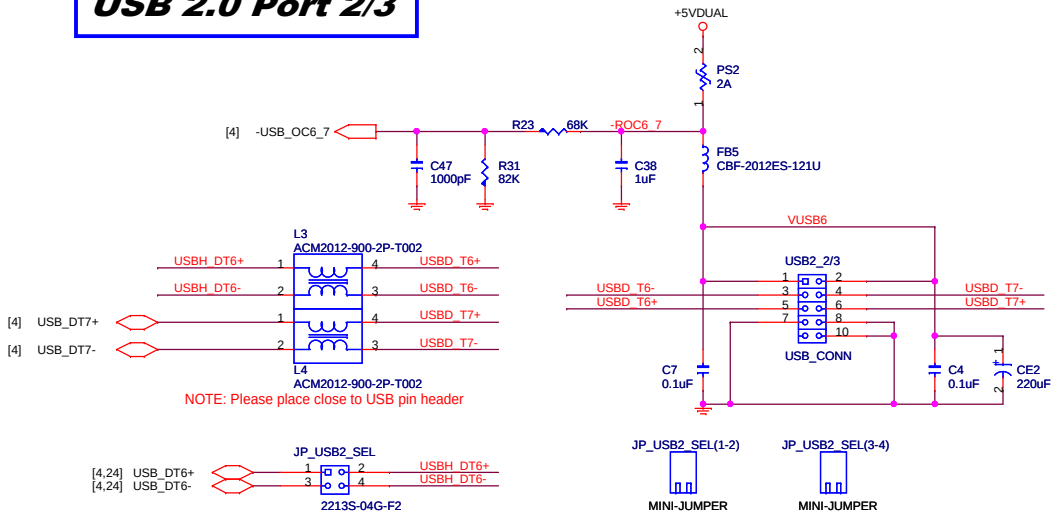
USBD_T5- , USBD_T5+ for VNT 6656

VNT

1.	VUSB4(+5VDUAL)
2.	USBD_T5-
3.	USBD_T5+
4.	GND
5.	W_LESS_LED Active High
6.	-RF_ON Active Low

VNT Connector: 1x6 2.54mm

USB 2.0 Port 2/3



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Title	USB 2.0_4 Ports	
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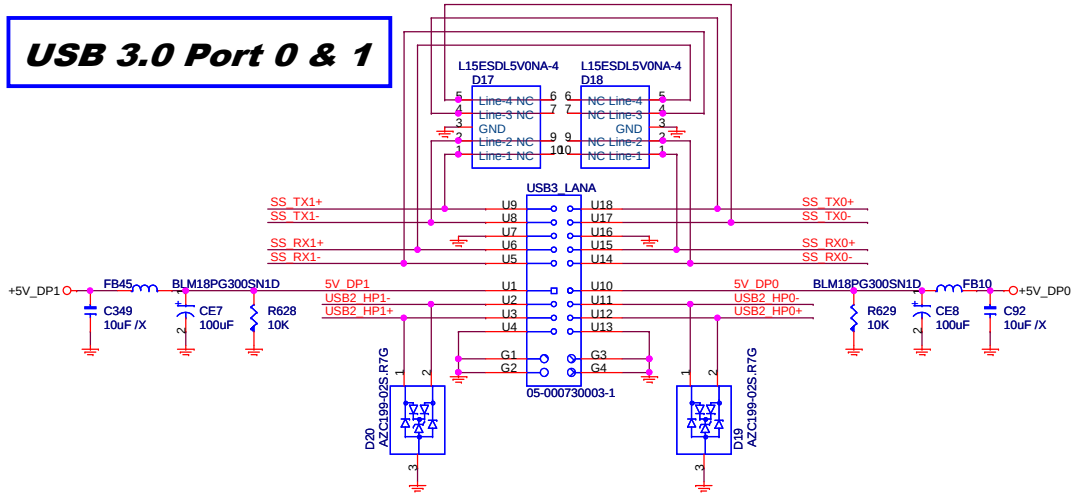
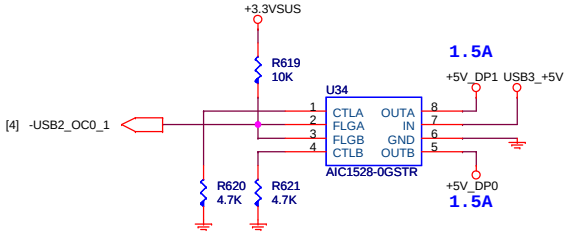
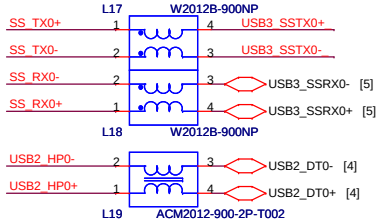
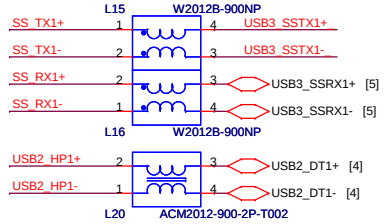
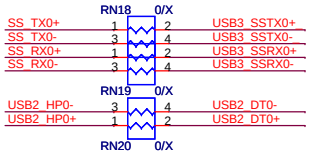
USB 3.0 Port 0 & 1



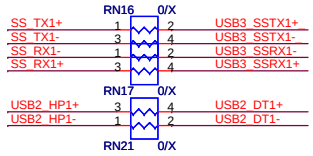








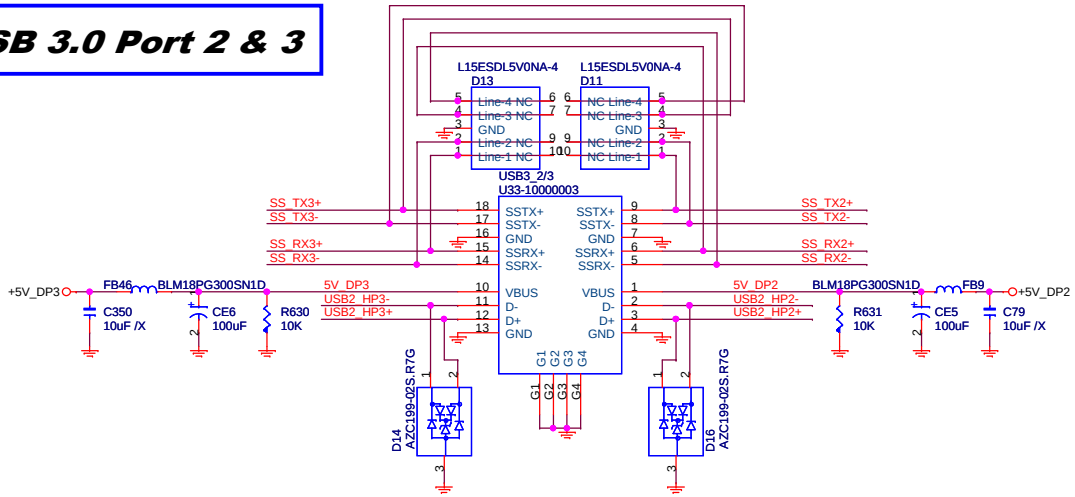
Co-Layout

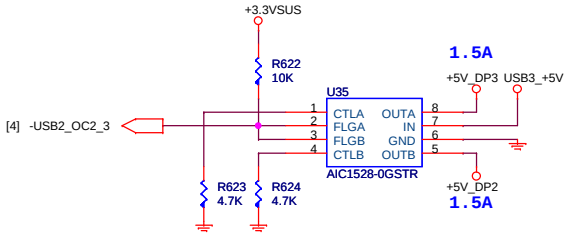


Co-Layout

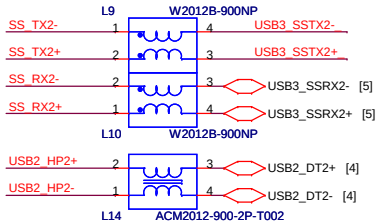
Note: Please place those parts close to USB Connector

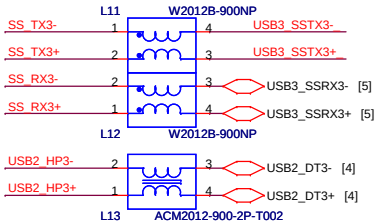
USB 3.0 Port 2 & 3

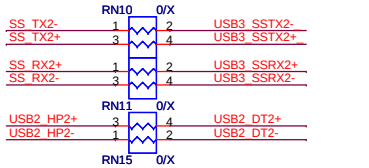




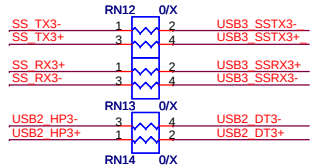
Note: Please place those parts close to USB Connector



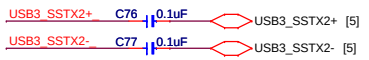




Co-Layout



Co-Layout



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VIA TECHNOLOGIES INC.		
Title: USB 3.0_4 Ports		
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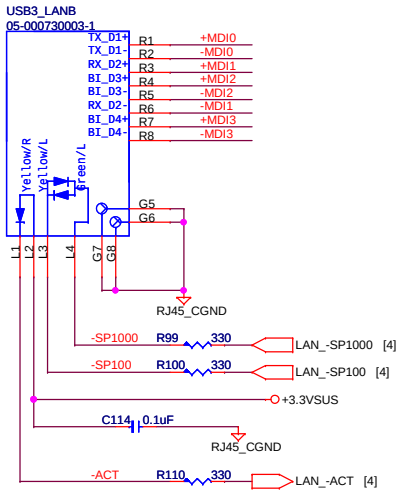
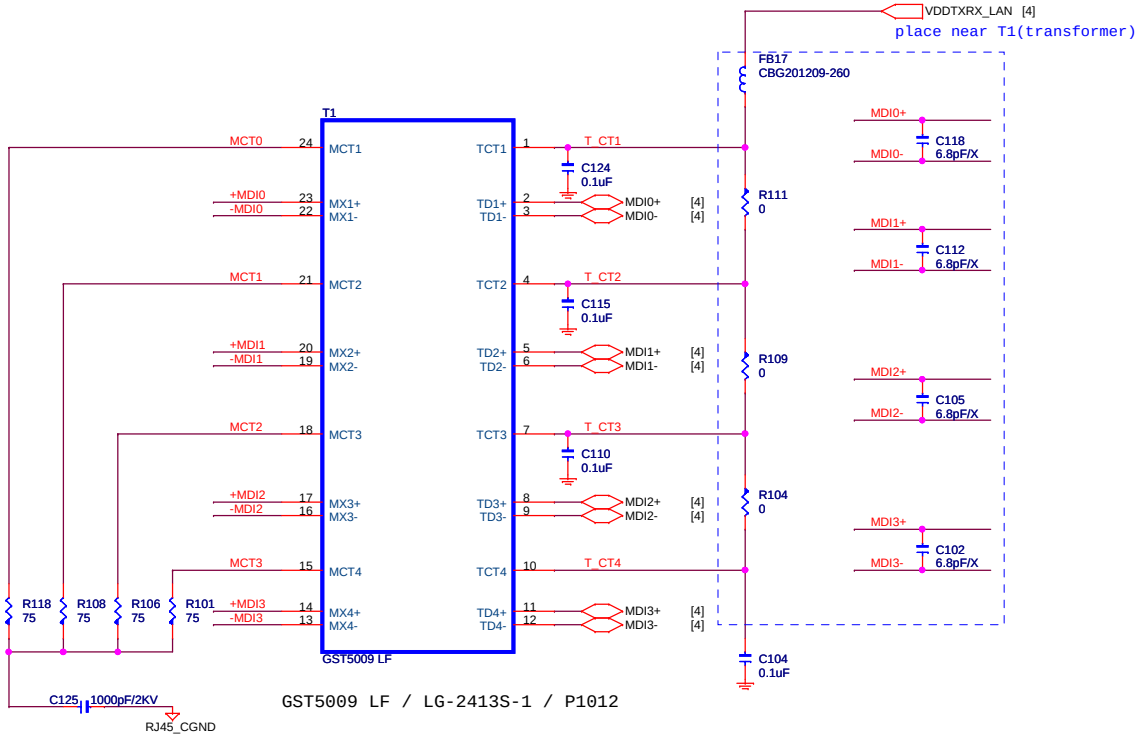
RJ45





GST5009 LF / LG-2413S-1 / P1012

RJ45 Link status GMTI_9711-8814-S0L30-E-A for VT6107

LED Selection	CASE_1
LEDS1,LEDS0	0,1
L10_LED2	Bi-Tripple-color mode {LED2,LED1}=
L9_LED1	01=100M Link(Green) 11=10M Link(Darkless) 00=Link off(Darkless)
L12_LED0	Link/Act (Yellow)

Note: Link: LED on

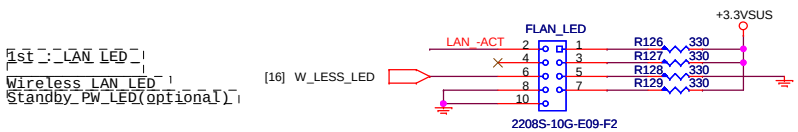
VT6107 T1 install TST1284A LF
VT6122 / VT6130 / RTL8111E T1 install GST5009 LF

T1	VT6107	RTL8111E /VT6122 / VT6130
Bothhand	TST1284A LF 99G26-070542	GST5009 LF 99G26-070532
LANKOM	LF-H6442S-1 99G26-07055F	LG-2413S-1 99G26-07056F
UDE	P1212(007-00) 99G26-07058J	P1012(001-00) 99G26-07053J

	T1	C124,C115	C110	C104	FB17	R111	R104, R109	C118,C112,C105,C102(6.8pFx4)
RTL8111E	GST5009 LF 99G26-070532	X	X	0.01uF	X	0	0	X
VT6107	TST1284A LF 99G26-070542	0	X	X	0	0	X	X
VT6122	GST5009 LF 99G26-070532	0	0	0.1uF	X	X	X	0
VT6130	GST5009 LF 99G26-070532	0	0	0.1uF	0	0	0	X

O:mount X:unmount

FRONT LAN LED



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VIA TECHNOLOGIES INC.

Title	RJ45/ LAN LED	
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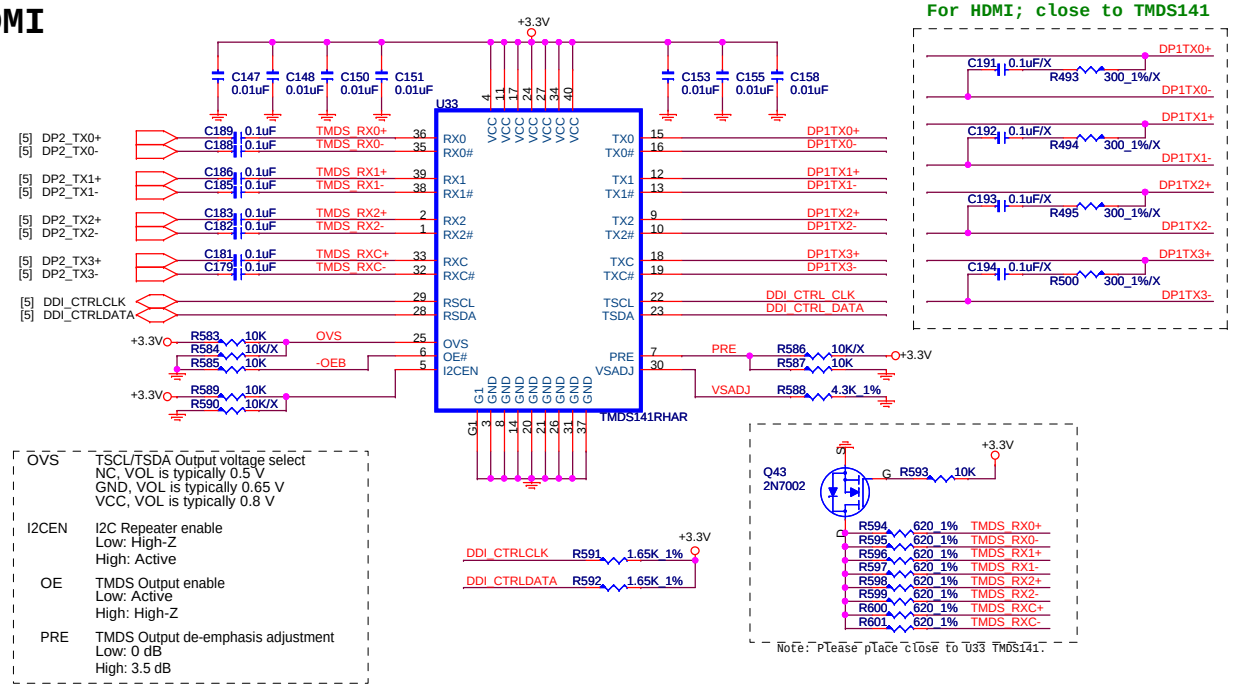
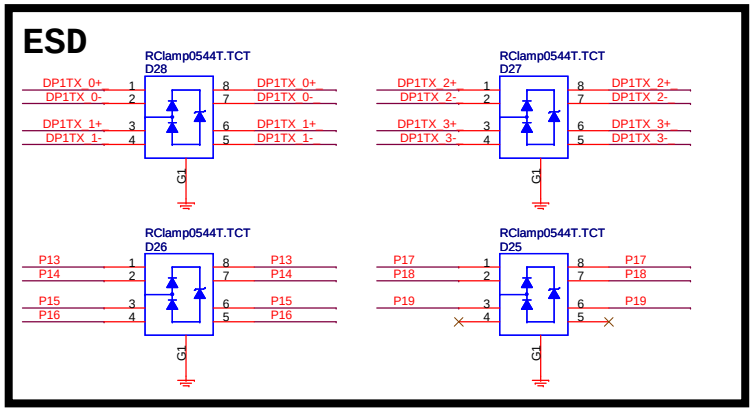
HDMI



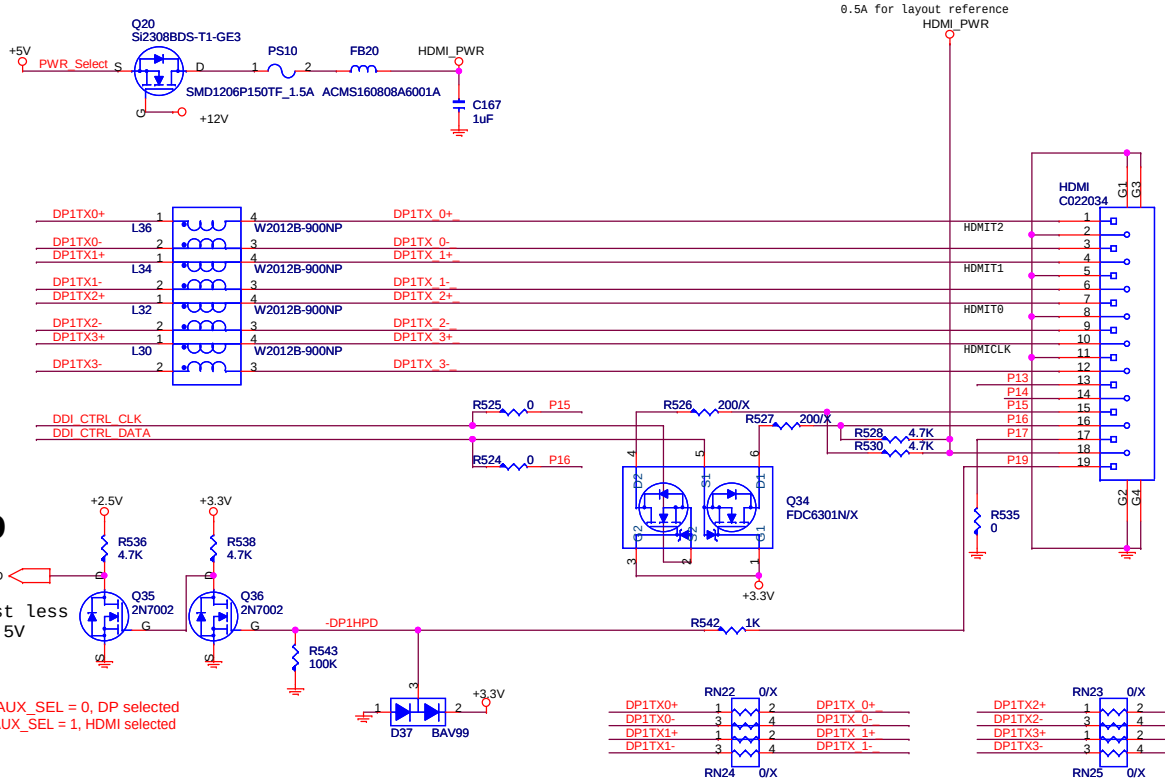
For HDMI; close to TMDS141

ESD Rcalmp
RCLAMP0524P(Package:GSLP2510P8)
RCLAMP0544T(Package:GSLP2010P8T)

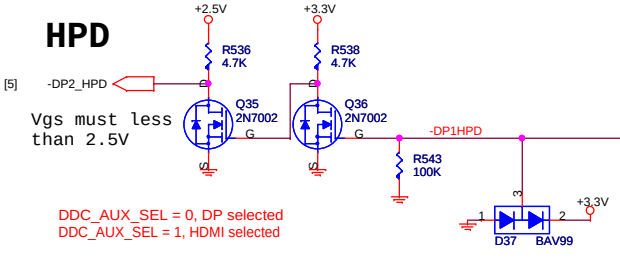


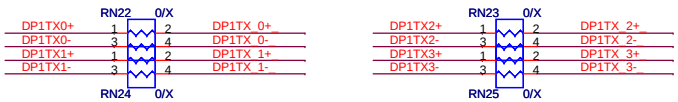
OVS	TSCL/TSDA Output voltage select NC, VOL is typically 0.5 V GND, VOL is typically 0.65 V VCC, VOL is typically 0.8 V
I2CEN	I2C Repeater enable Low: High-Z High: Active
OE	TMDS Output enable Low: Active High: High-Z
PRE	TMDS Output de-emphasis adjustment Low: 0 dB High: 3.5 dB

Note: Please place close to U33 TMDS141.



HPD





	HDMI
1	TMDS D2+
2	GND Shield
3	TMDS D2-
4	TMDS D1+
5	GND Shield
6	TMDS D1-
7	TMDS D0+
8	GND Shield
9	TMDS D0-
10	TMDS CLK+
11	GND Shield
12	TMDS CLK-
13	CEC
14	Reserved
15	SCL
16	SDA
17	DDC/CEC GND
18	+5V Power
19	H.P. Detect
20	

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VIA TECHNOLOGIES INC.

Title: HDMI ReDriver TMDS141

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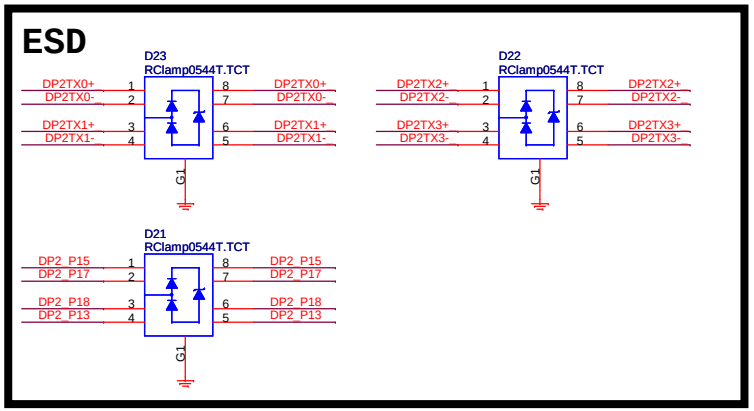
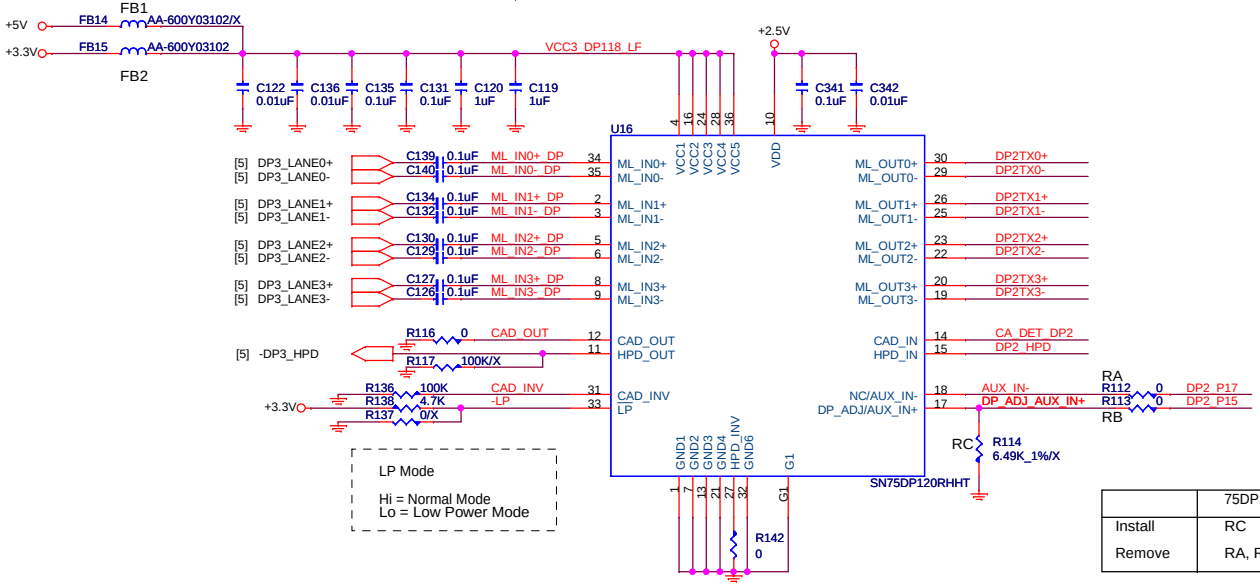
DP reDriver

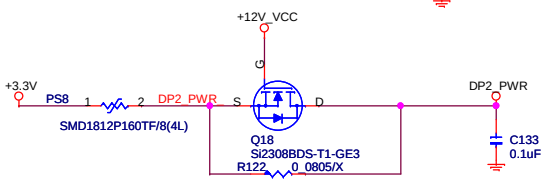
	75DP118	75DP120
Install	FB1	FB2
Remove	FB2	FB1

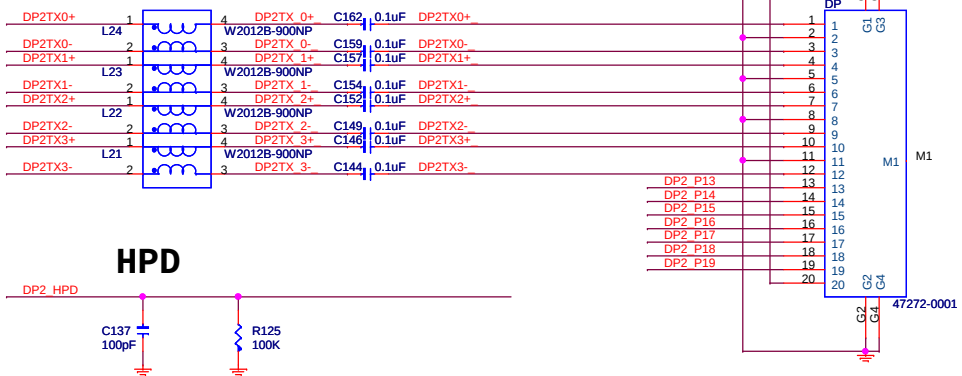
ESD Rcalmp
RCLAMP0524P(Package:GSLP2510P8)
RCLAMP0544T(Package:GSLP2010P8T)

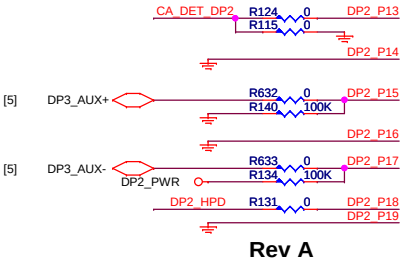




	75DP118	75DP120 *
Install	RC	RA, RB
Remove	RA, RB	RC

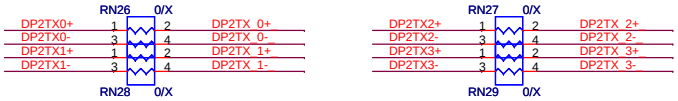






Rev A

HPD



	DisplayPort
1	ML_Lane0+
2	GND
3	ML_Lane0-
4	ML_Lane1+
5	GND
6	ML_Lane1-
7	ML_Lane2+
8	GND
9	ML_Lane2-
10	ML_Lane3+
11	GND
12	ML_Lane3-
13	GND
14	GND
15	AUX_CH+
16	GND
17	AUX_CH-
18	H.P. Detect
19	DP_PWR_Return
20	DP_PWR

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Title	DP reDriver SN75DP120	
Size C	Document Number COMBED2	Rev A
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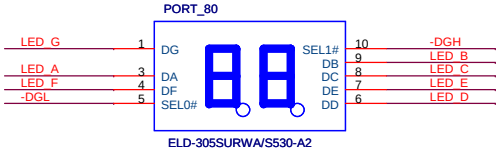
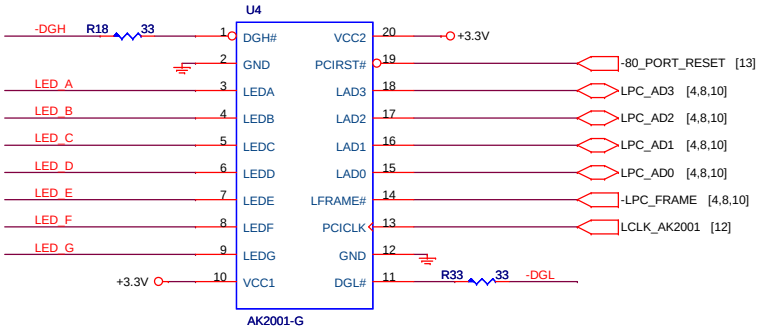
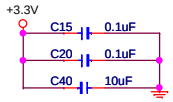
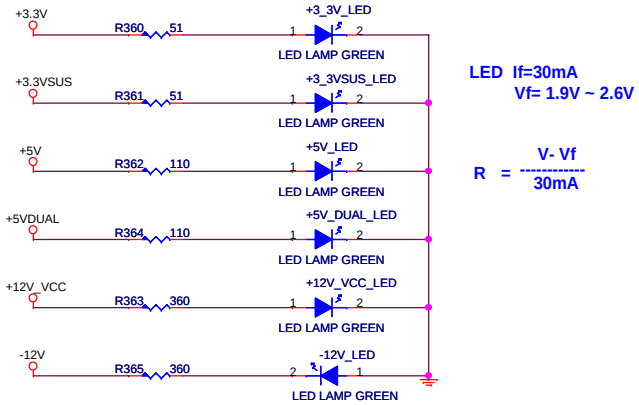
LPC DEBUG PORT







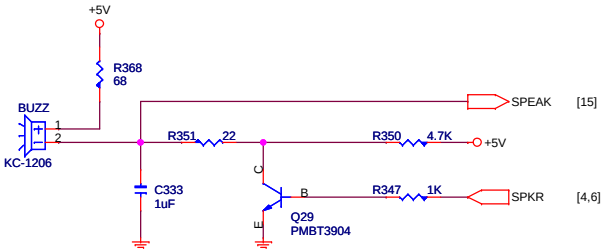
LED



LED If=30mA
Vf= 1.9V ~ 2.6V

$$R = \frac{V - Vf}{30mA}$$

BUZZER



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Title	LPC Debug Port & LED
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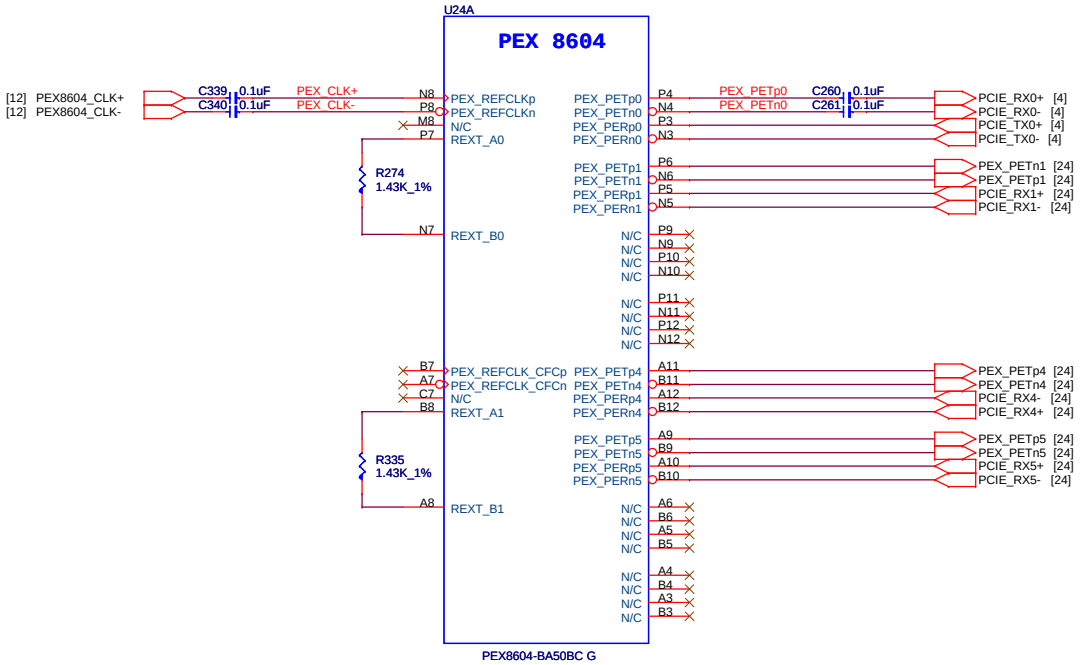
PEX 8604/8608



Port0 from VX900

Port1 to PE1 slot

Port4 to PE2 slot

Port5 to Mini-PCIe

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Title	PEX8604 PCI-e Switch/ClockBuffer	
Size C	Document Number COMEDB2	Rev A
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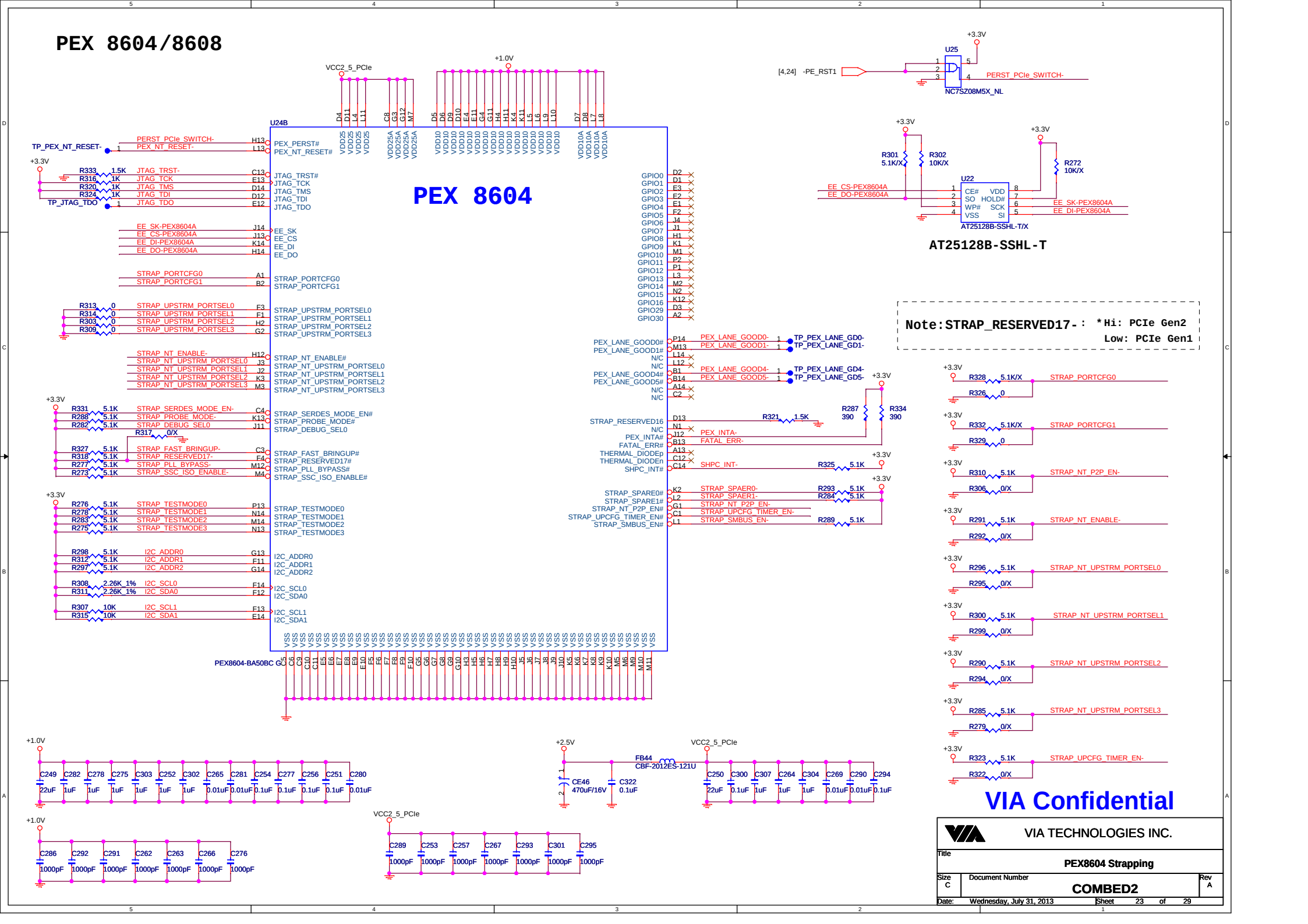
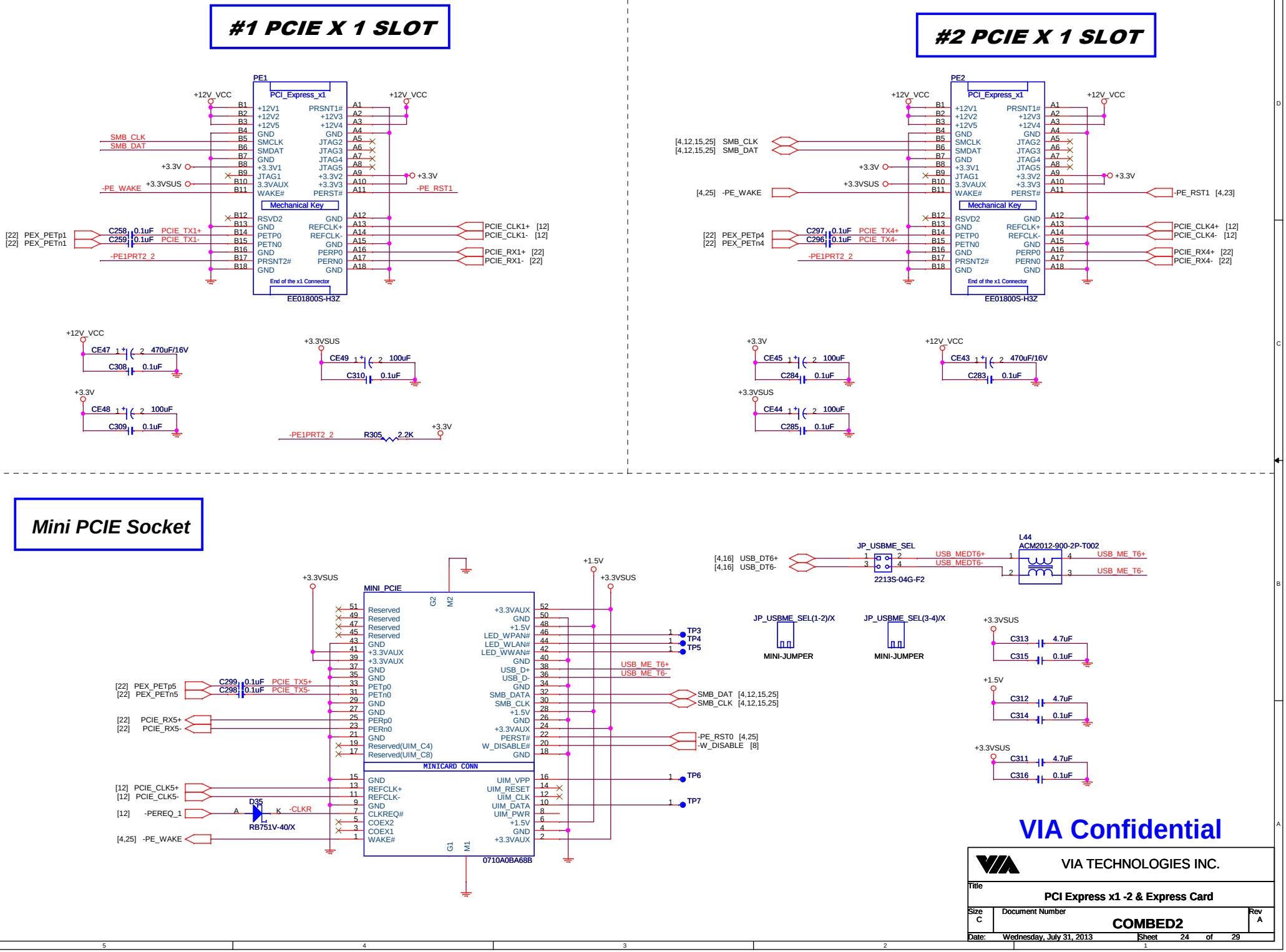
PEX 8604/8608




#1 PCIE X 1 SLOT
PE1
PCI_Express_x1
+12V_VCC
SMB_CLK
SMB_DAT
+3.3V
-PE_WAKE
+3.3VSUS
-PE_RST1
Mechanical Key
End of the x1 Connector
EE01800S-H3Z
[22] PEX_PETp1
[22] PEX_PETn1
C258 0.1uF PCIE_TX1+
C259 0.1uF PCIE_TX1-
-PE1PRT2_2
PCIE_CLK1+ [12]
PCIE_CLK1- [12]
PCIE_RX1+ [22]
PCIE_RX1- [22]
CE47 470uF/16V
C308 0.1uF
CE48 100uF
C309 0.1uF
CE49 100uF
C310 0.1uF
R305 2.2K
#2 PCIE X 1 SLOT
PE2
[4,12,15,25] SMB_CLK
[4,12,15,25] SMB_DAT
[4,25] -PE_WAKE
-PE_RST1 [4,23]
[22] PEX_PETp4
[22] PEX_PETn4
C297 0.1uF PCIE_TX4+
C296 0.1uF PCIE_TX4-
PCIE_CLK4+ [12]
PCIE_CLK4- [12]
PCIE_RX4+ [22]
PCIE_RX4- [22]
CE45 100uF
C284 0.1uF
CE44 100uF
C285 0.1uF
CE43 470uF/16V
C283 0.1uF
Mini PCIE Socket
MINI_PCIE
MINICARD CONN
0710A0BA68B
[22] PEX_PETp5
[22] PEX_PETn5
C299 0.1uF PCIE_TX5+
C298 0.1uF PCIE_TX5-
[22] PCIE_RX5+
[22] PCIE_RX5-
[12] PCIE_CLK5+
[12] PCIE_CLK5-
[12] -PEREQ_1
[4,25] -PE_WAKE
D35
RB751V-40/X
-CLKR
SMB_DAT [4,12,15,25]
SMB_CLK [4,12,15,25]
-PE_RST0 [4,25]
-W_DISABLE [8]
USB_ME_T6+
USB_ME_T6-
TP3
TP4
TP5
TP6
TP7
[4,16] USB_DT6+
[4,16] USB_DT6-
JP_USBME_SEL
2213S-04G-F2
USB_MEDT6+
USB_MEDT6-
L44
ACM2012-900-2P-T002
JP_USBME_SEL(1-2)/X
JP_USBME_SEL(3-4)/X
MINI-JUMPER
C313 4.7uF
C315 0.1uF
C312 4.7uF
C314 0.1uF
C311 4.7uF
C316 0.1uF
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Title
PCI Express x1 -2 & Express Card
Size C
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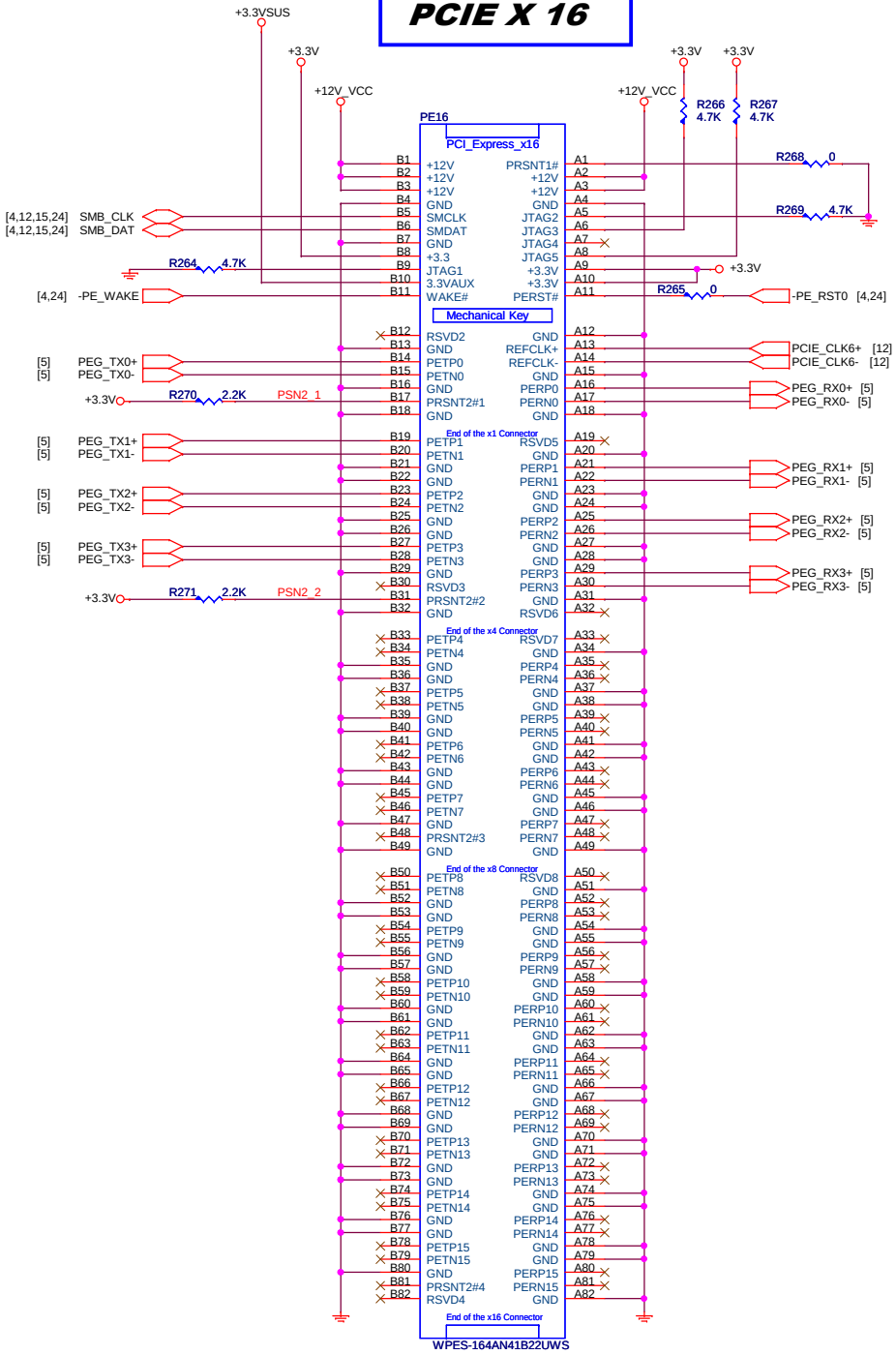
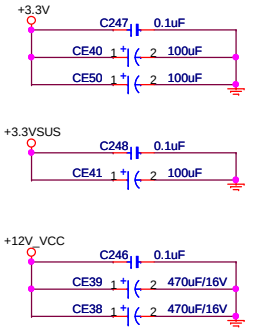
PCIE X 16





Close PCI Express x16 Slot

PCI Express x16, +12V 300mil width.

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Title	PCI Express x16	
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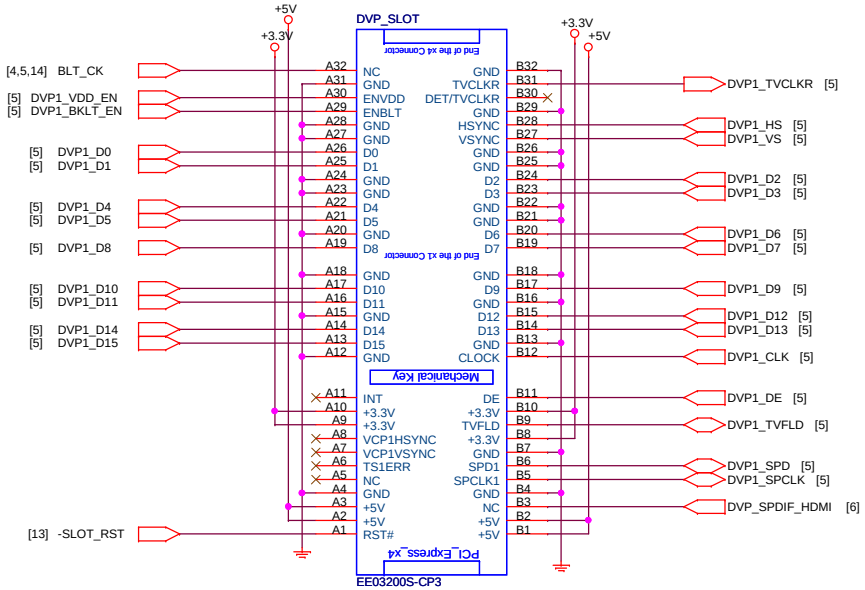
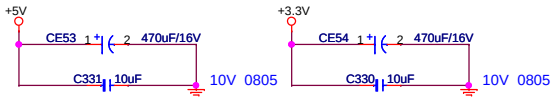
DVP SLOT





TV_DVP_SEL	DVP1TVCLKR function selection
1-2	TTL/TV from DVP
2-3*	Plug detection from DVP

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Title	DVP SLOT	
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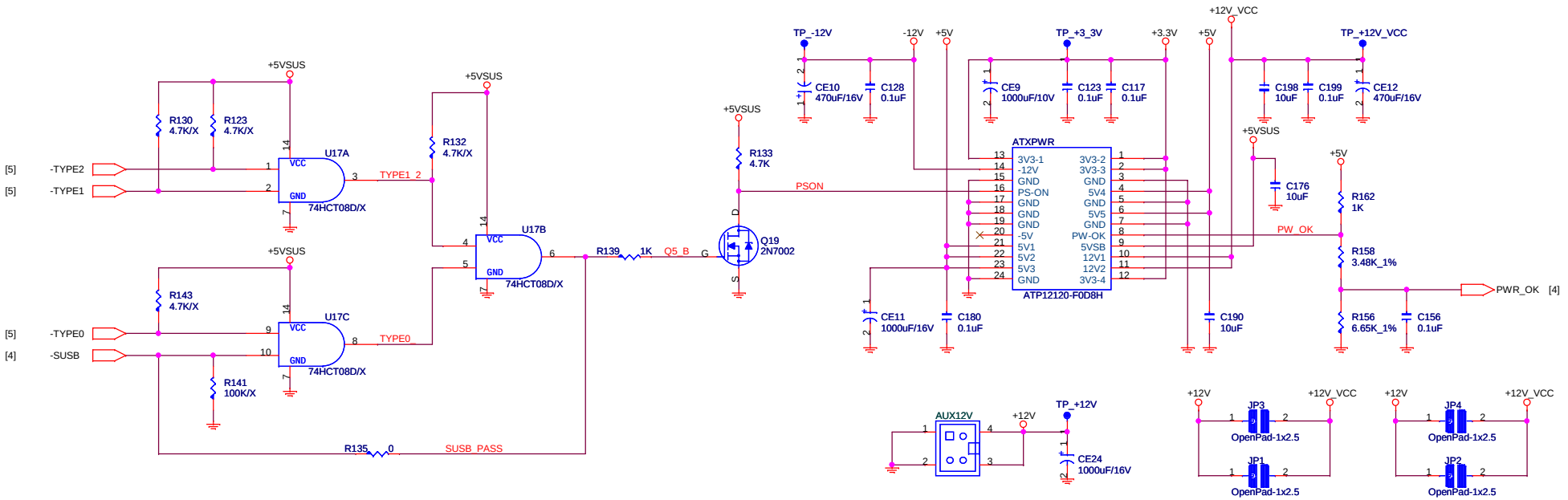
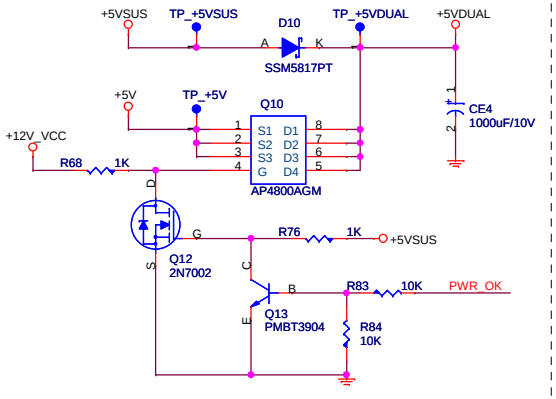
ATX POWER

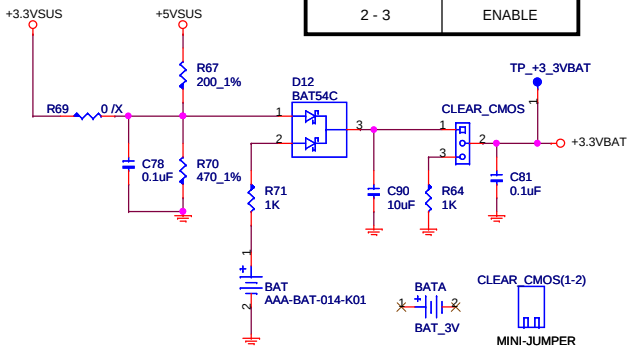


+5VDUAL

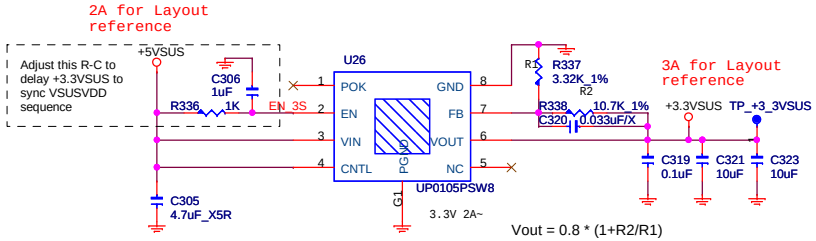


VCC_RTC

CLEAR_CMOS	FUNCTION
* 1 - 2	NORMAL
2 - 3	ENABLE

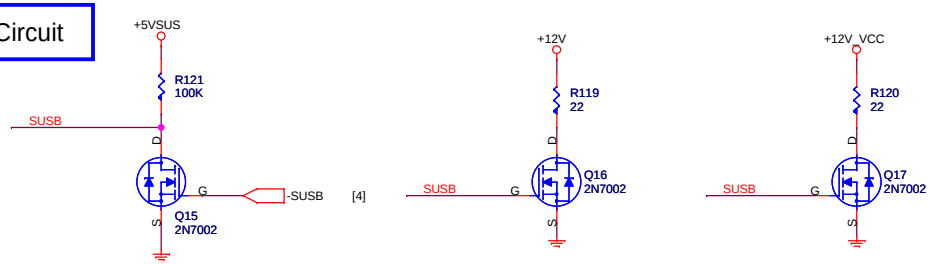


+3.3VSUS



Iout Max = 2A

Discharge Circuit



-SUSB	-SUSC	Pstate
0	0	S4/S5
0	1	S3
1	1	S1

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Title	ATX POWER	
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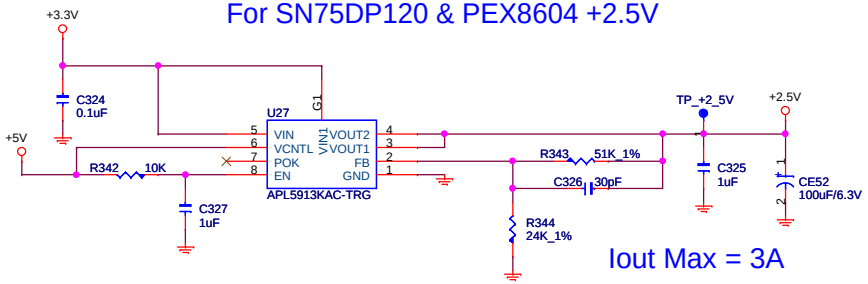
+2.5V

For SN75DP120 & PEX8604 +2.5V

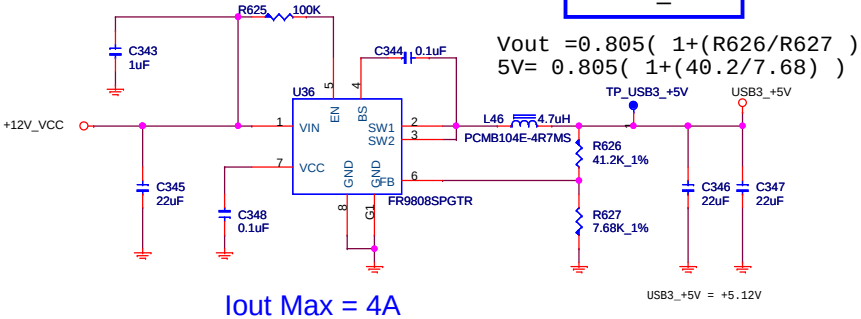


Iout Max = 3A

For USB3 Connector +5V

USB3_+5V

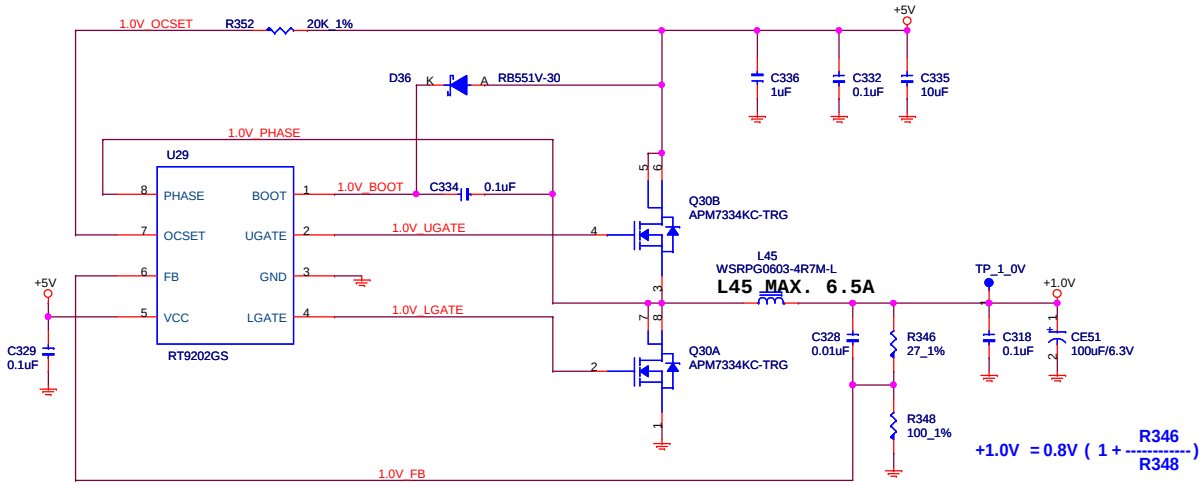
Vout =0.805(1+(R626/R627)
5V= 0.805(1+(40.2/7.68))



Iout Max = 4A

+1.0V

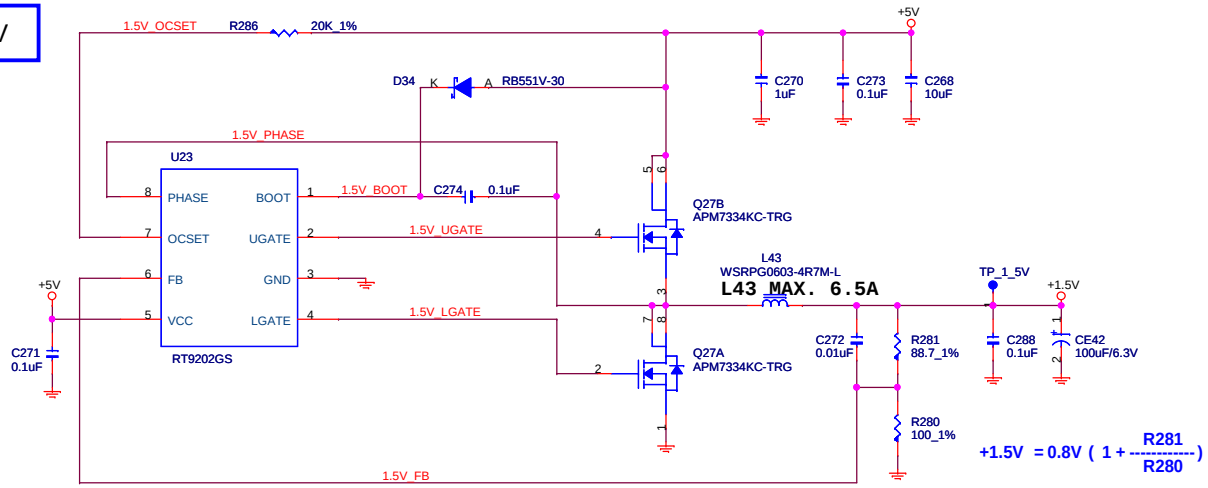
For PEX8604 +1.0V



$$+1.0V = 0.8V \left(1 + \frac{R346}{R348}\right)$$

+1.5V

For Mini-PCIe Slot +1.5V



$$+1.5V = 0.8V \left(1 + \frac{R281}{R280}\right)$$

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Title: System Power	
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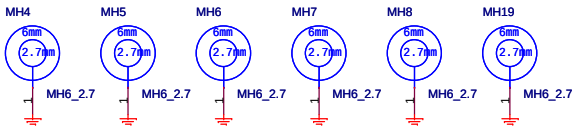
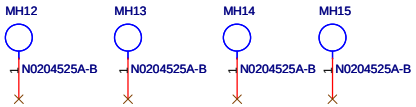
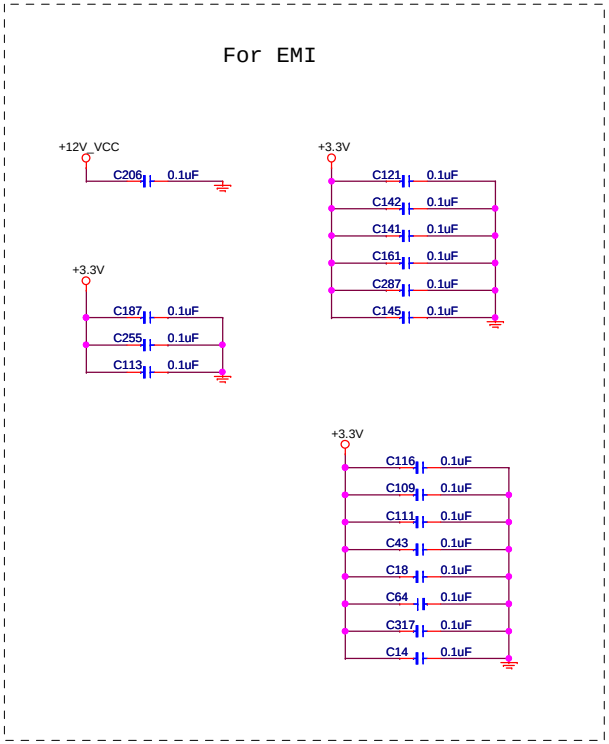
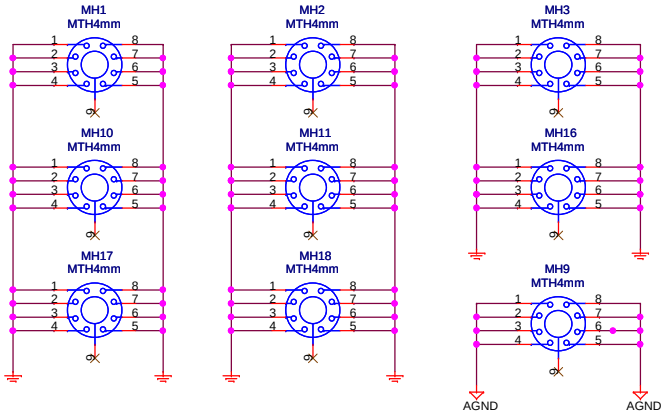
FOR COM EXPRESS MODULE



FOR Mini-PCIE MODULE







FIDUCIAL MARK

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Title: Mounting Holes		
Size: C	Document Number: COMBD2	Rev: A
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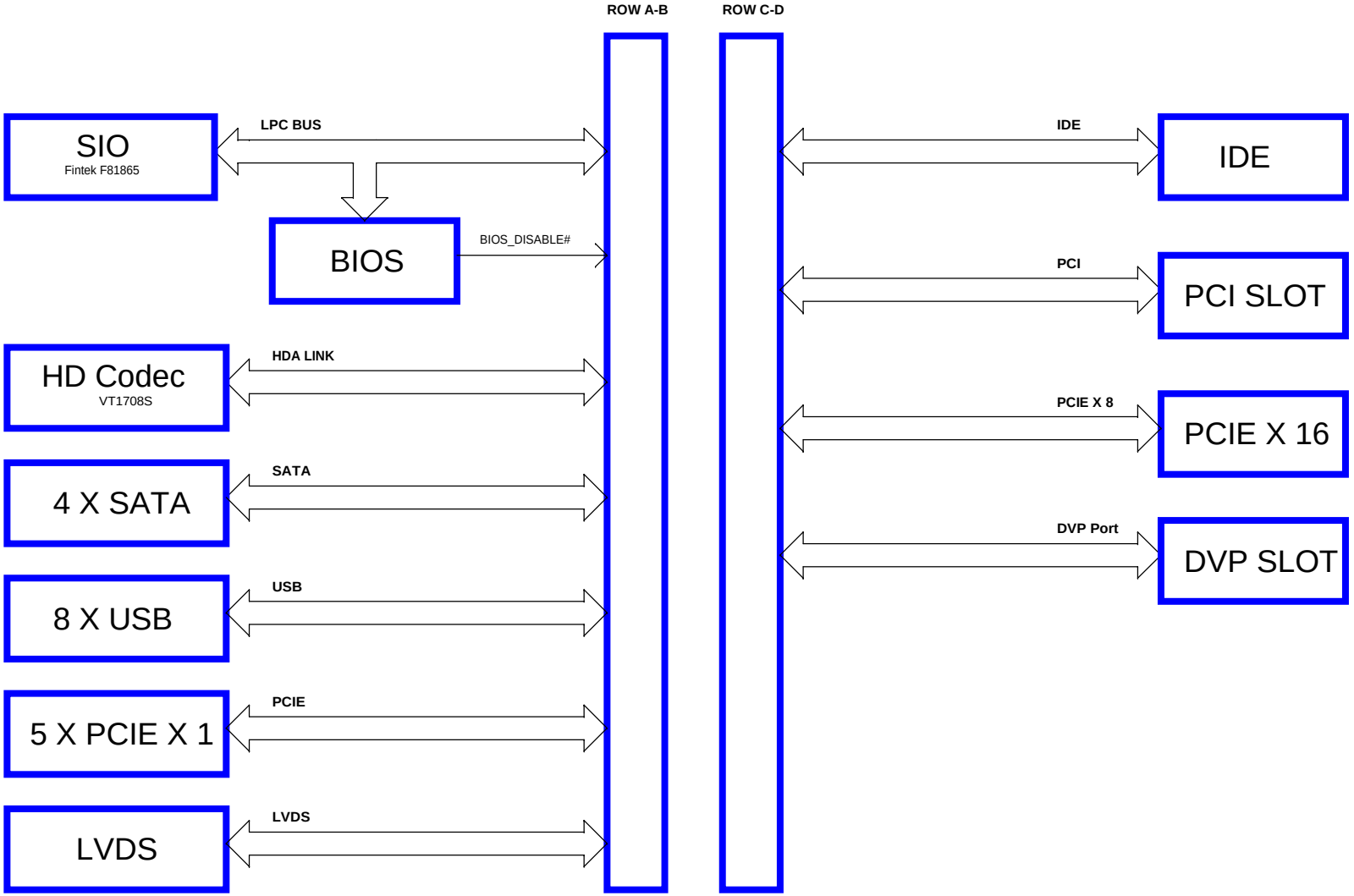
COMEBD1 Block Diagram



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Title	Block Diagram	
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COMEDB1

Revision A

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COM Express Connector (C-D)	4
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Audio Connectors	6
LPCSIO F81865	7
PCI-E / PCI CLOCK BUFFER	8
PS2 KB / MS, VGA CONNECTOR	9
IDE, CF CARD CONNECTOR	10
SATA, FAN CONNECTOR	11
COM1, COM2 PORTS	12
COM3, COM4 PORTS	13
PRINTER PORT, BIOS, LPC HEADER	14
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LPC DEBUG PORT, LED	20
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PCI-E X1 SLOT 4, 5, 6	22
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DVP SLOT	24
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ATX Power Connector / Reset / OTHERS DC-DC Converters	27
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Title	COVER SHEET	
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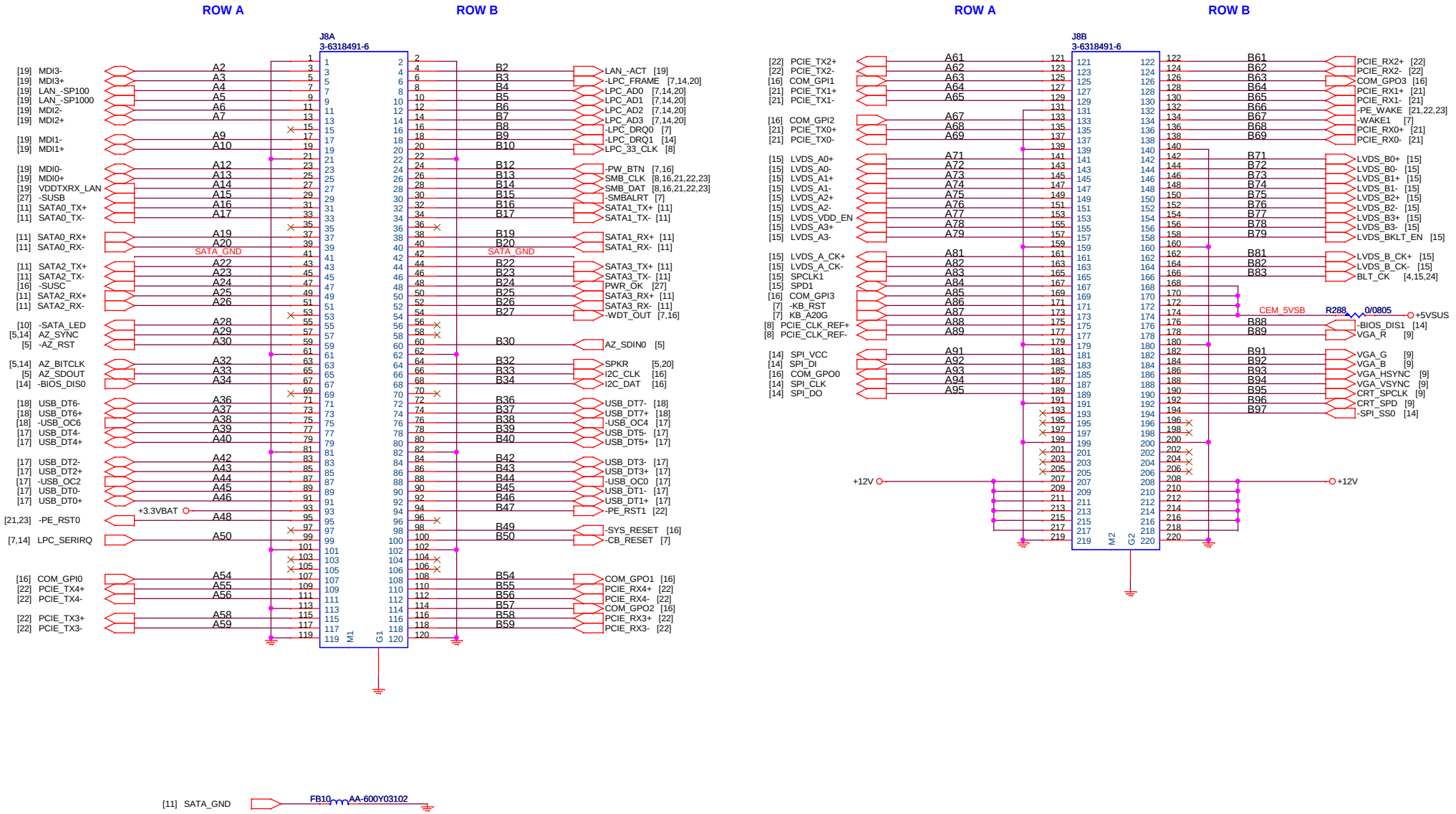

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Title	COME_CONN(A-B)
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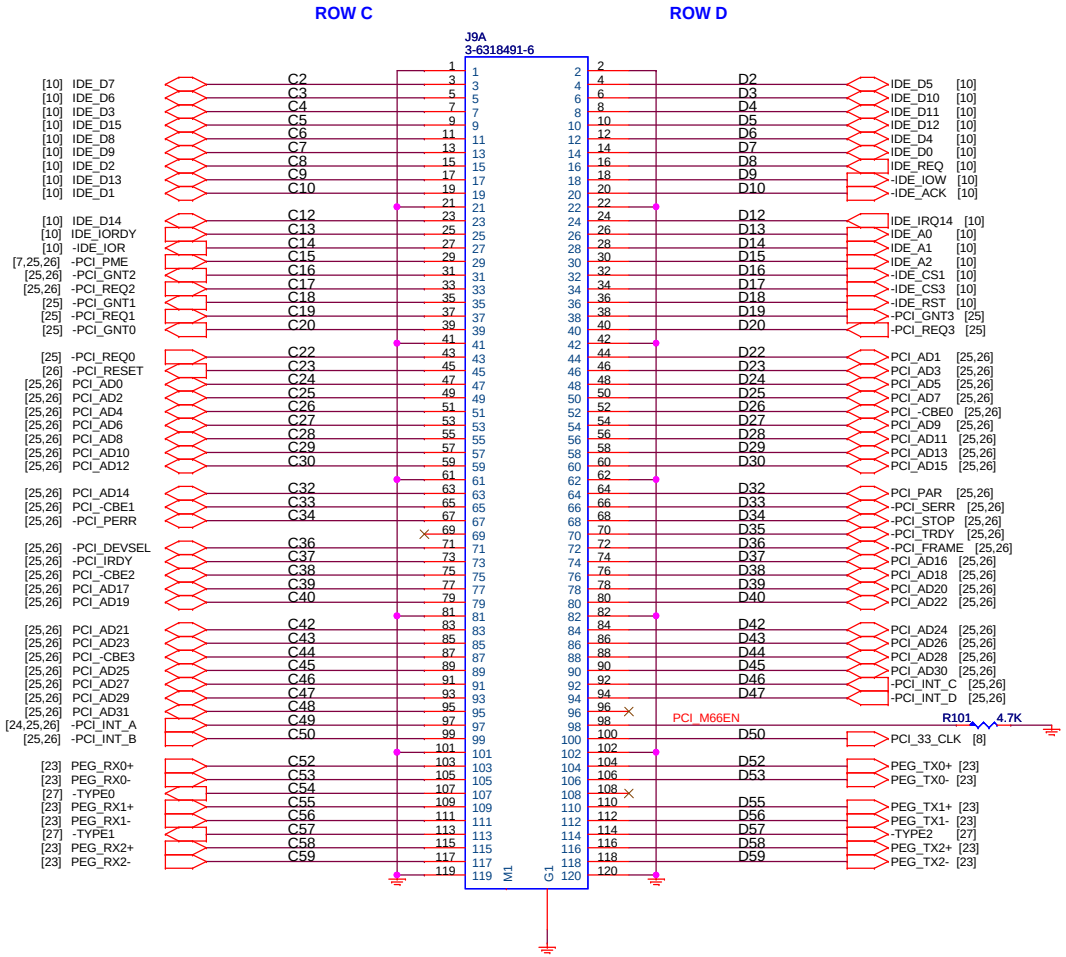

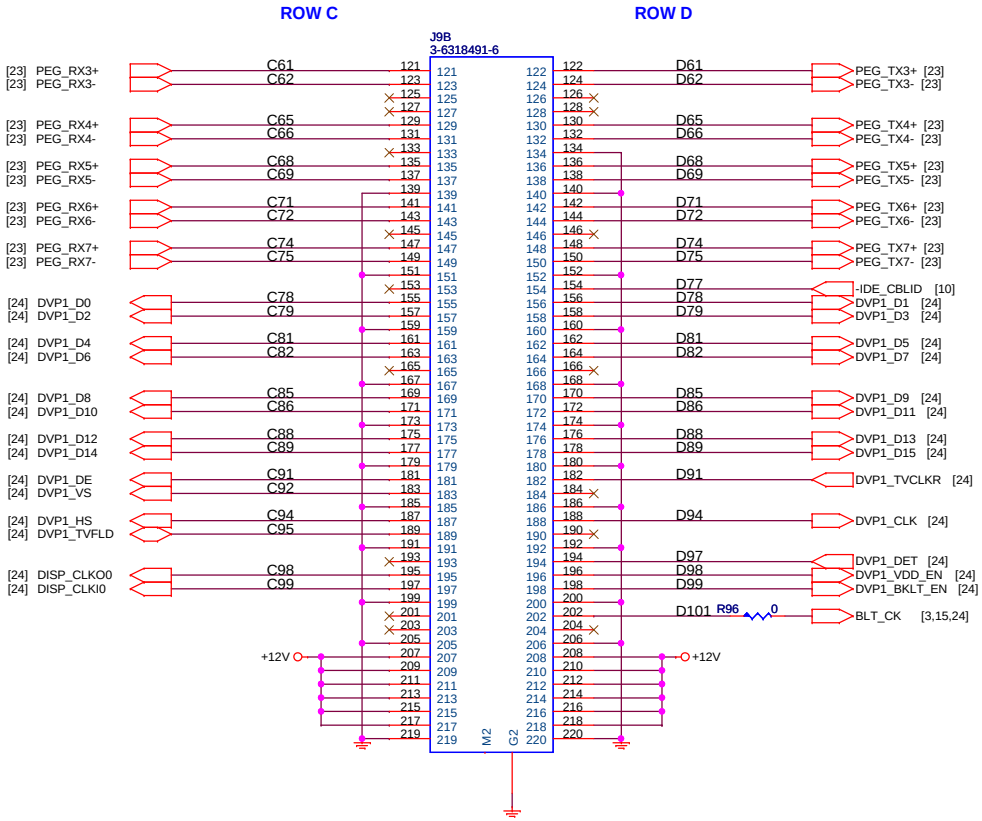

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Title	COME_CONN (C-D)	
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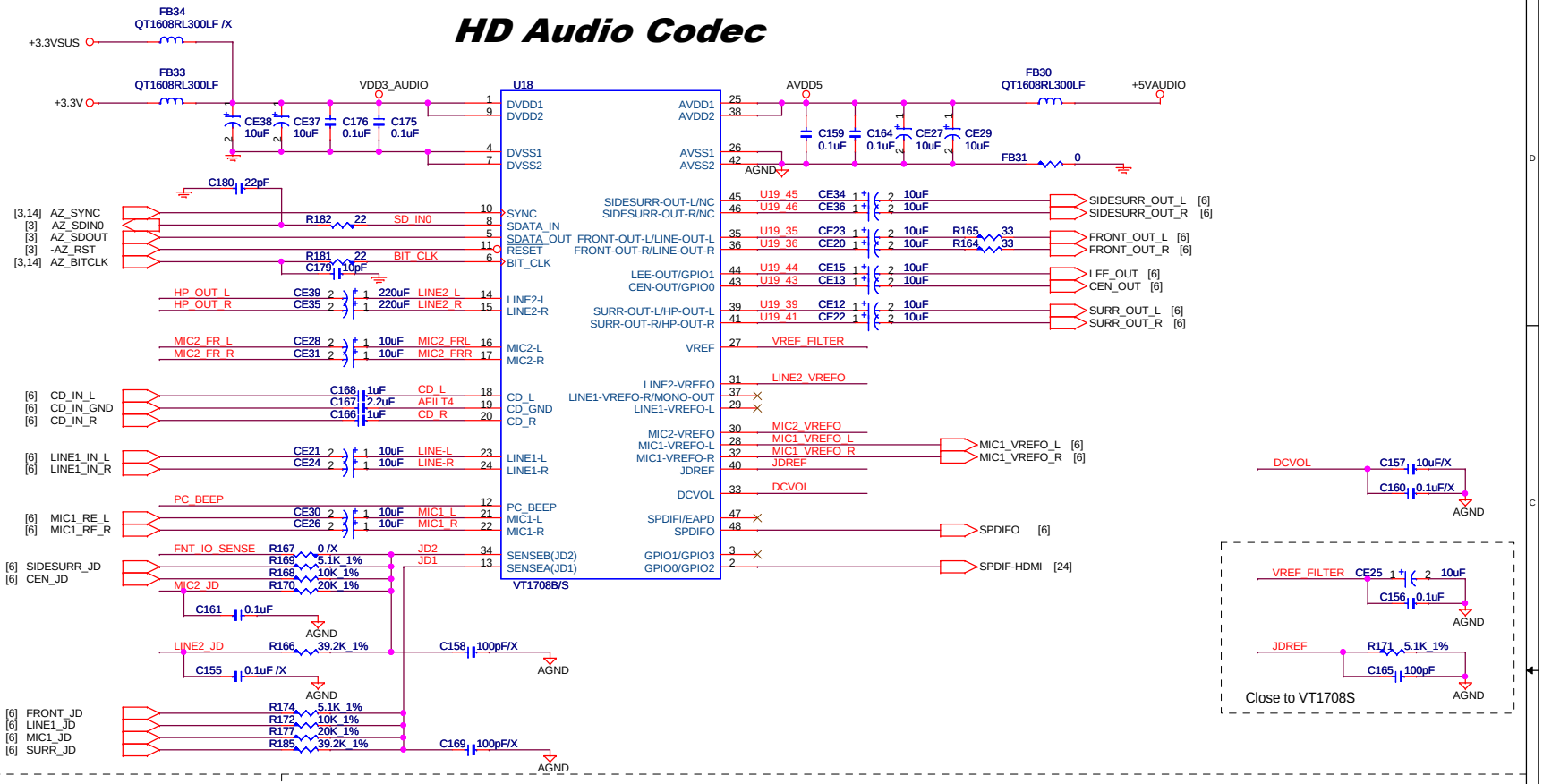
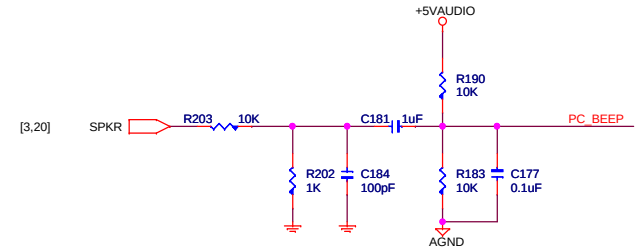
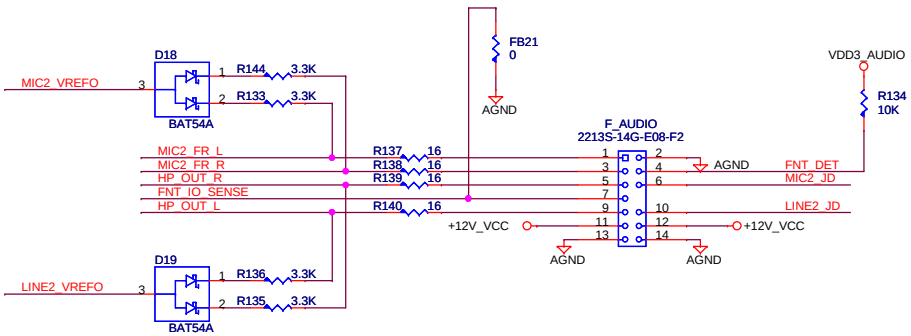
HD Audio Codec

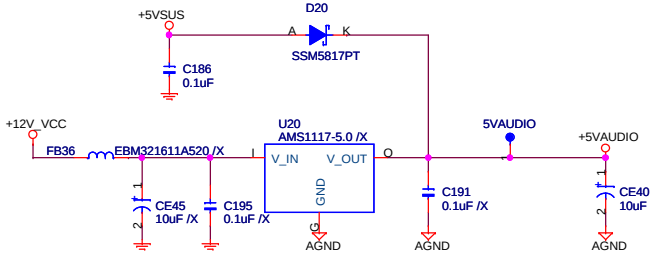


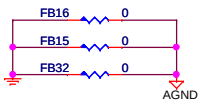


FRONT AUDIO



+5VAUDIO





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Title: HD Audio VT1708A		
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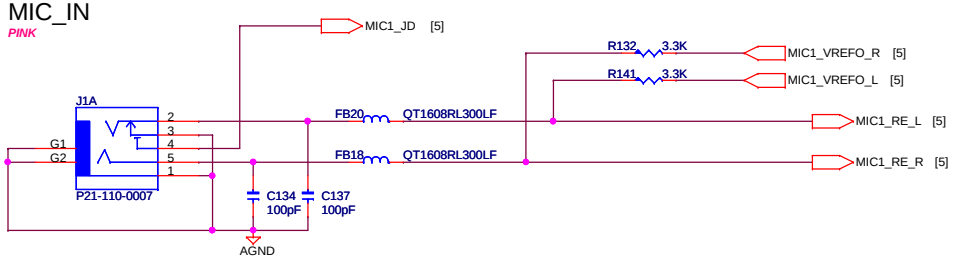
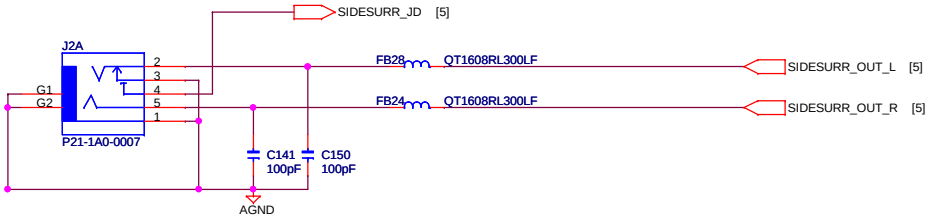
MIC_IN

PINK



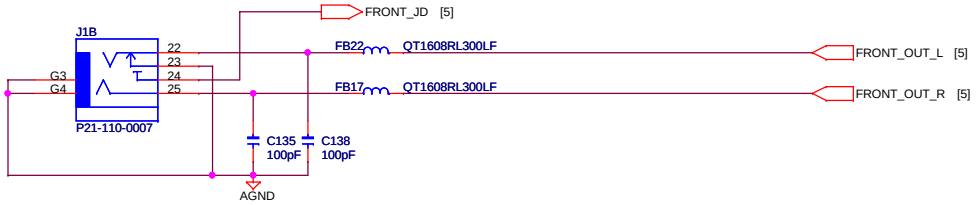
SIDESURR_OUT

GREY



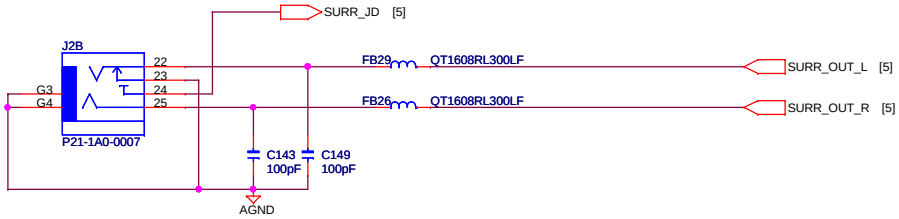
FRONT_OUT

GREEN



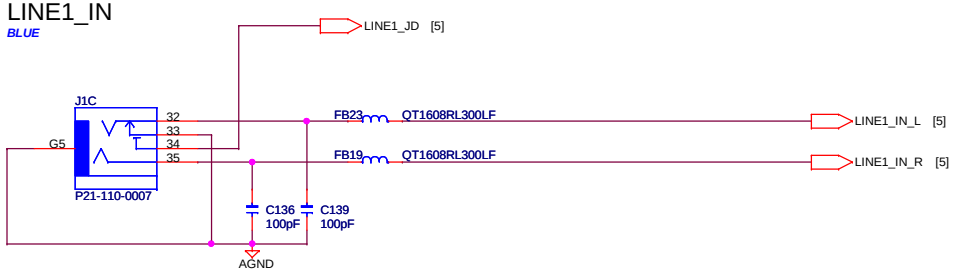
SURR_OUT

BLACK



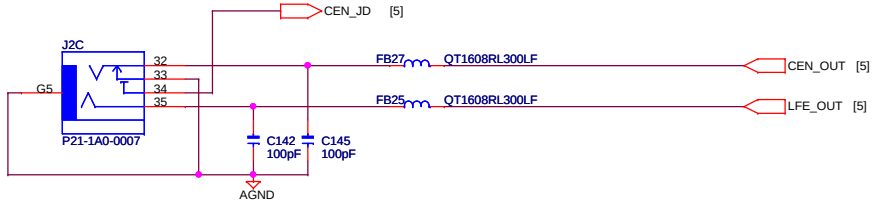
LINE1_IN

BLUE

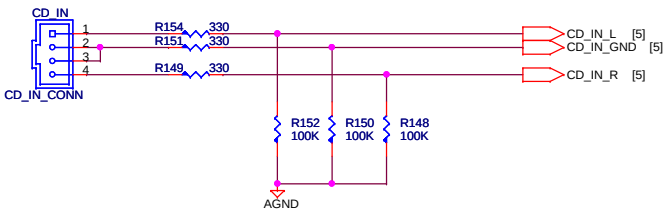


CENTER/LFE

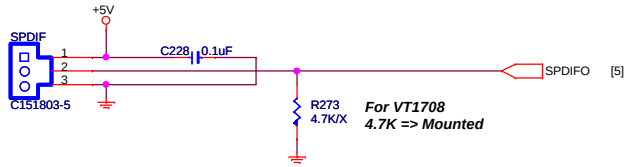
ORANGE



CD_IN



SPDIF



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VIA TECHNOLOGIES INC.	
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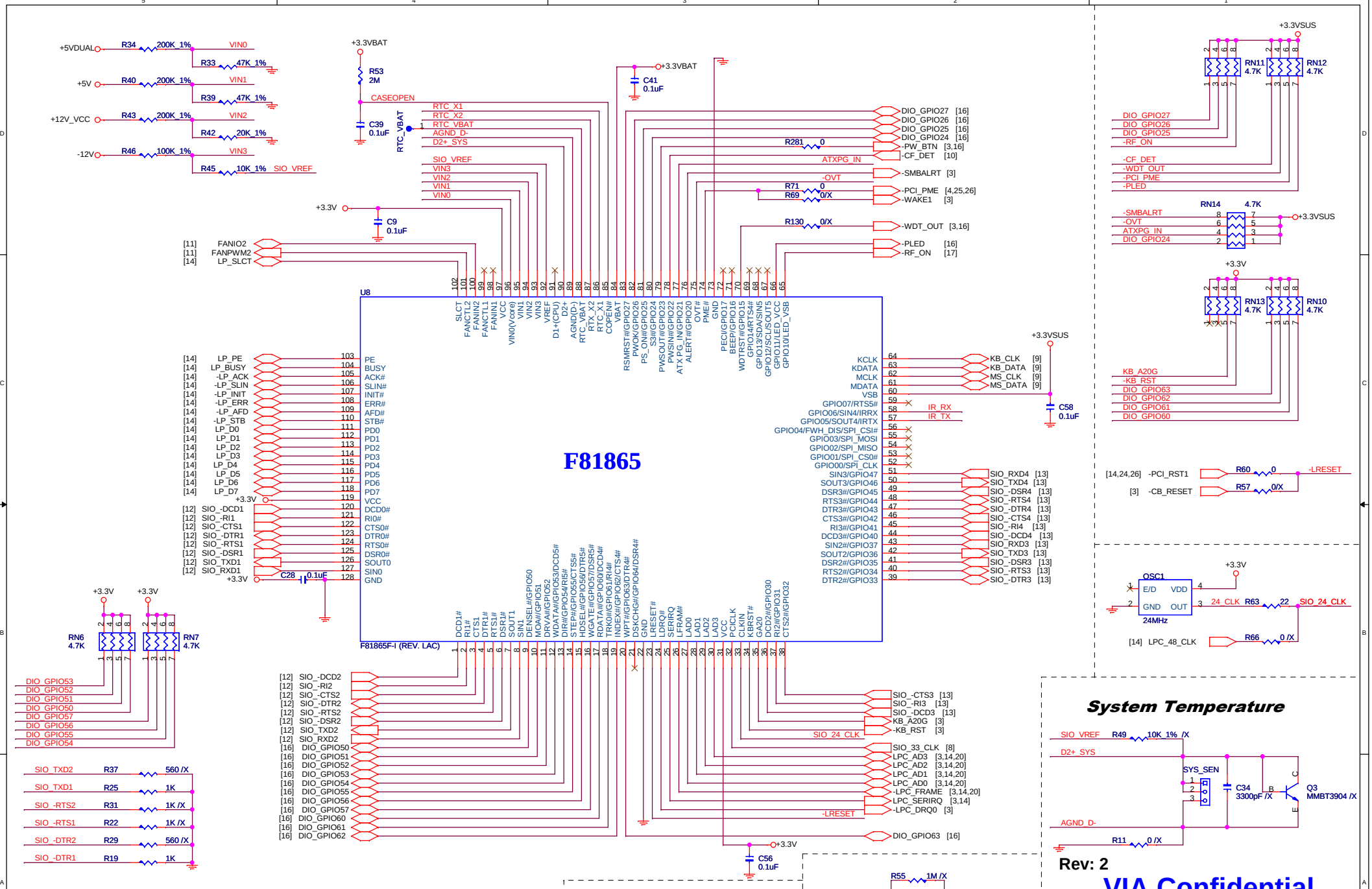

SIO_TXD2 On : SPI Enable Off : SPI Disable

SIO_TXD1 On : Config 2E Off : Config 4E

SIO_-RTS2 On : DAC Off : PWM

SIO_-RTS1 On : IC2 5A Off : IC2 5C

SIO_-DTR2 On : SPI as a Primary BIOS Off : SPI as a Back up BIOS

SIO_-DTR1 : On : FAN 100% Off : FAN 60%

Rev: 2

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VIA TECHNOLOGIES INC.

Title	F81865F	
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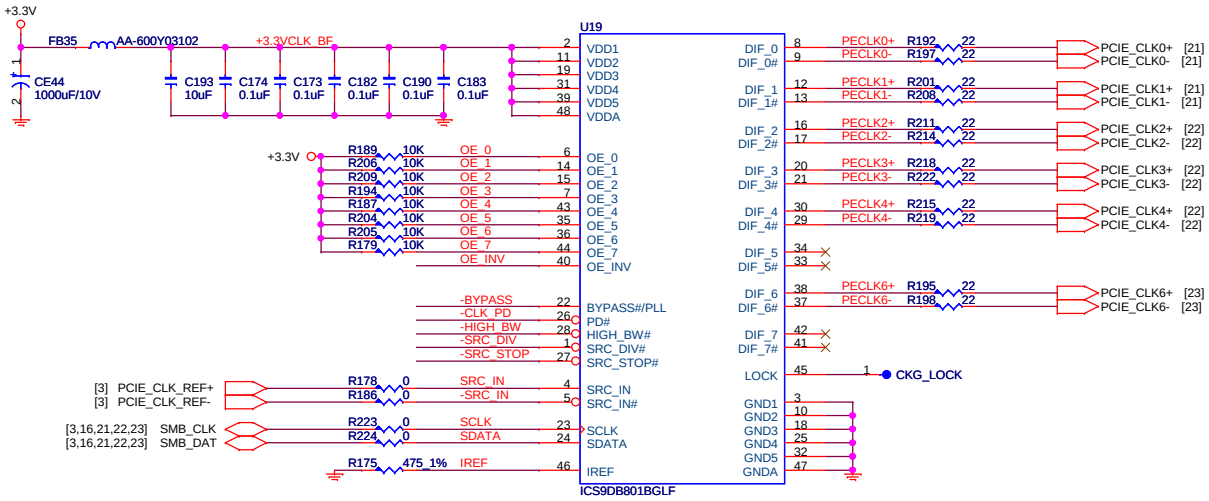
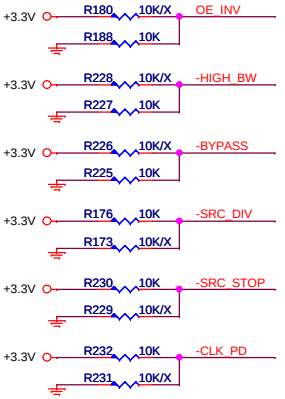
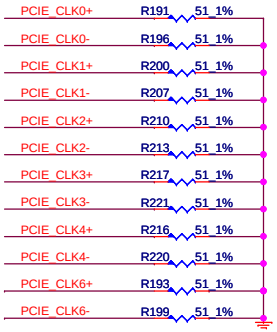
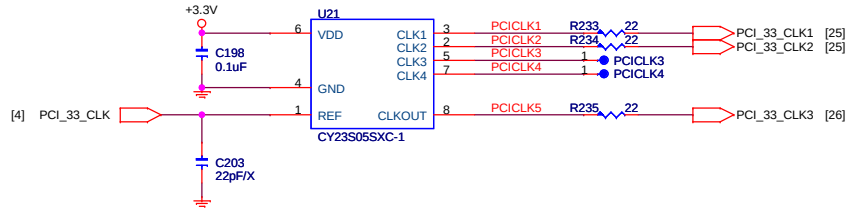
PCIE CLOCK BUFFER



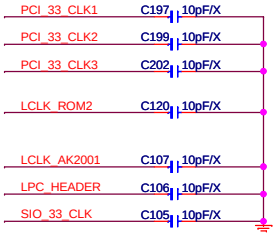




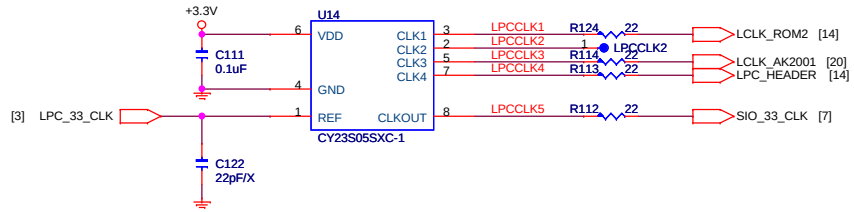
PCI CLOCK BUFFER



meet Zdif=49.9 ohm



LPC CLOCK BUFFER



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VIA TECHNOLOGIES INC.

Title	PCIE / PCI Clock Buffer	
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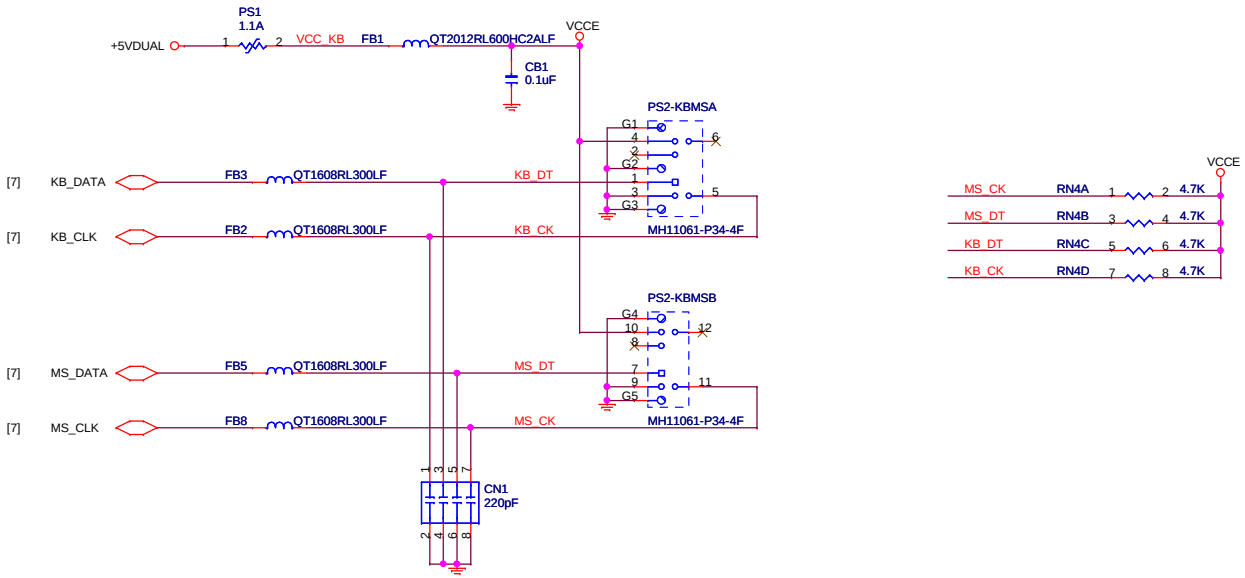
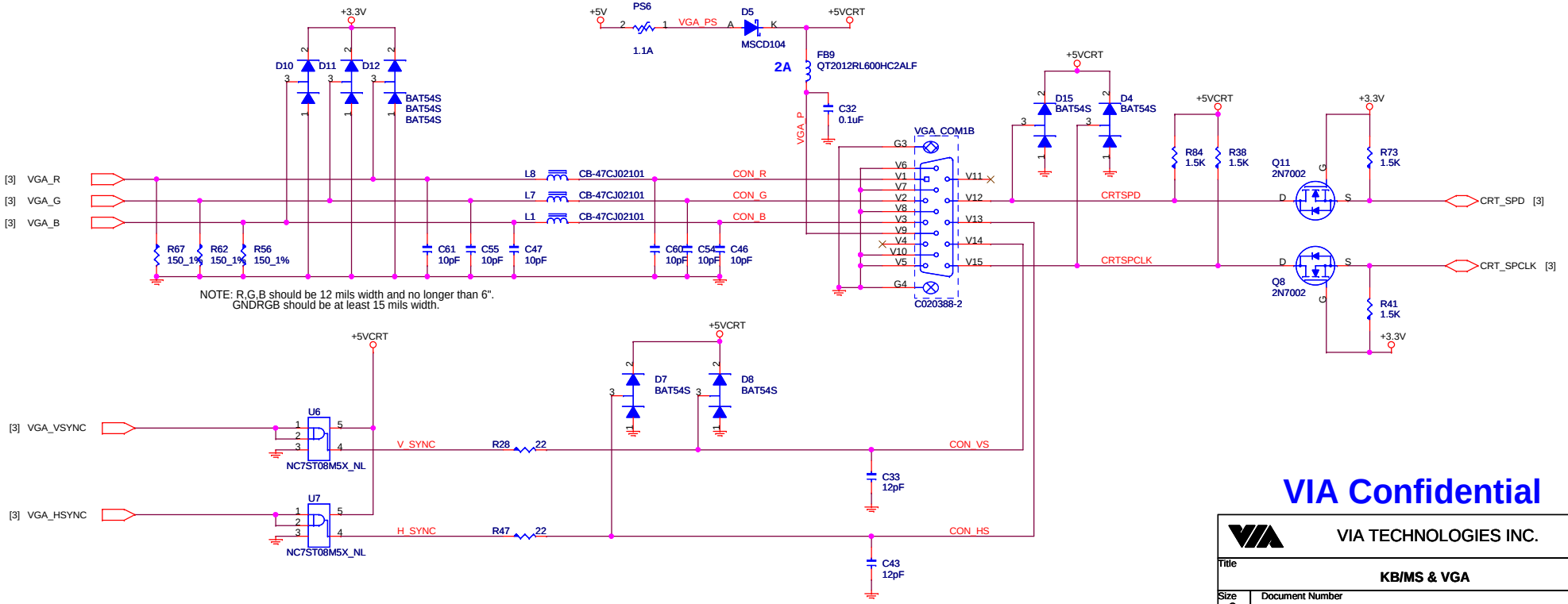
KB / MS



VGA



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Title: KB/MS & VGA		
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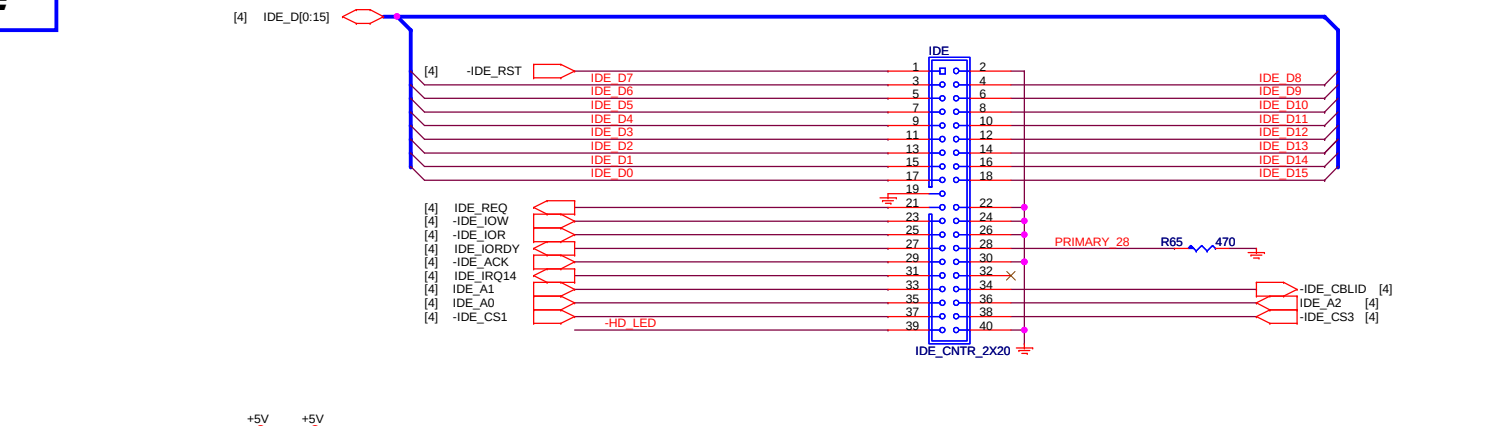
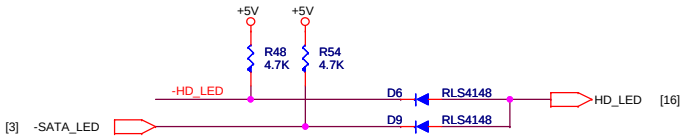
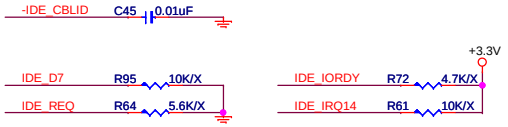
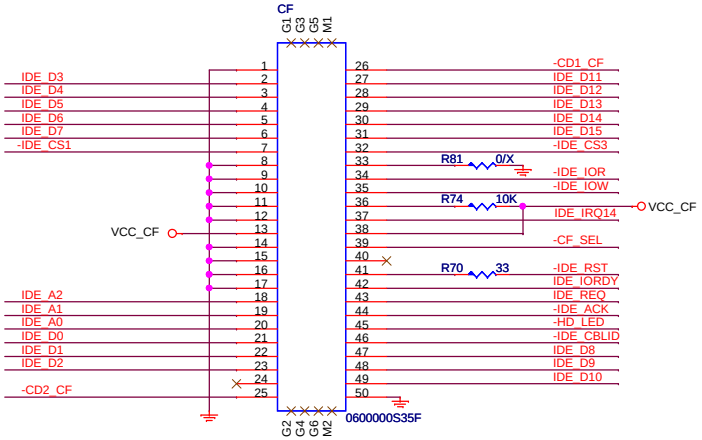
IDE

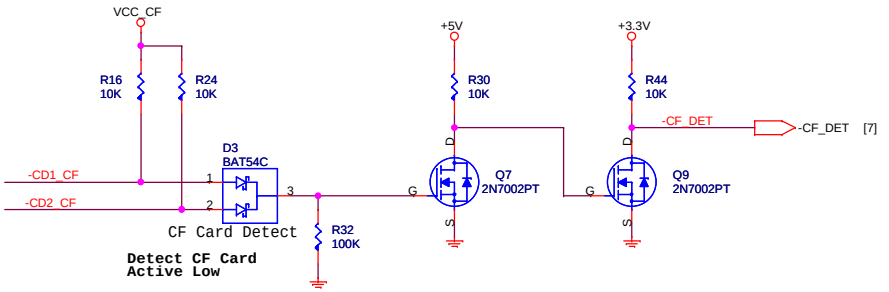






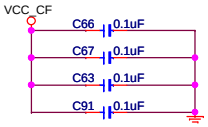
CF Card

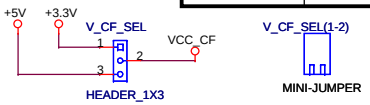




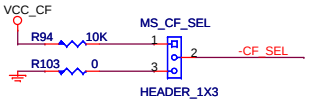
CF VOLTAGE	V_CF_SEL
+3.3V	1 - 2
+5V	2 - 3

CF MASTER/SLAVE	MS_CF_SEL
SLAVE	1 - 2
MASTER	2 - 3





V_CF : Power Voltage Selection
Default: Pin (1,2) Close



MS_CF_SEL1:
* PIN 1-2: Hi -> Slave : Default
PIN 2-3: Lo -> Master

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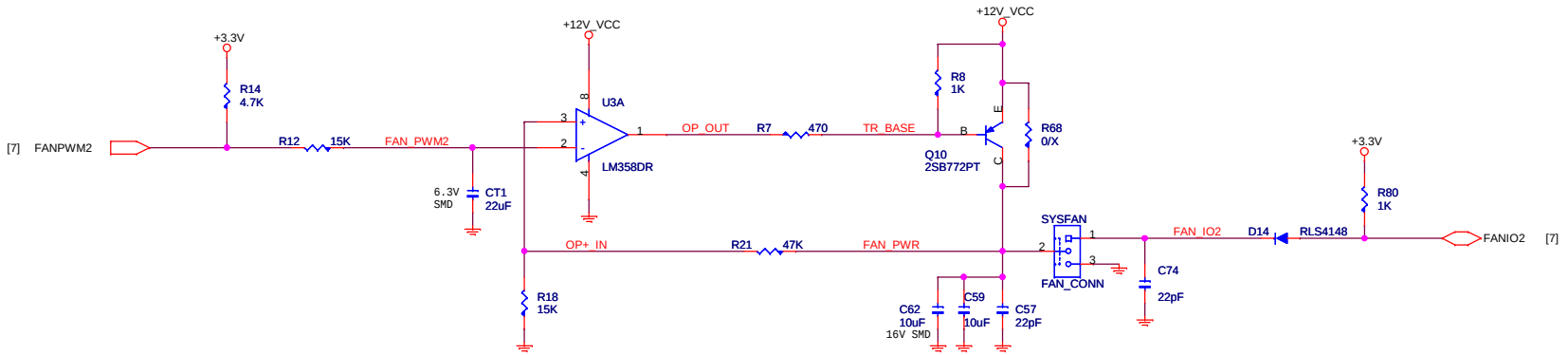
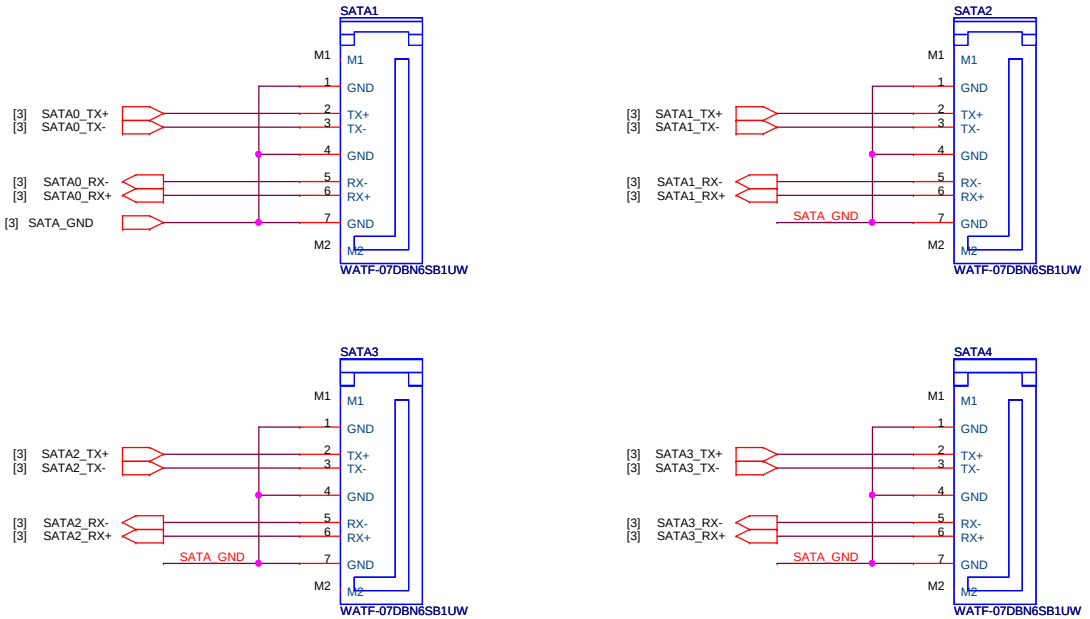
FAN CONNECTOR



SATA



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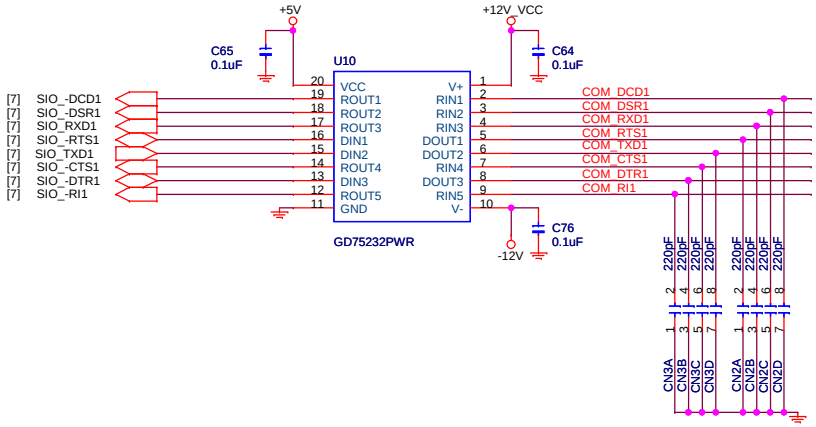
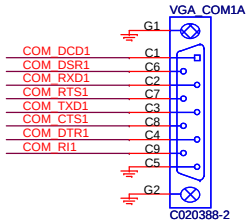
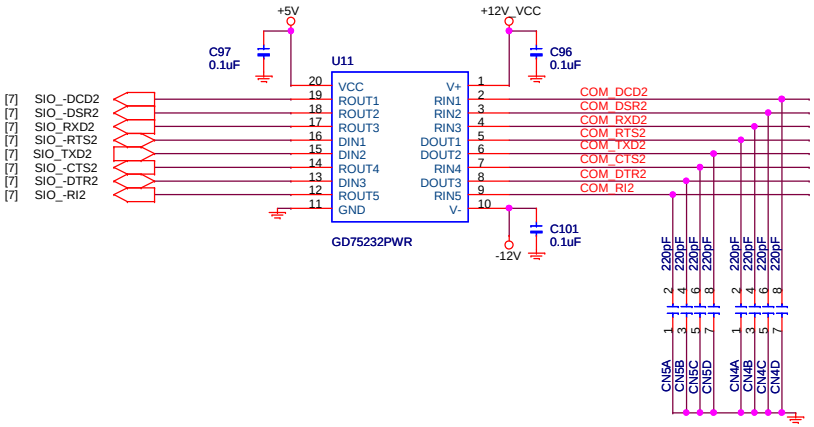
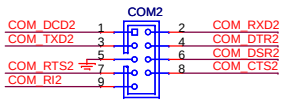
COM 1





COM 2





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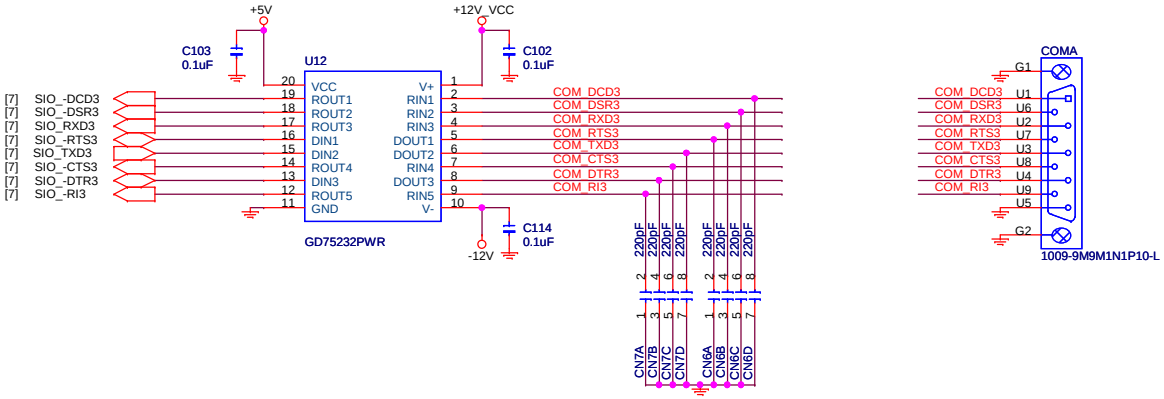
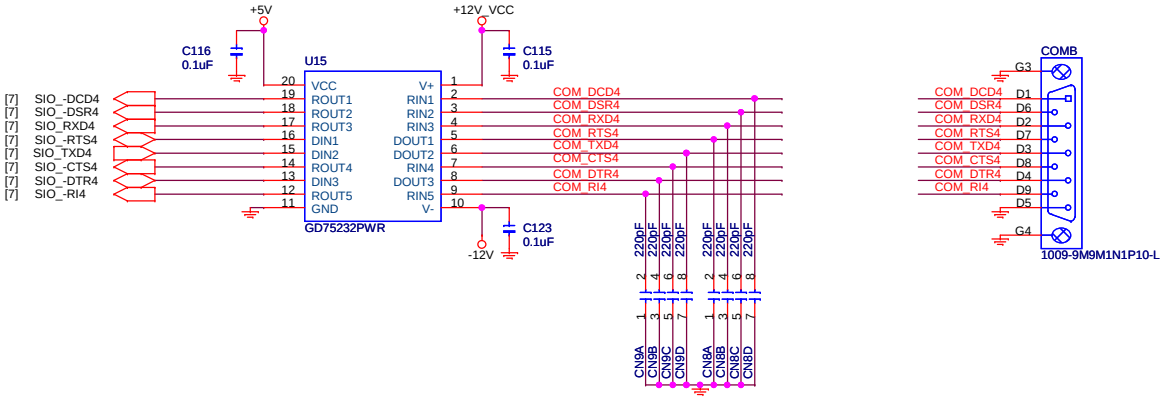
COM 3



COM 4



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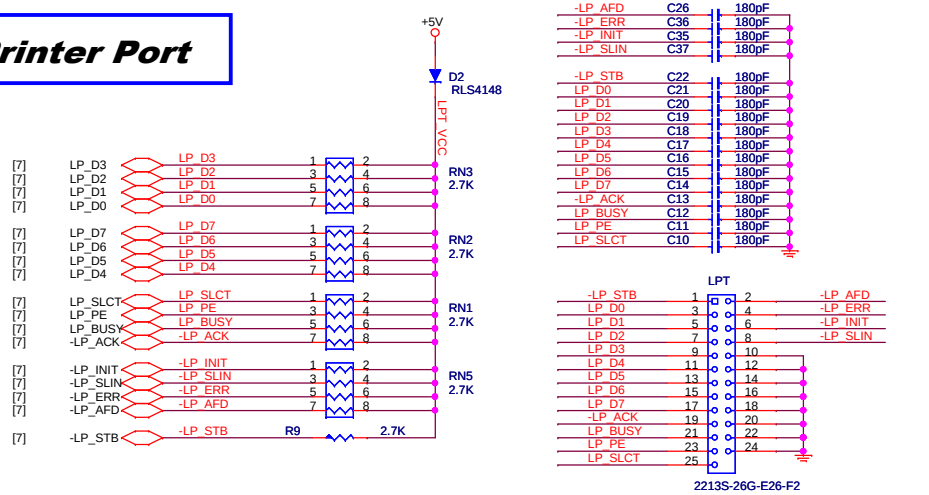
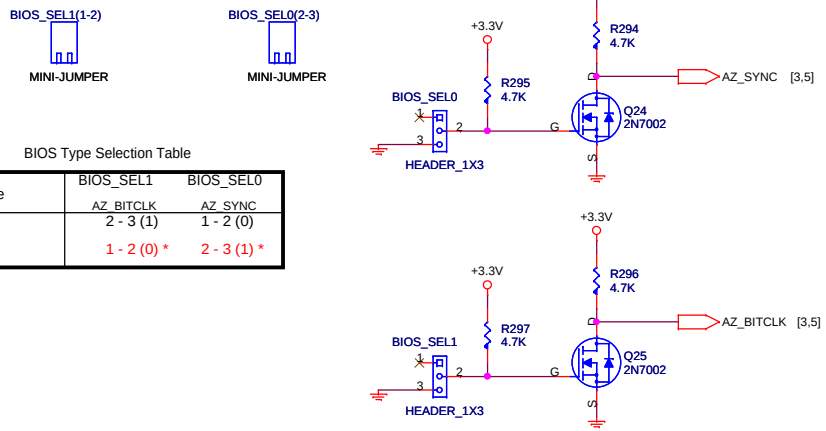
Printer Port

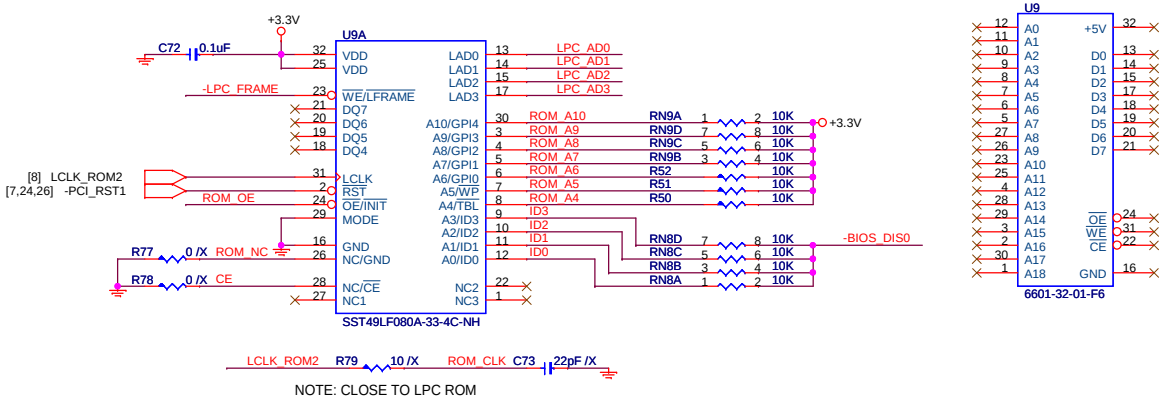




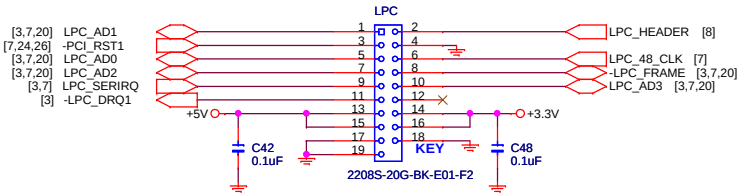
BIOS Type Selection Table

BIOS_Type	BIOS_SEL1 AZ_BITCLK	BIOS_SEL0 AZ_SYNC
SPI BIOS	2 - 3 (1)	1 - 2 (0)
LPC BIOS	1 - 2 (0) *	2 - 3 (1) *

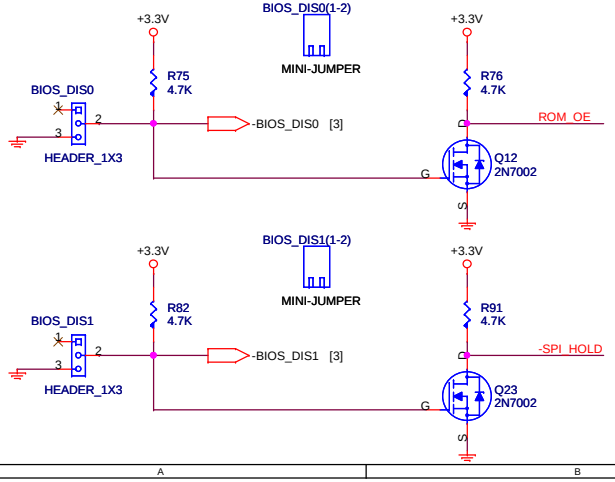
LPC FLASH ROM



LPC HEADER



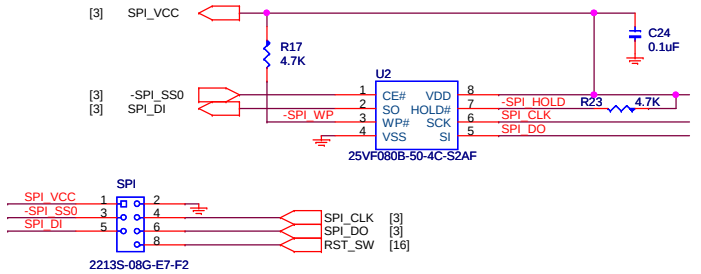
BIOS DISABLE



BIOS Selection Table

BIOS_DISABLE	BIOS_DIS1	BIOS_DIS0
MODULE LPC BIOS	1 - 2 (1) *	1 - 2 (1) *
MODULE SPI BIOS	1 - 2 (1)	2 - 3 (0)
CARRIER LPC BIOS	1 - 2 (1)	2 - 3 (0)
CARRIER SPI BIOS	2 - 3 (0)	1 - 2 (1)

SPI ROM



Pitch 2.54mm

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Title	Printer Port, BIOS & LPC	
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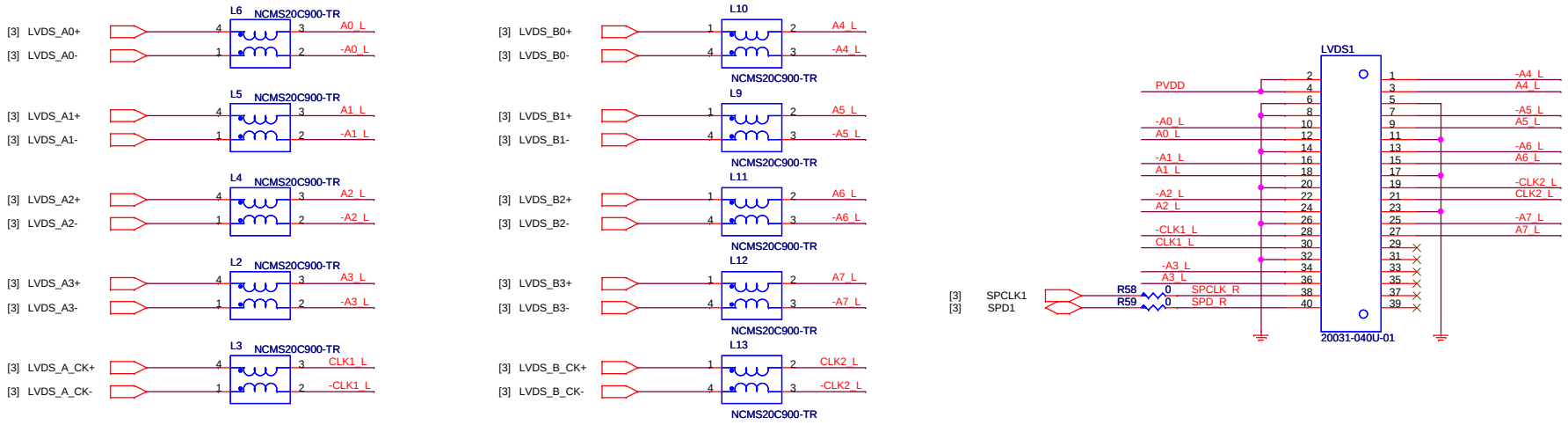
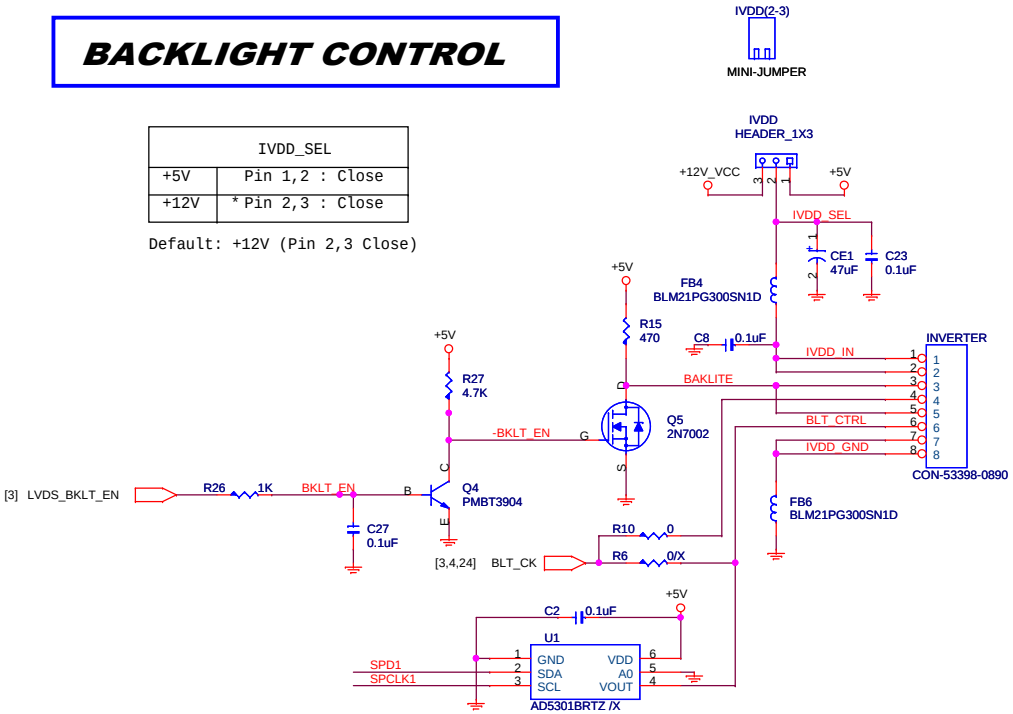
LVDS CONNECTOR



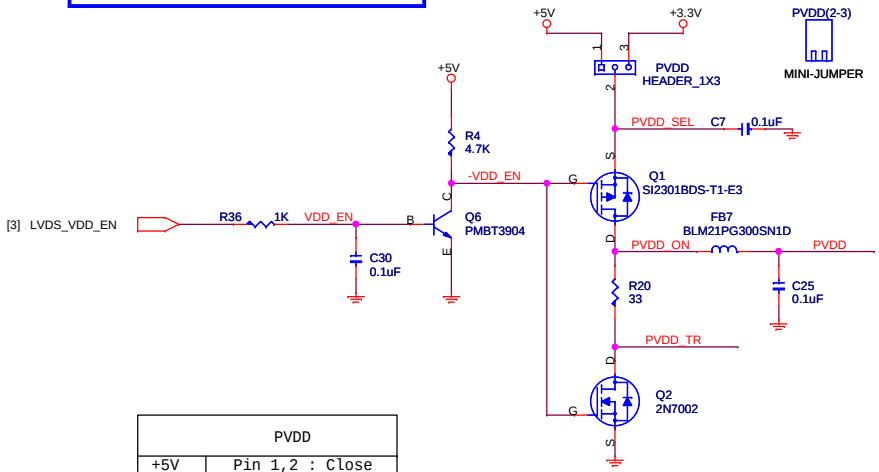
BACKLIGHT CONTROL



IVDD_SEL	
+5V	Pin 1,2 : Close
+12V	* Pin 2,3 : Close

Default: +12V (Pin 2,3 Close)

PANEL POWER



PVDD	
+5V	Pin 1,2 : Close
+3.3V	* Pin 2,3 : Close

Default: +3.3V (Pin 2,3 Close)

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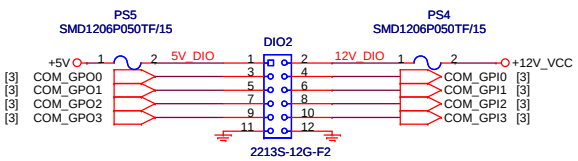
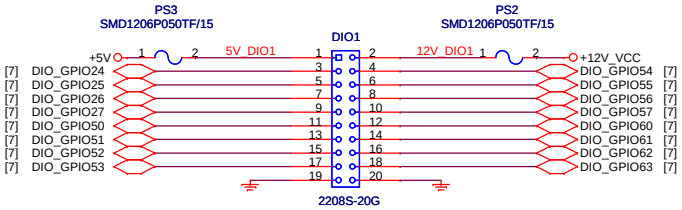
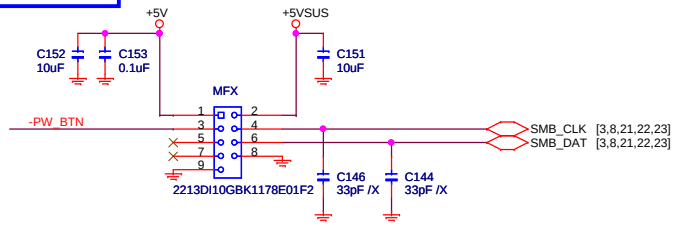
Digital I/O

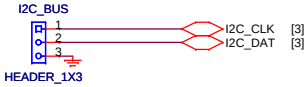




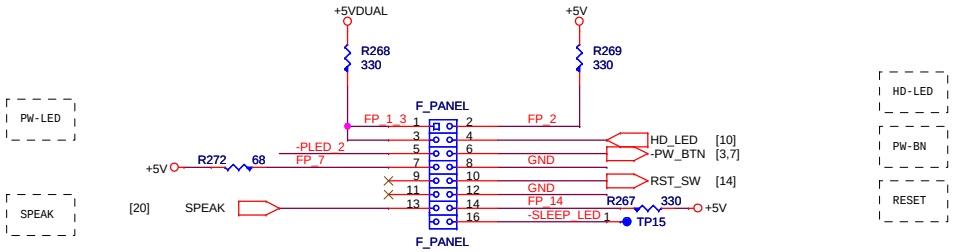
MFX

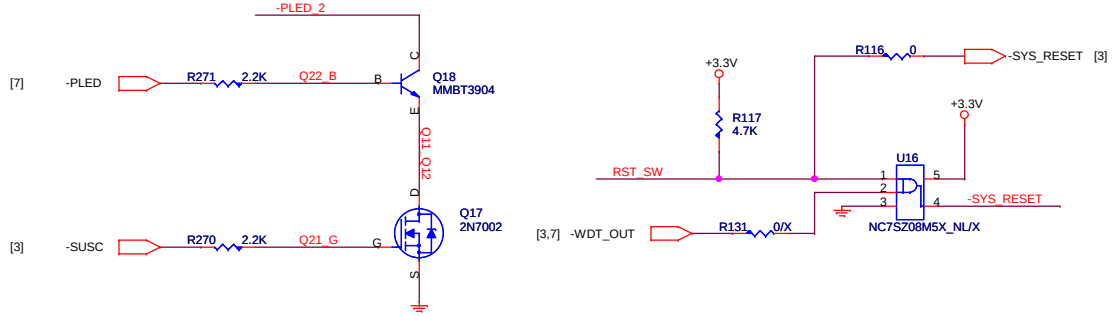


I2C_BUS

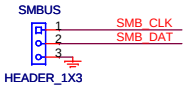


FRONT PANEL

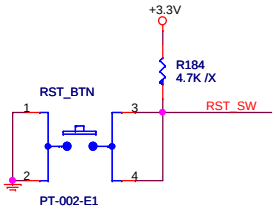




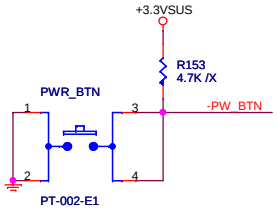
SMBUS



RESET_BTN



PWRBTN



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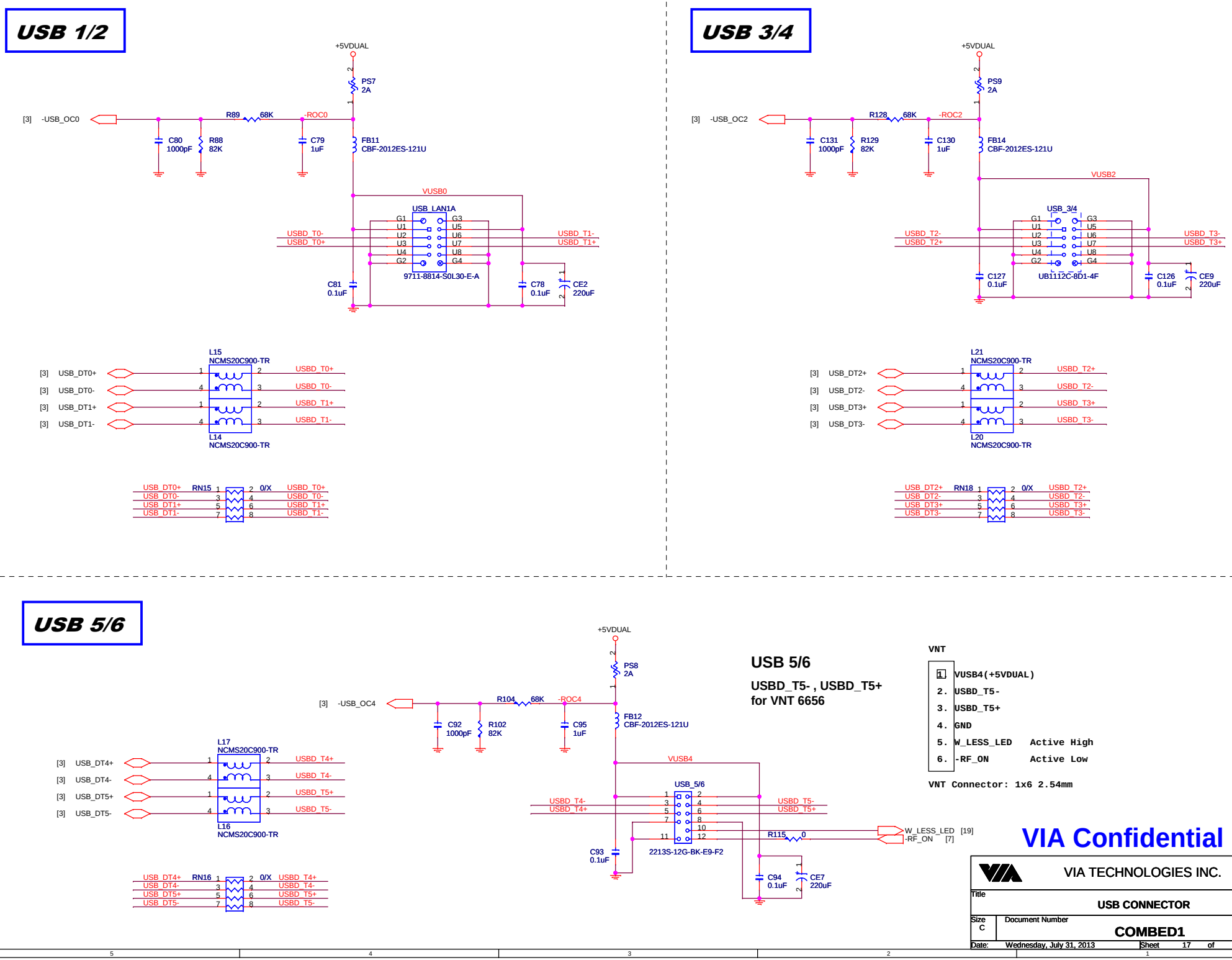
USB 1/2
+5VDUAL
PS7
2A
[3] -USB_OC0
R89 68K -ROC0
C80 1000pF
R88 82K
C79 1uF
FB11 CBF-2012ES-121U
VUSB0
USB_LAN1A
USBD_T0-
USBD_T0+
USBD_T1-
USBD_T1+
9711-8814-S0L30-E-A
C81 0.1uF
C78 0.1uF
CE2 220uF
L15 NCMS20C900-TR
[3] USB_DT0+
[3] USB_DT0-
[3] USB_DT1+
[3] USB_DT1-
L14 NCMS20C900-TR
RN15
0/X
USB_DT0+
USB_DT0-
USB_DT1+
USB_DT1-
USB 3/4
+5VDUAL
PS9
2A
[3] -USB_OC2
R128 68K -ROC2
C131 1000pF
R129 82K
C130 1uF
FB14 CBF-2012ES-121U
VUSB2
USB_3/4
USBD_T2-
USBD_T2+
USBD_T3-
USBD_T3+
UB1112C-8D1-4F
C127 0.1uF
C126 0.1uF
CE9 220uF
L21 NCMS20C900-TR
[3] USB_DT2+
[3] USB_DT2-
[3] USB_DT3+
[3] USB_DT3-
L20 NCMS20C900-TR
RN18
0/X
USB 5/6
+5VDUAL
PS8
2A
[3] -USB_OC4
R104 68K -ROC4
C92 1000pF
R102 82K
C95 1uF
FB12 CBF-2012ES-121U
VUSB4
USB_5/6
USBD_T4-
USBD_T4+
USBD_T5-
USBD_T5+
2213S-12G-BK-E9-F2
R115 0
W_LESS_LED [19]
-RF_ON [7]
C93 0.1uF
C94 0.1uF
CE7 220uF
L17 NCMS20C900-TR
[3] USB_DT4+
[3] USB_DT4-
[3] USB_DT5+
[3] USB_DT5-
L16 NCMS20C900-TR
RN16
0/X
USB 5/6
USBD_T5- , USBD_T5+
for VNT 6656
VNT
1. VUSB4(+5VDUAL)
2. USBD_T5-
3. USBD_T5+
4. GND
5. W_LESS_LED Active High
6. -RF_ON Active Low
VNT Connector: 1x6 2.54mm
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VIA TECHNOLOGIES INC.
Title
USB CONNECTOR
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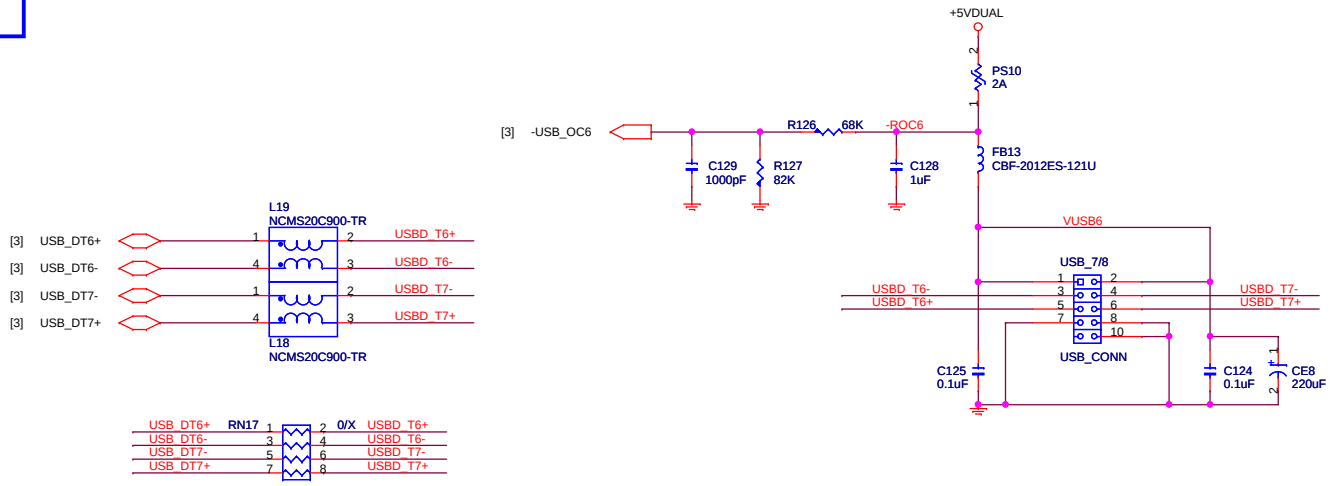
USB 7/8



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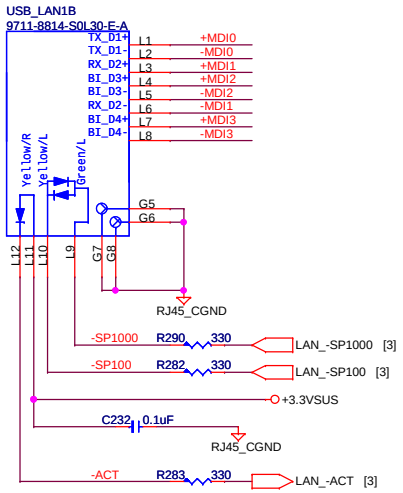
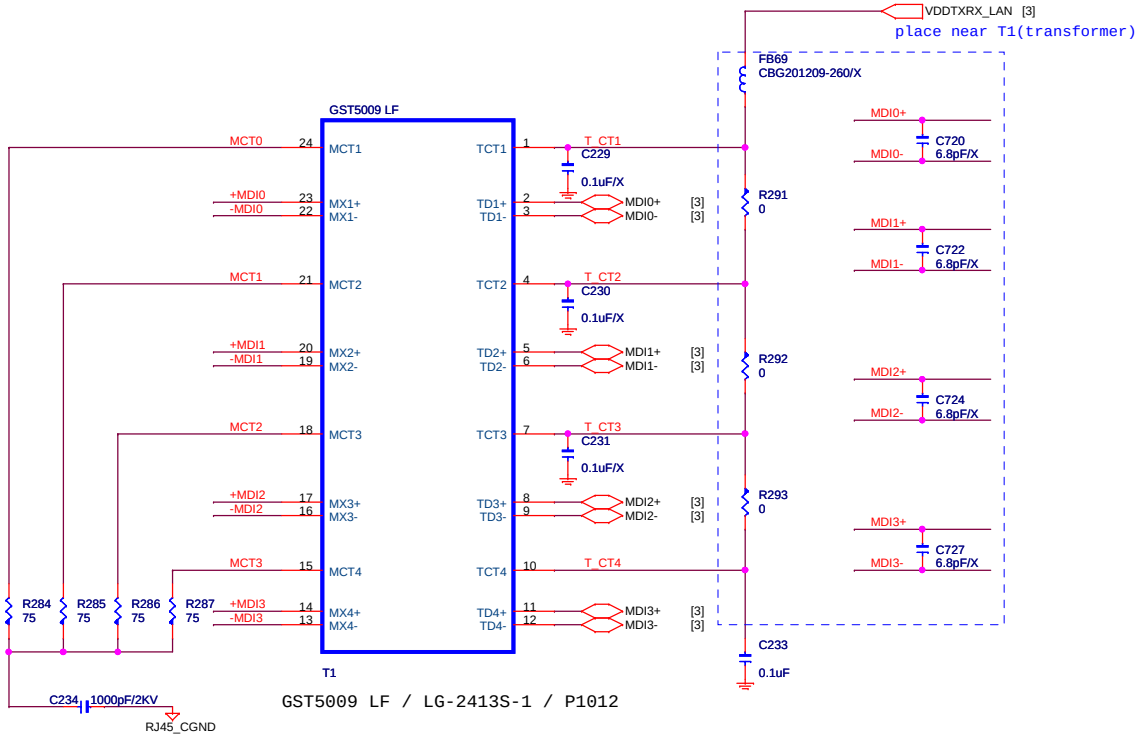
RJ45





GST5009 LF / LG-2413S-1 / P1012

RJ45 Link status GMTI_9711-8814-S0L30-E-A for VT6107

LED Selection	CASE_1
LEDS1,LEDS0	0,1
L10_LED2	Bi-Tripple-color mode {LED2,LED1}=
L9_LED1	01=100M Link(Green) 11=10M Link(Darkless) 00=Link off(Darkless)
L12_LED0	Link/Act (Yellow)

Note: Link: LED on

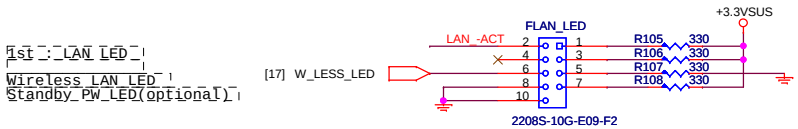
VT6107 T1 install TST1284A LF
VT6122 / RTL8111E T1 install GST5009 LF

T1	VT6107	RTL8111E /VT6122
Bothhand	TST1284A LF 99G26-070542	GST5009 LF 99G26-070532
LANKOM	LF-H6442S-1 99G26-07055F	LG-2413S-1 99G26-07056F
UDE	P1212(007-00) 99G26-07058J	P1012(001-00) 99G26-07053J

	T1	C229,C230	C231	C233	FB69	R291	R292, R293	C720,C722,C724,C727(6.8pFx4)
RTL8111E	GST5009 LF 99G26-070532	X	X	0.01uF	X	0	0	X
VT6107	TST1284A LF 99G26-070542	0	X	X	0	0	X	X
VT6122	GST5009 LF 99G26-070532	0	0	0.1uF	X	X	X	0

O:mount X:unmount

FRONT LAN LED



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Title	RJ45/ LAN LED	
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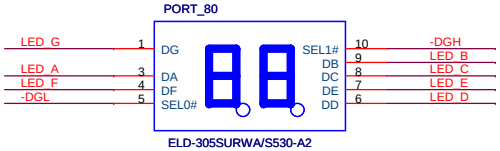
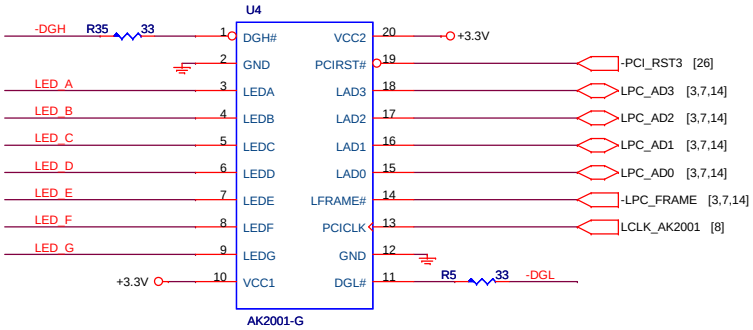
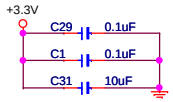
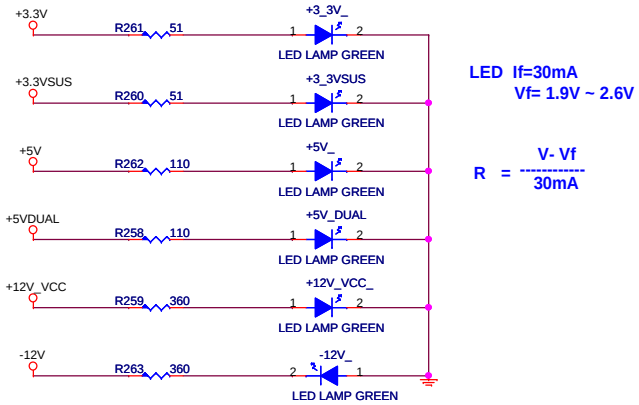
LPC DEBUG PORT







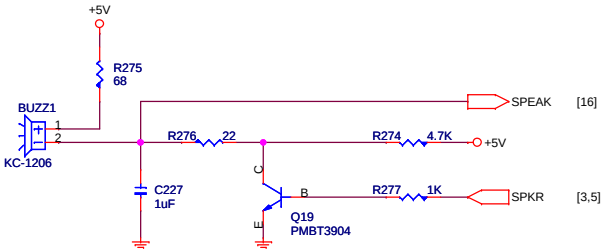
LED



LED If=30mA
Vf= 1.9V ~ 2.6V

$$R = \frac{V - Vf}{30mA}$$

BUZZER



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Title: LPC Debug Port & LED		
Size: C	Document Number: COMBED1	Rev: A1
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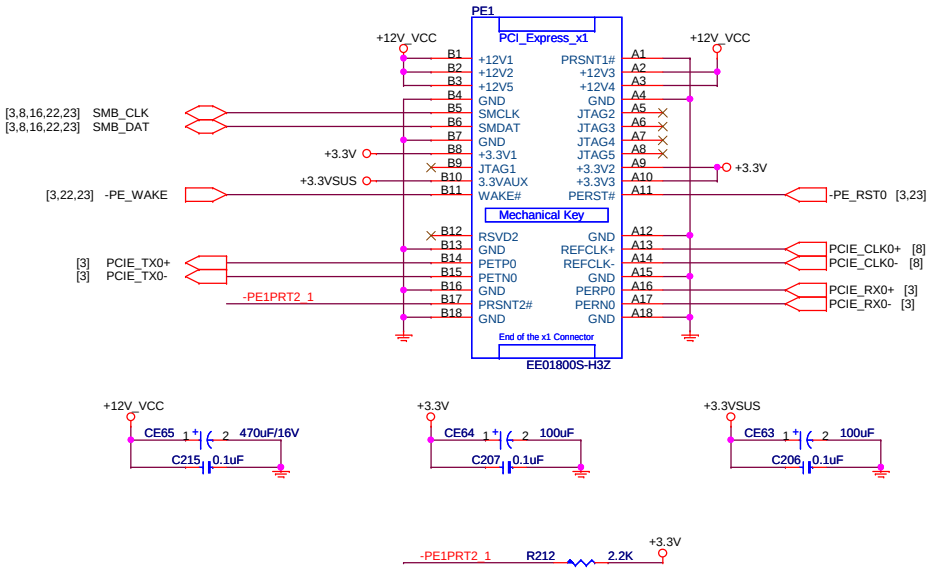
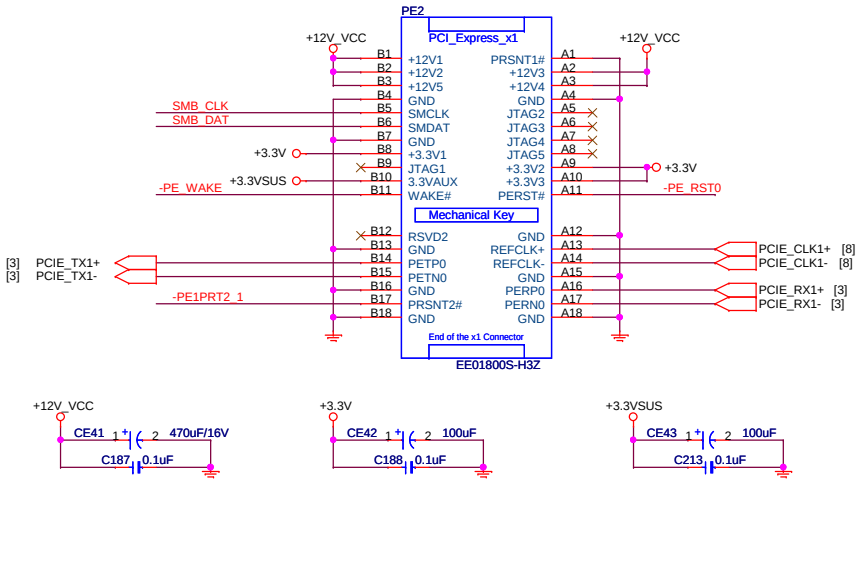
#1 PCIE X 1



#2 PCIE X 1



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Title	PCI Express x1	
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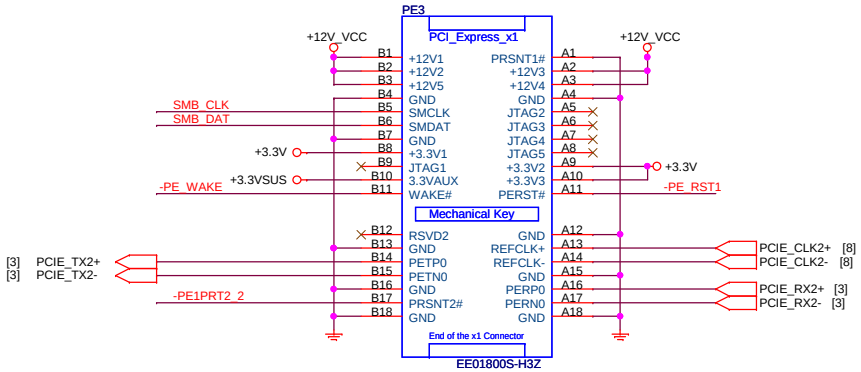
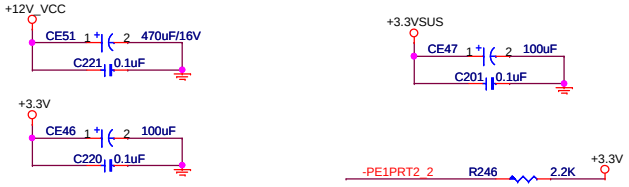
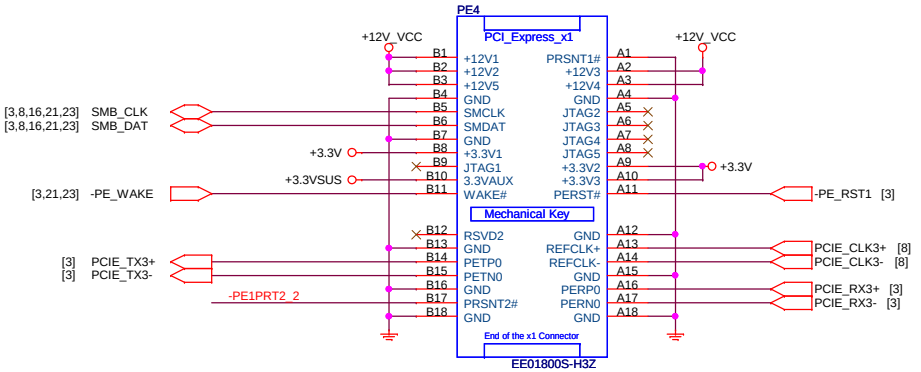
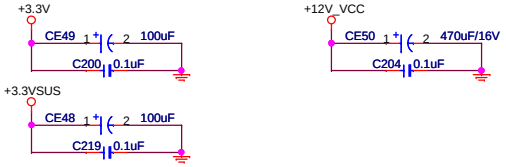
#3 PCIE X 1



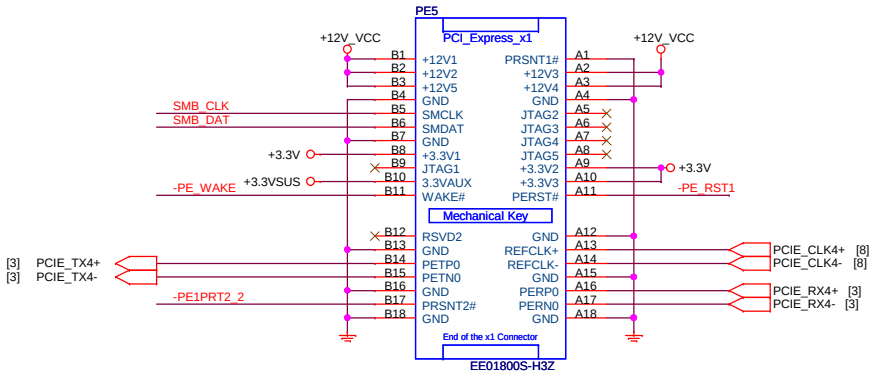


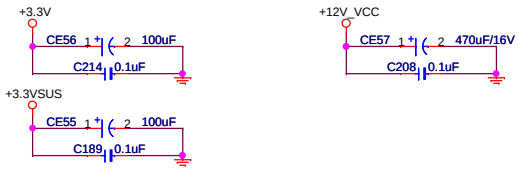
#4 PCIE X 1





#5 PCIE X 1





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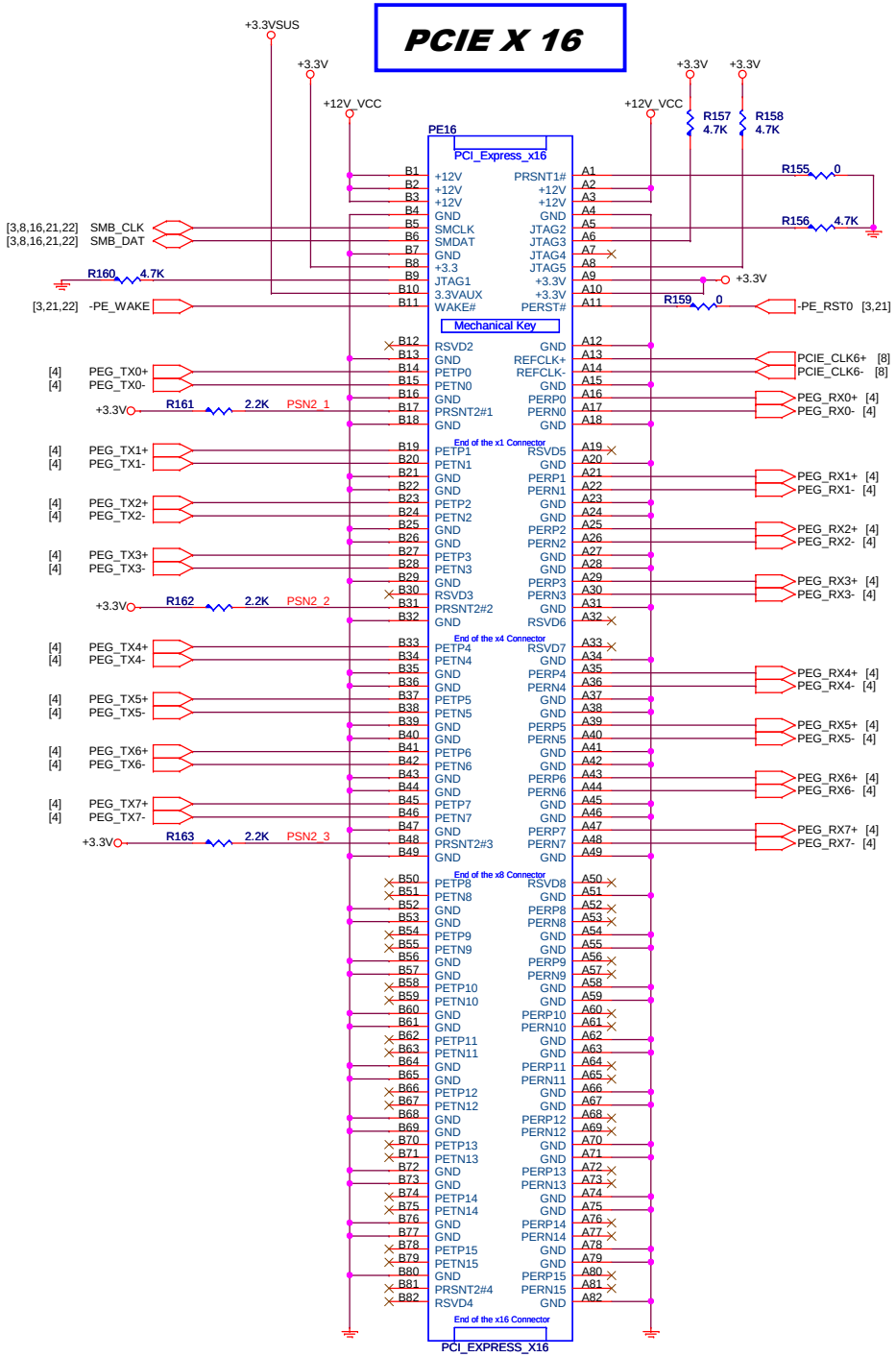
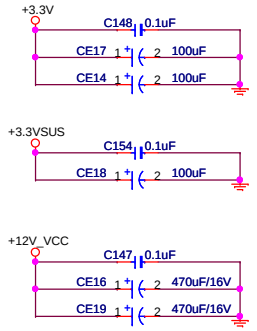
PCIE X 16





Close PCI Express x16 Slot

PCI Express x16, +12V 300mil width.

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Title	PCI Express x16	
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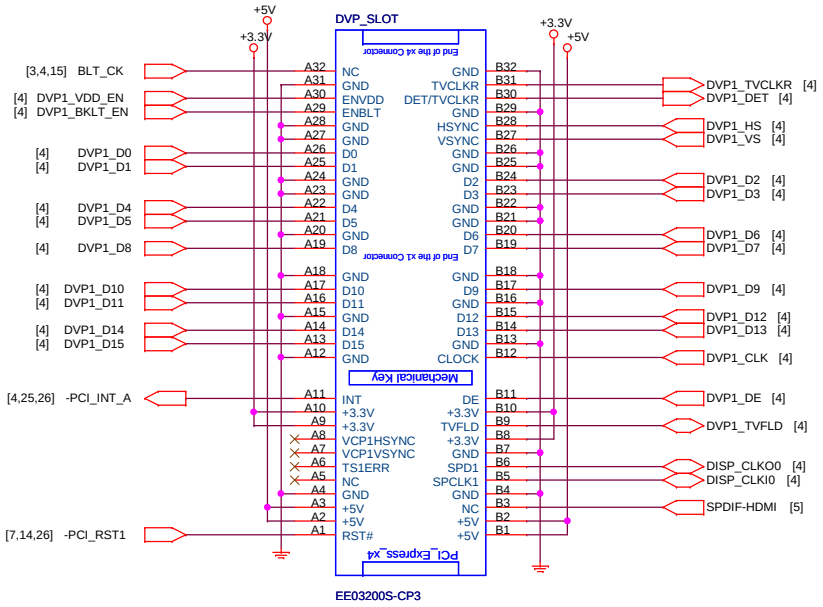
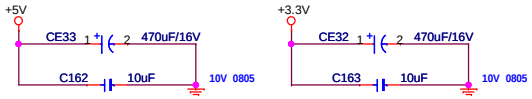
DVP SLOT





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VIA TECHNOLOGIES INC.		
Title: DVP SLOT		
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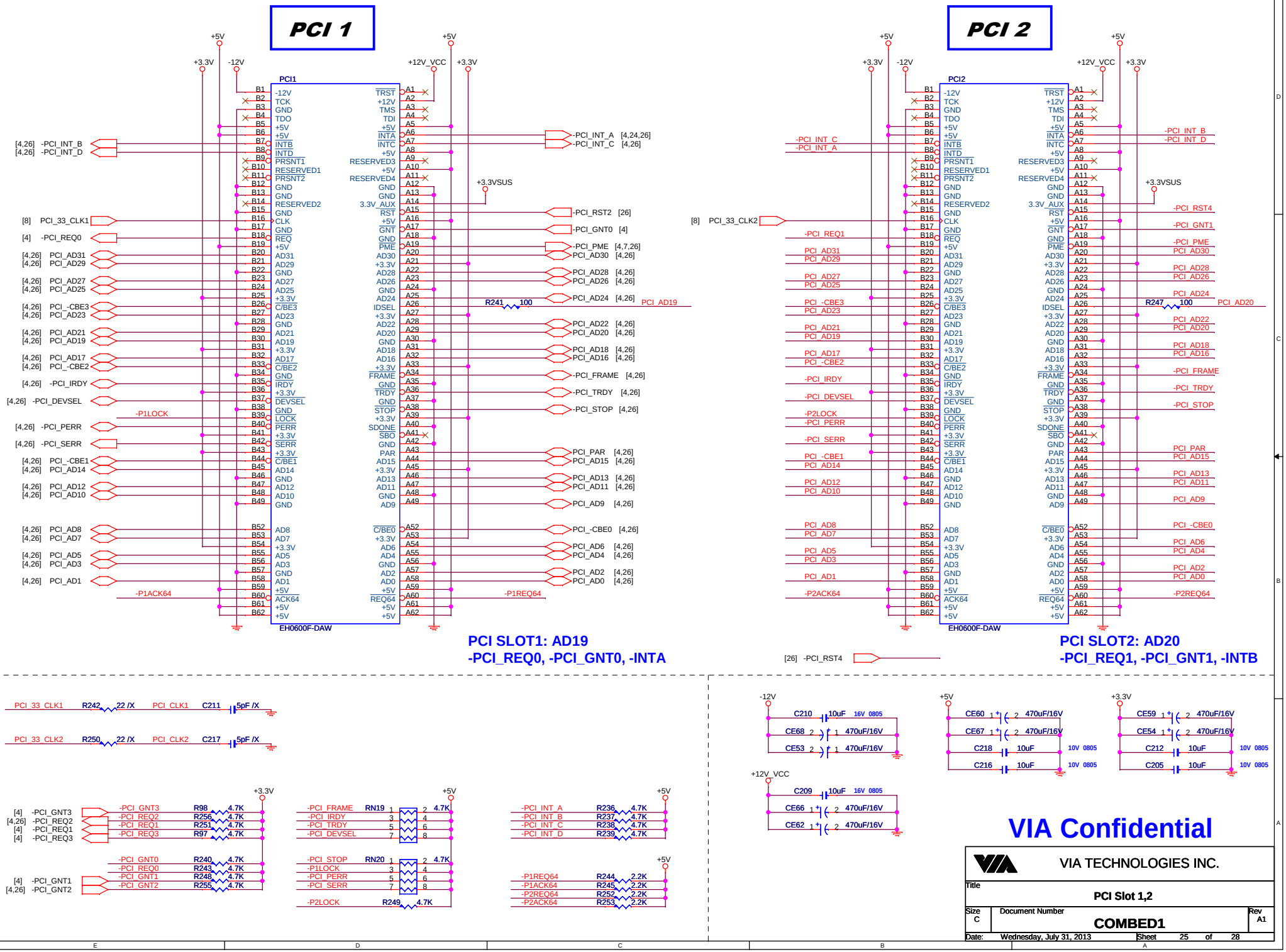
PCI 1
PCI1
EH0600F-DAW
PCI SLOT1: AD19
-PCI_REQ0, -PCI_GNT0, -INTA
PCI 2
PCI2
EH0600F-DAW
PCI SLOT2: AD20
-PCI_REQ1, -PCI_GNT1, -INTB
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VIA TECHNOLOGIES INC.
Title
PCI Slot 1,2
Size C
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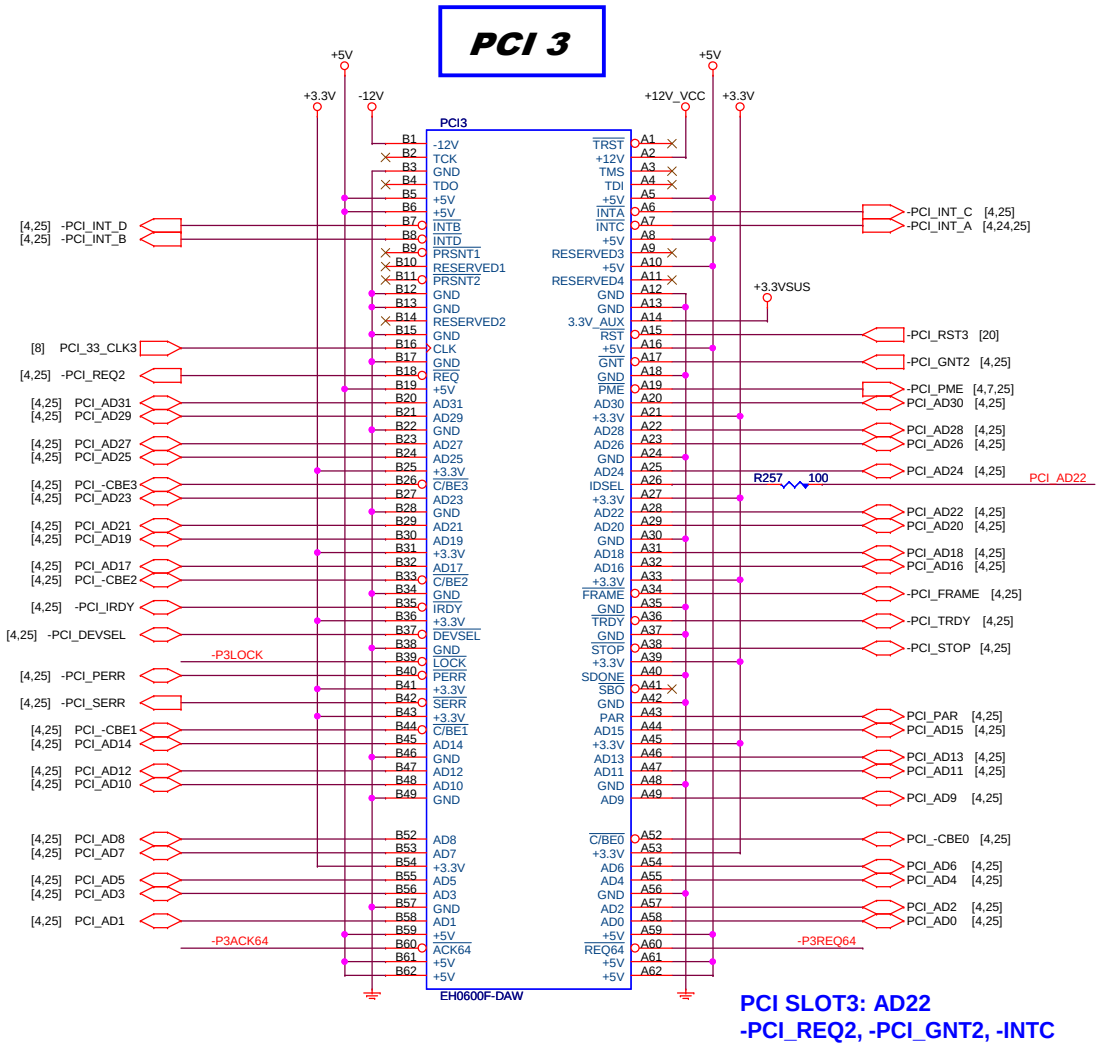

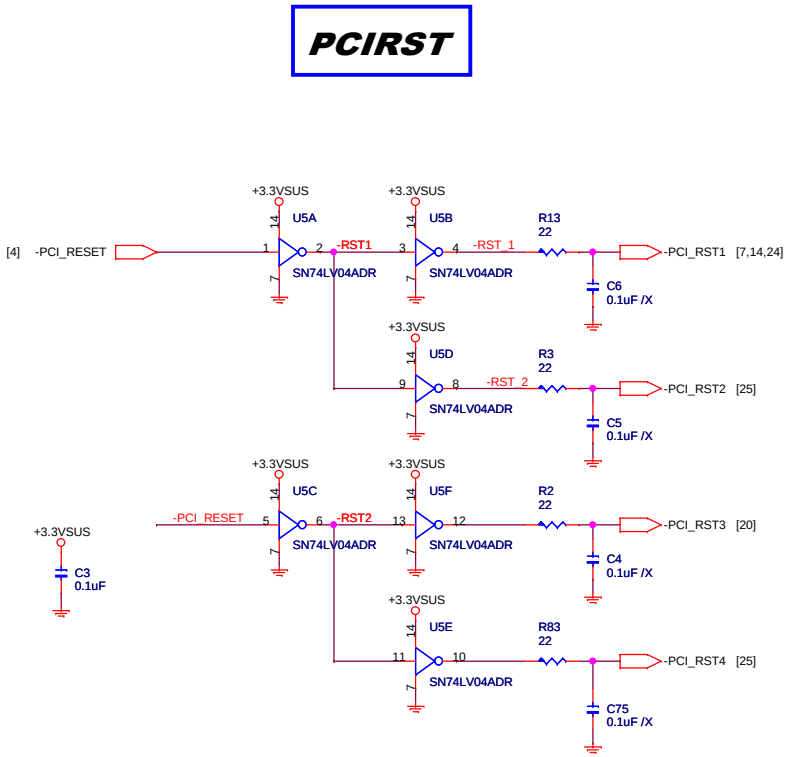

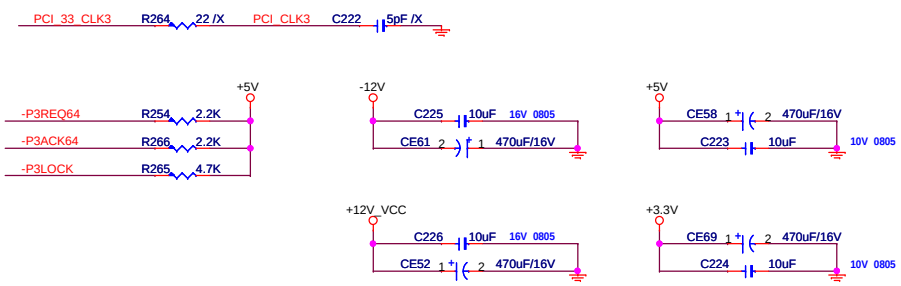

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Title	PCI Slot 3	
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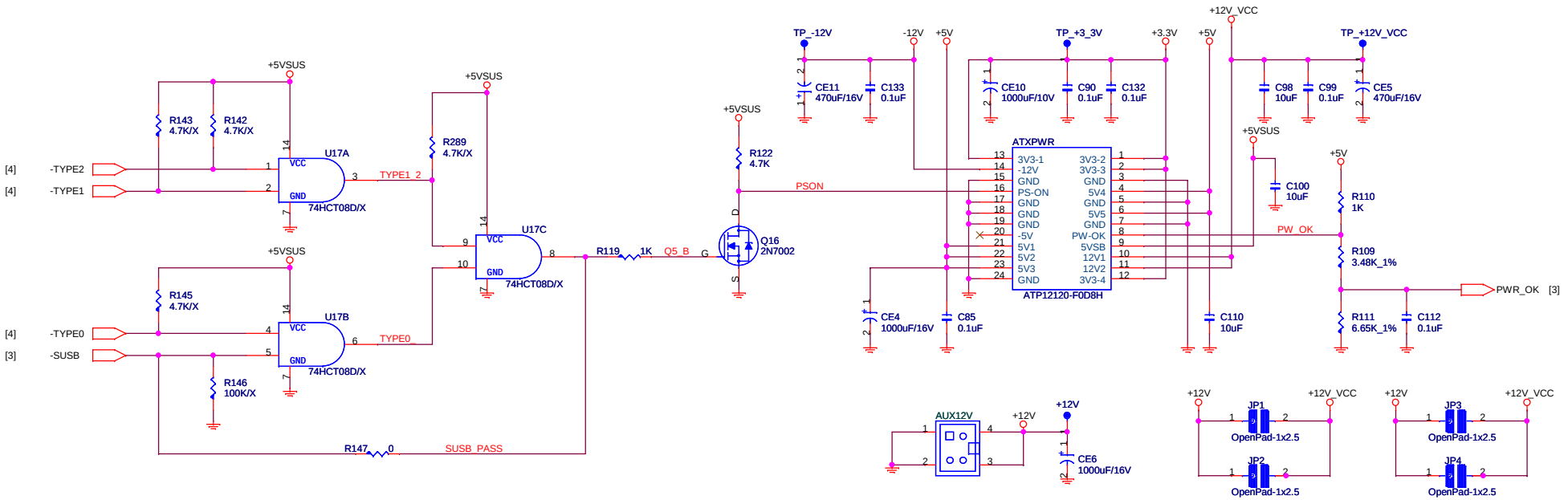
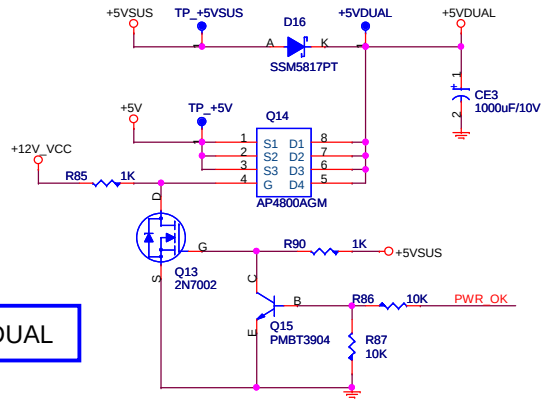
ATX POWER

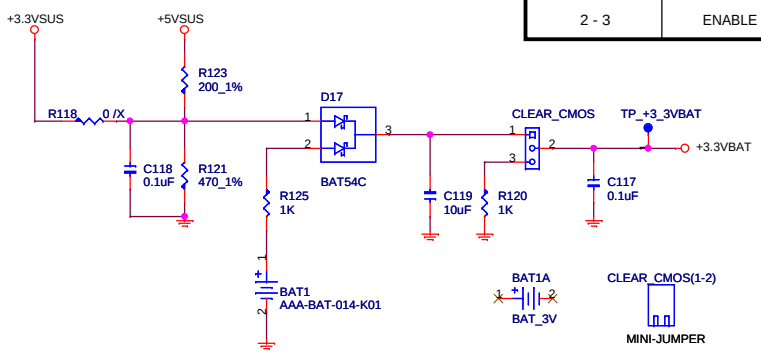


+5VDUAL

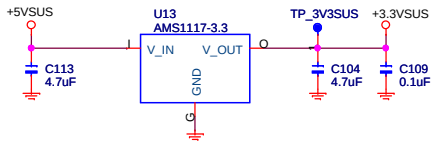


VCC_RTC

CLEAR_CMOS	FUNCTION
* 1 - 2	NORMAL
2 - 3	ENABLE

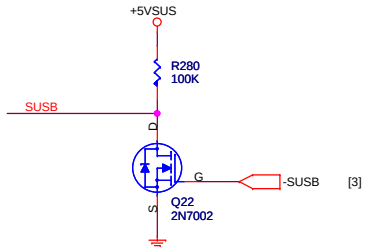


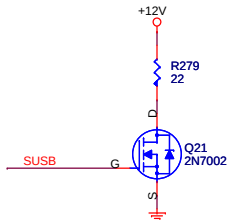
+3.3VSUS

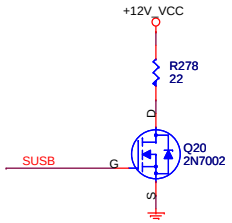


-SUSB	-SUSC	Pstate
0	0	S4/S5
0	1	S3
1	1	S1

Discharge Circuit







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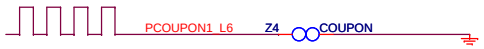
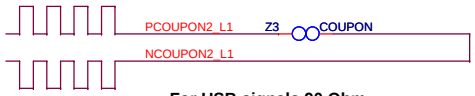
TEST COUPON

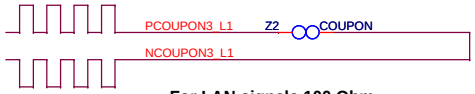


For single end signals 55 Ohm +- 15 Ohm impedance 5 mils

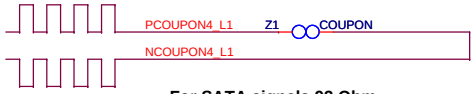
DIFFERENTIAL TRACE SIGNALS



For USB signals 90 Ohm impedance(6:7:6)

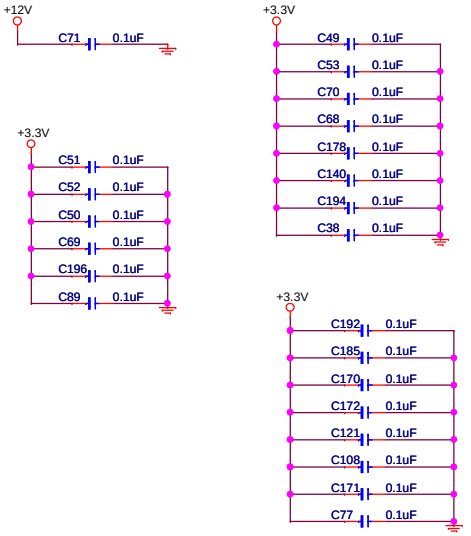


For LAN signals 100 Ohm impedance(5:8:5)

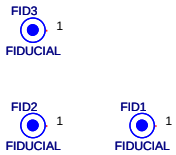


For SATA signals 93 Ohm impedance(6:8:6)

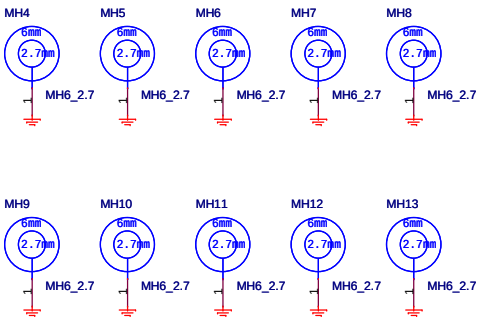
For EMI

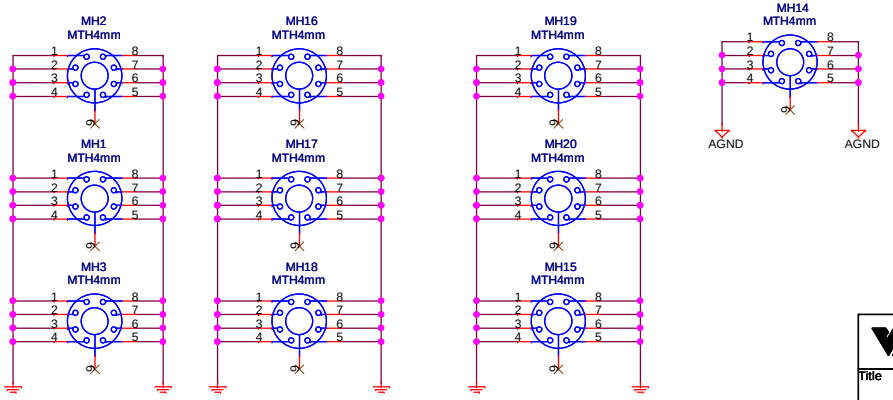


FIDUCIAL MARK



FOR COM EXPRESS MODULE





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