



DESIGN GUIDE

Carrier Board

for SOM-6X50 Module

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Revision History

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1. Introduction

This document provides design guidelines and rule recommendations for the developers of a carrier board that supports the features of the VIA SOM-6X50 module. This document includes the layout and routing guidelines for general board designs and major underlying interfaces (e.g. HDMI, Ethernet, USB). In addition, the document includes the placement and mechanical information on the SOM DDR3 SODIMM slot which is used to provide high-speed interfaces between the carrier board and the module.

Please note that this document is considered to be a reference guide only. This document is not intended to be a specification. All information and examples listed below are considered to be accurate as of the publication date. However, developers must be aware that this document is only a reference guide.

1.1 Document Overview

A brief description of each chapter is given below.

Chapter 1: Introduction

This chapter briefly introduces the structure of the design guide document.

Chapter 2: General Carrier Board Recommendations

The general design schemes and recommended layout rules are shown in this chapter.

Chapter 3: SOM-6X50 Module and SOM DDR3 SODIMM Slot Specification Overview

Detailed information about the SOM-6X50 module and SOM DDR3 SODIMM slot placement and dimensions are described in this chapter.

Chapter 4: Layout and Routing Recommendations

Detailed layout and routing guidelines for each major interface are described in this chapter.

Appendix A: Carrier Board Reference Schematics

Reference schematics of the SOMDB1 evaluation carrier board.

1.2 Acronyms Used

Term	Description
ASIC	Application-specific Integrated Circuit
DDR	Double Data Rate
EMI	Electromagnetic Interference
ESD	Electrostatic-discharge
GPIO	General Purpose Input/Output
HDMI	High-Definition Multimedia Interface
I ² C	Inter-IC
IC	Integrated Circuit
LCD	Liquid-Crystal Display
LVDS	Low-Voltage Differential Signaling
P2P	Point-to-Point
PCB	Printed Circuit Board
RGB	Red, Green and Blue
RJ-45	Registered Jack 45
RS-232	Recommend Standard number 232
SD	Secure Digital
SODIMM	Small Outline Dual In-line Memory Module
SMT	Surface Mount Technology
SOM	System-On-Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USB OTG	USB On-The-Go

Table 1: Acronyms used

1.3 Schematic Conventions

The reference schematics depicted in this document show the directional flow of the signals. Directional flow is indicated by the pointed ends of the arrow shapes.

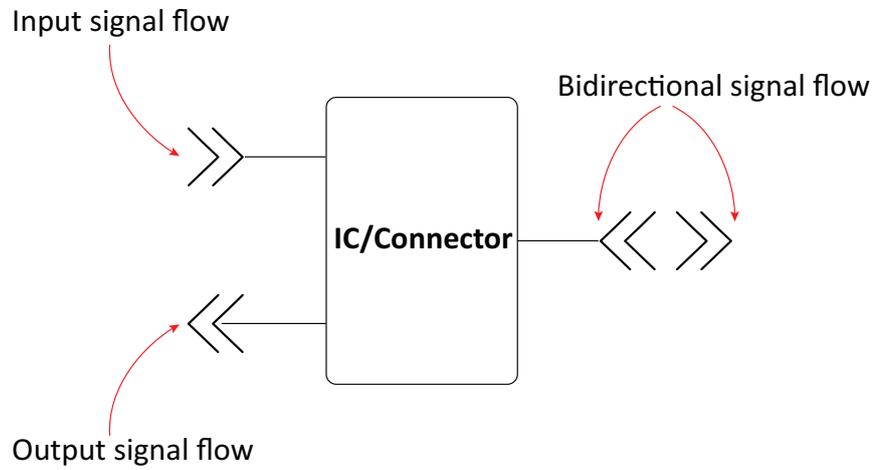


Figure 1: Schematic conventions

2. General Carrier Board Recommendations

This section contains general guidelines for the PCB stackup and the layout of traces. The general guidelines for routing style, topology, and trace attribute recommendations are also discussed.

2.1 PCB Stackup

The PCB stackup consists of signal layers and reference layers (power and ground). The signal layers are referred to as the component layer (top), inner layer and solder layer (bottom).

The carrier board designers can choose between two basic categories of PCB stackup design: microstrip and stripline. The microstrip designs have the outer signal layers exposed. The stripline designs have the outermost signal layers shielded by reference layers.

The following figures show an example of microstrip and stripline designs.

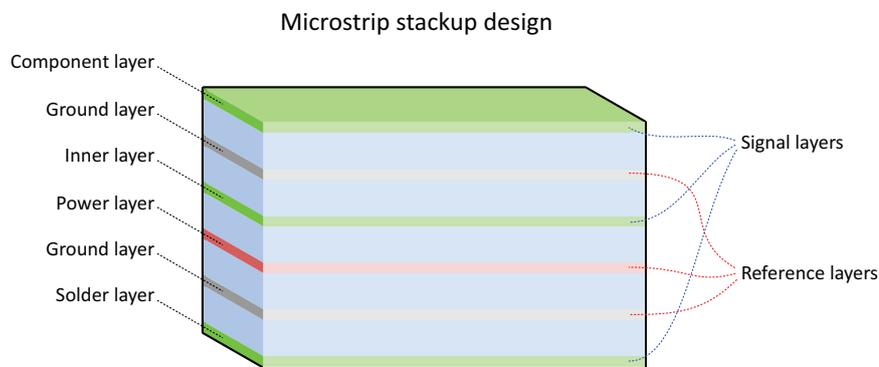


Figure 2: Microstrip PCB stackup example

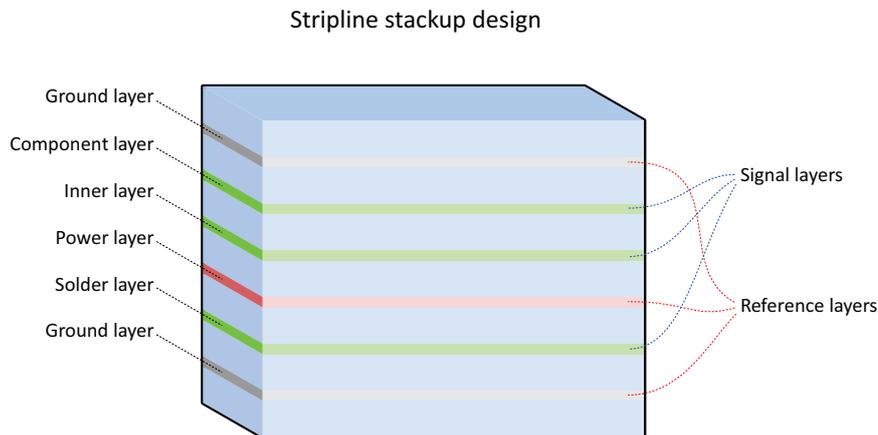


Figure 3: Stripline PCB stackup example

The choice of microstrip or stripline design depends on the application for which the carrier board is being designed. If the carrier board is being designed for locations where sensitivity to EMI is an issue, a stripline design is recommended for reducing EMI and noise coupling. For applications where the tolerance for EMI levels is greater, a microstrip design is recommended to reduce costs. Due to the inherent nature of stripline PCB stacks, broad-side coupling is possible.

2.1.1 4-Layer PCB Stackup Example

The following figure shows the recommended 4-layer PCB stackup design for the carrier board of the SOM-6X50 module.

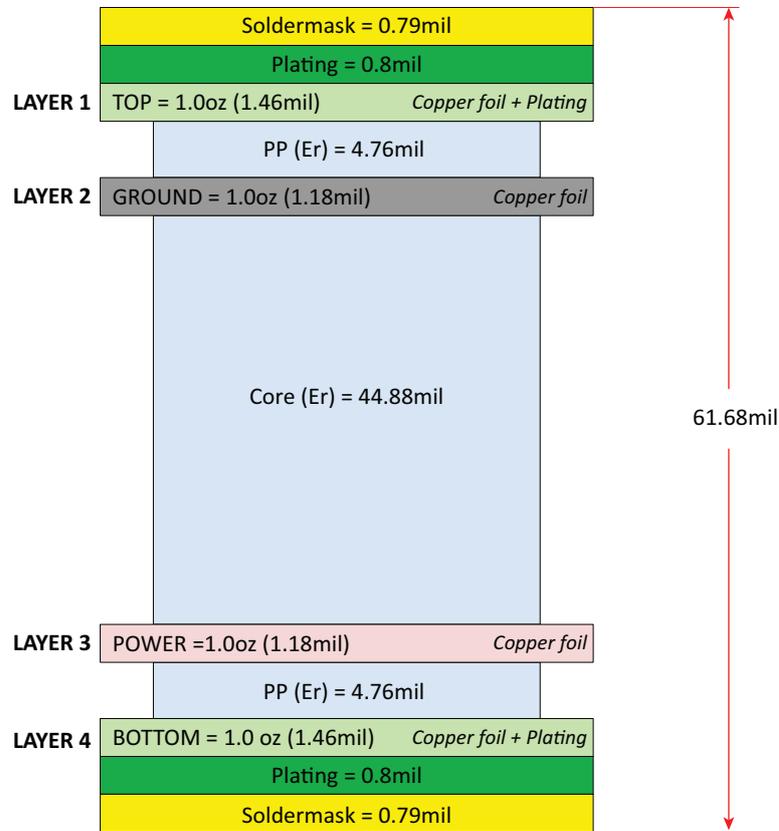


Figure 4: 4-Layer PCB board stackup detail

2.1.2 4-Layer PCB Impedance Control

± 10%	40Ω Single-end	50Ω Single-end	55Ω Single-end	85Ω Differential	90Ω Differential	90Ω Differential
Layer 1	12mil	8mil	7mil	7.8 : 9 : 7.8 mil	7.6 : 8 : 7.6 mil	7 : 7.5 : 7 mil
Layer 4	12mil	8mil	7mil	7.8 : 9 : 7.8 mil	7.6 : 8 : 7.6 mil	7 : 7.5 : 7 mil

Table 2: 4-Layer PCB impedance control

2.2 General Layout and Routing Guidelines

This section provides general layout rules and routing guidelines for designing carrier boards of SOM-6X50 module.

2.2.1 Routing Styles and Topology

Topology is the physical connectivity of a net or a group of nets. There are two types of topologies for a carrier board layout: point-to-point (P2P) and multi-drop. An example of these topologies is shown in Figure 5.

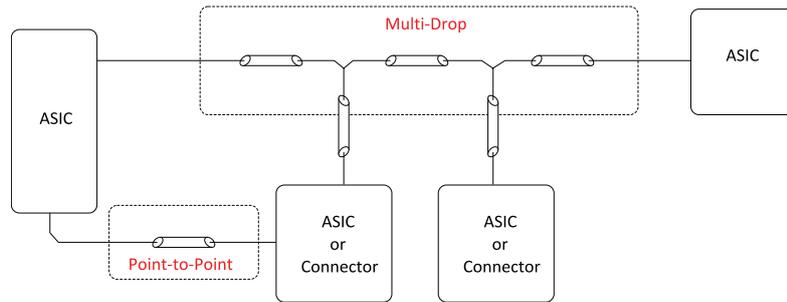


Figure 5: Point-to-point and multi-drop examples

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept as short as possible (less than 1.5”). Therefore, daisy chain style routing is strongly recommended for these signals. Figure 6 below shows an example of daisy chain routing.

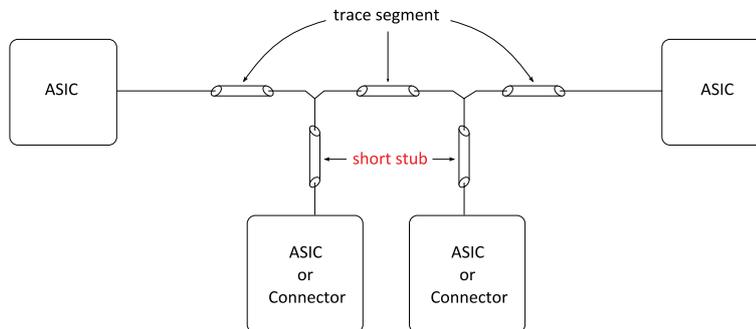


Figure 6: Daisy-chain example

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 7. In this case, the branch point is somewhere between both ends. It may be near the source or near the loads, but being close to the load side is best. The separated traces should be equal in length.

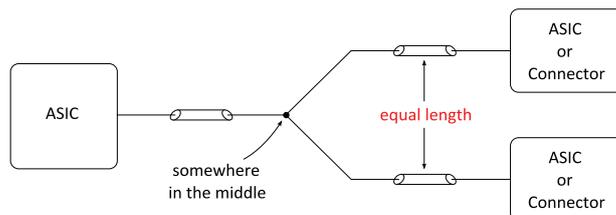


Figure 7: Alternate multi-drop example

2.2.2 General Trace Attribute Recommendation

A 5mil trace width and 10mil spacing are generally advised for most signal traces on a carrier board layout. To reduce trace inductance the minimum power trace width is recommended to be 30mil.

As a quick reference, the overall recommended trace width and spacing for different trace types are listed in Table 3, and the recommended trace width and spacing for each signal group is shown in Chapter 4.

Trace Type	Trace Width (mil)	Spacing (mil)
Regular Signal	5 or wider	10 or wider
Interface or Bus Reference Voltage Signal	20 or wider	20 or wider
Power	30 or wider	20 or wider

Table 3: Recommended trace width and spacing

General rules for minimizing crosstalk in high-speed bus designs are listed below:

- Maximize the distance between traces. Maintain 10mil minimum spaces between traces wherever possible.
- Maximize the distance (30mil minimum) between two adjacent routing areas of different signal groups wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Provide stable reference planes for all high-speed signals.
- Never route high-speed signals over splits in their perspective reference planes.
- Select a board stack-up that minimizes coupling between adjacent traces.

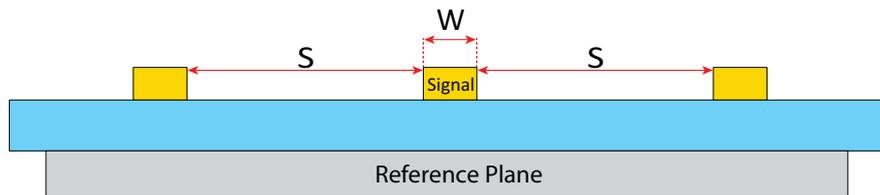


Figure 8: Signal trace width and spacing example

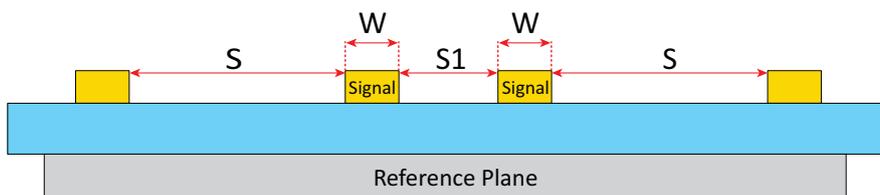


Figure 9: Differential signal trace width and spacing example

Notes:

1. W: Trace width
2. S: The spacing to other traces
3. S1: Differential pair spacing

2.2.3 General Clock Routing Considerations

The clock routing guidelines are listed below:

- The recommended clock trace width is 5mil.
- The minimum space between one clock trace and adjacent clock traces is 20mil. The minimum space from one segment of a clock trace to other segments of the same clock trace is at least two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 10).
- The clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 11).
- The series terminations (damping resistors) are needed for all clock signals (typically 0Ω to 47Ω). When two loads are driven by one clock signal, the series termination layout is shown in Figure 12. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20mil to 50mil wide) is preferred.
- No clock traces on the internal layer if a six-layer board is used.

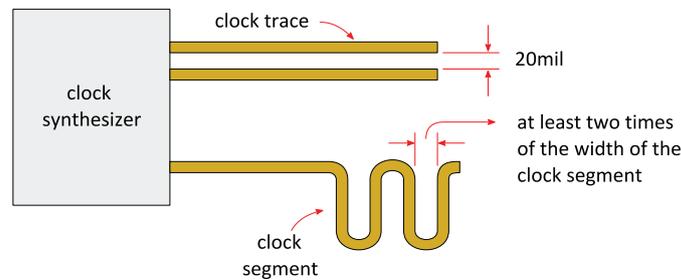


Figure 10: Suggested clock trace spacing

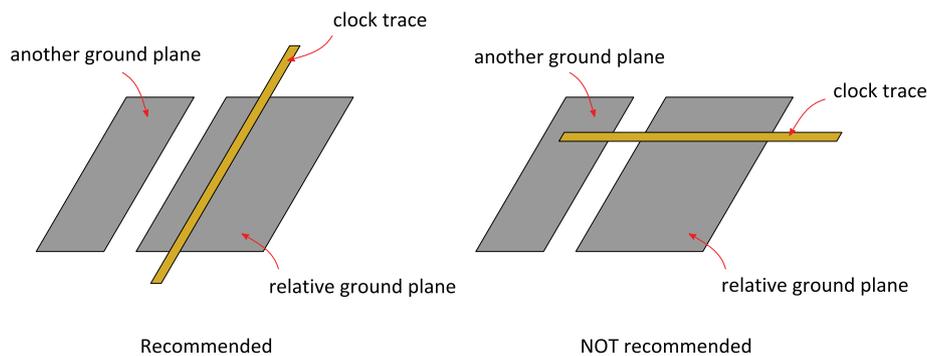


Figure 11: Clock trace layout in relation to the ground plane

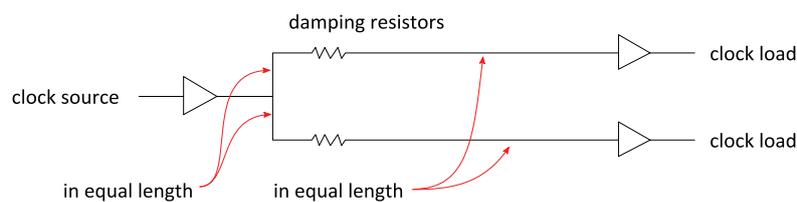


Figure 12: Series termination for multiple clock loads

3. SOM-6X50 Module and SOM DDR3 SODIMM Slot Specification Overview

3.1 SOM-6X50 Module Placement

The following figure shows the depiction of the top view of the carrier board PCB (SOMDB1) with the appropriate amount of space reserved for the SOM-6X50 module.

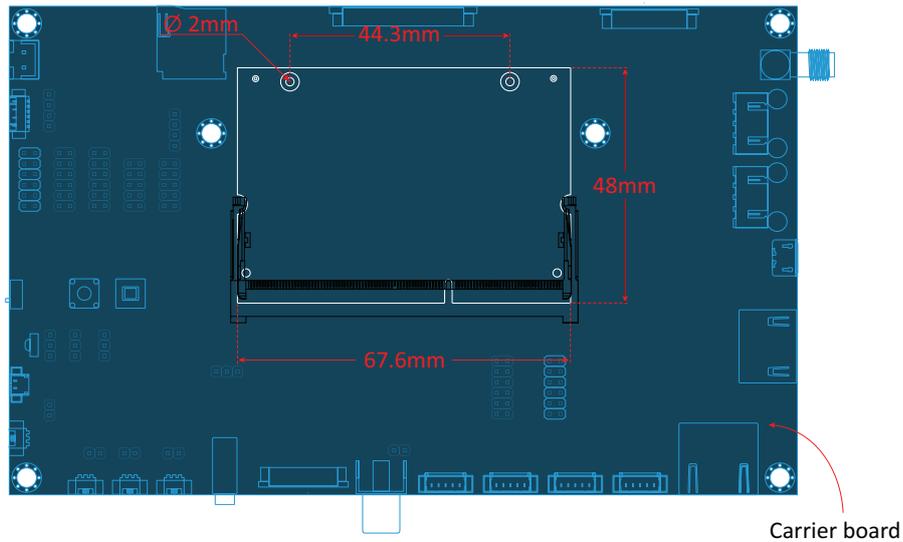


Figure 13: SOM-6X50 module placement example on the carrier board

3.2 SOM-6X50 Module Mechanical Characteristics

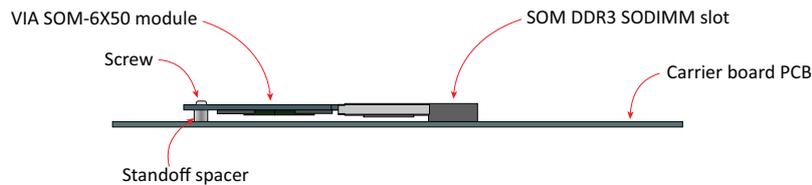


Figure 14: Carrier board with SOM-6X50 module (side view)

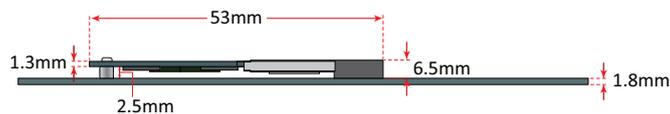


Figure 15: Carrier board and SOM-6X50 module height distribution (side view)

3.3 SOM-6X50 Module and Carrier Board Dimensions

The following figures show the mechanical dimensions of the SOM-6X50 module and the reference carrier board (SOMDB1).

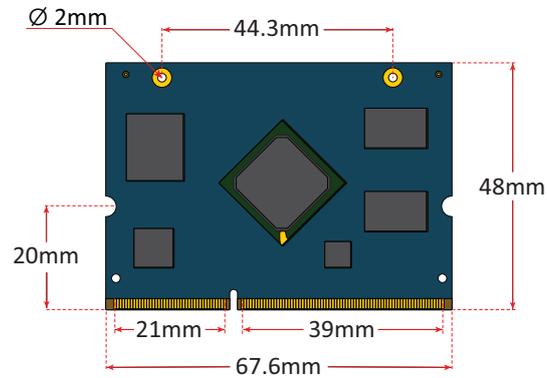


Figure 16: Dimensions of the SOM-6X50 module

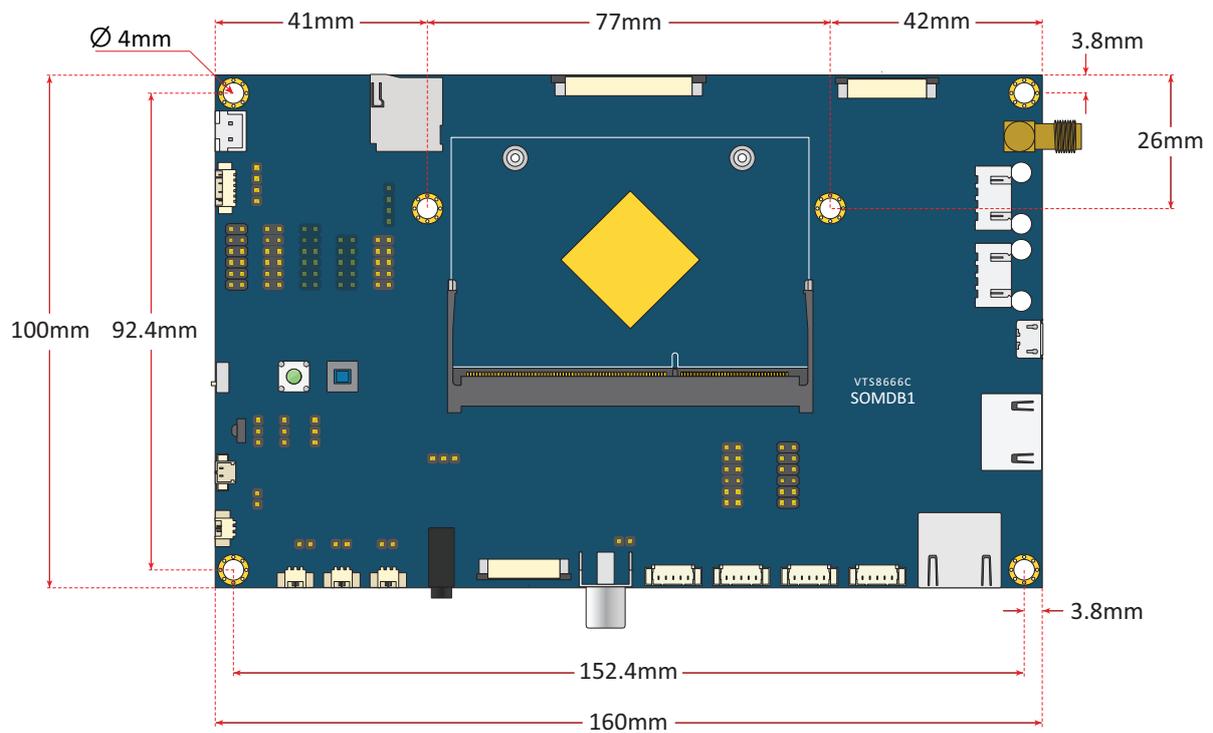


Figure 17: Dimensions of the reference carrier board

3.4 SOM DDR3 SODIMM Slot

The SOM DDR3 SODIMM slot can handle high-speed signals and comprises 204 pins to connect the SOM-6X50 module. Table 4 shows the specification sample of the SOM DDR3 SODIMM slot.

Part Number	Description	Height	Vendor
40-40024-02	DDR3 SODIMM 5.2H 1.5V STD PLASTIC LATCH ASSEMBLY	5.2mm	Deren

Table 4: SOM DDR3 SODIMM slot sample

3.4.1 SOM DDR3 SODIMM Slot Dimensions

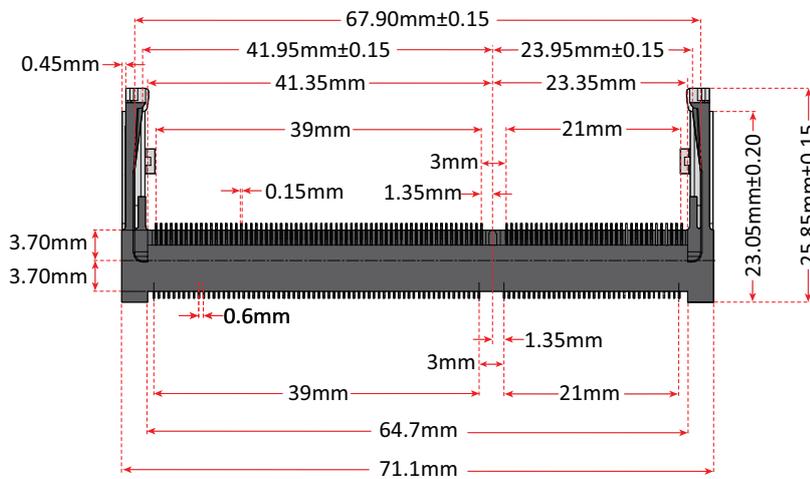


Figure 18: Dimensions of the SOM DDR3 SODIMM slot (top view)

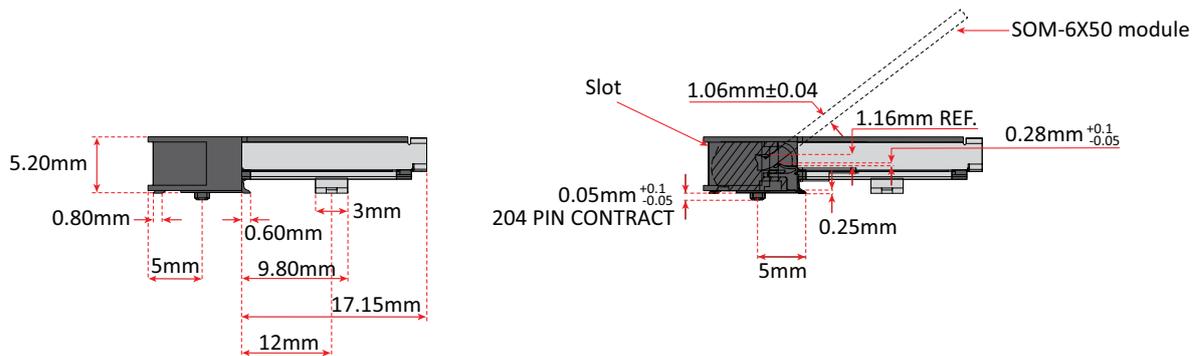


Figure 19: Dimensions of the SOM DDR3 SODIMM slot (side view)

3.4.2 SOM DDR3 SODIMM Slot Footprint

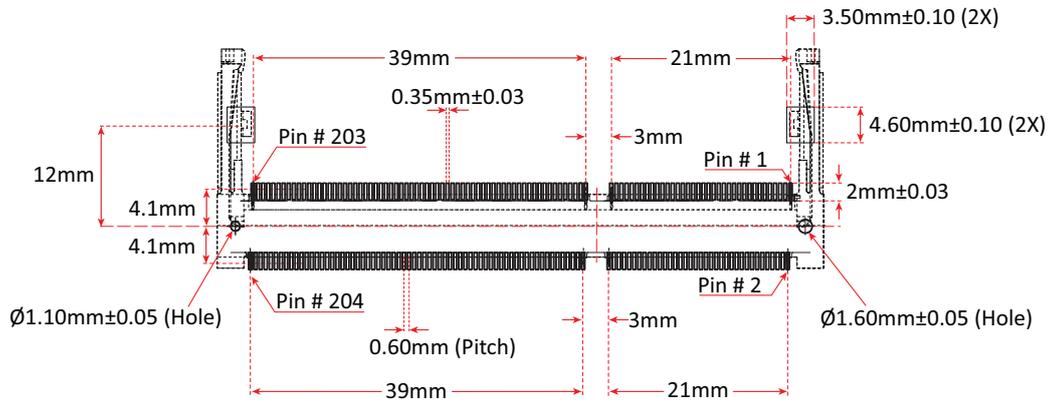


Figure 20: PCB footprint of the SOM DDR3 SODIMM slot

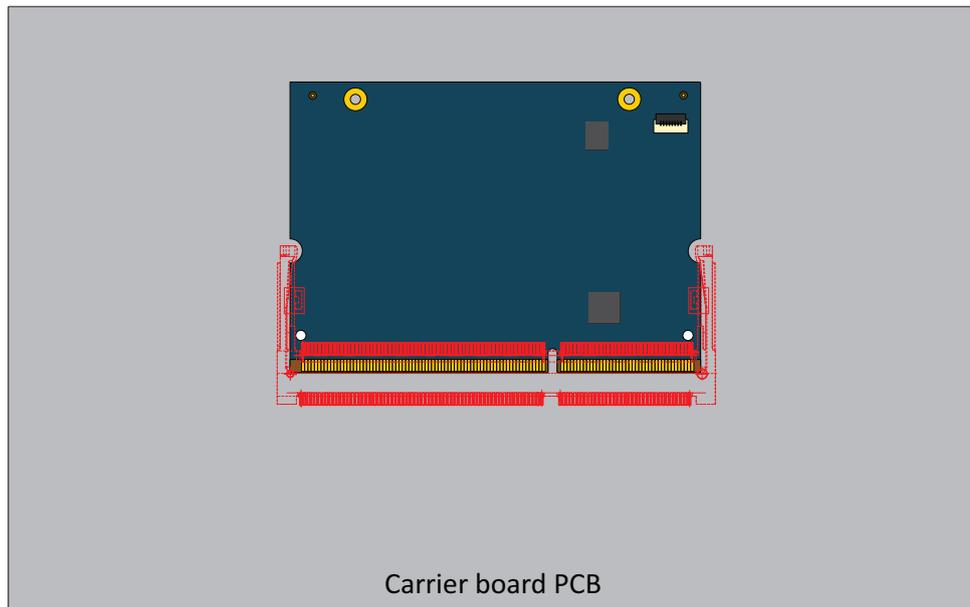


Figure 21: PCB footprint of the SOM DDR3 SODIMM slot with SOM-6X50 module

3.5 SOM DDR3 SODIMM Slot Pin Assignments

The SOM DDR3 SODIMM slot consists of 204 pins. The pinouts of the SOM DDR3 SODIMM slot are shown below.

Pin	Signal	Pin	Signal
1	USBATTA0	2	GND
3	USBID0	4	nUSBH2+
5	USBSW0	6	nUSBH2-
7	GND	8	GND
9	SPI0MISO	10	nUSBH1+
11	SPI0MOSI	12	nUSBH1-
13	SPI0CLK	14	GND
15	SPI0SS0-	16	nUSBHD0+
17	GND	18	nUSBHD0-
19	SD0CLK	20	GND
21	SD0DATA1	22	UARTB_CTS
23	SD0WP	24	UARTB_RTS
25	SD0DATA0	26	UARTB_RX
27	SD0CMD	28	UARTB_TX
29	SD0DATA2	30	UARTA_CTS
31	SD0DATA3	32	UARTA_RTS
33	SD0PWRSW	34	UARTA_RX
35	SD0CD	36	UARTA_TX
37	MO_LINK	38	UARTC_RTS
39	MO_SPEED	40	UARTC_RX
41	PWMOUT0	42	UARTC_TX
43	PWMOUT1	44	UARTC_CTS
45	GND	46	UARTD_RTS
47	NET_RX-	48	UARTD_CTS
49	NET_RX+	50	UARTD_TX
51	GND	52	UARTD_RX
53	NET_TX-	54	VDHSYNC
55	NET_TX+	56	VDVSYNC
57	GND	58	VDDEN
59	nHDMIHPD	60	VDCLK
61	nHDMICEC	62	VDOUT0
63	nHDMIDDCSDA	64	VDOUT8
65	nHDMIDDCSCL	66	VDOUT1
67	GND	68	VDOUT10
69	nLCD1DO3+	70	VDOUT3
71	nLCD1DO3-	72	VDOUT2
73	GND	74	VDOUT5
75	nLCD1CLK+	76	VDOUT4
77	nLCD1CLK-	78	VDOUT6

Pin	Signal	Pin	Signal
79	GND	80	VDOUT13
81	nLCD1DO0+	82	VDOUT9
83	nLCD1DO0-	84	VDOUT7
85	GND	86	VDOUT15
87	nLCD1DO1+	88	VDOUT11
89	nLCD1DO1-	90	VDOUT12
91	GND	92	VDOUT19
93	nLCD1DO2+	94	VDOUT14
95	nLCD1DO2-	96	VDOUT18
97	GND	98	VDOUT17
99	VDIN0	100	VDOUT20
101	VDIN1	102	VDOUT21
103	VDIN2	104	VDOUT16
105	VDIN4	106	VDOUT23
107	VDIN3	108	VDOUT22
109	VCLK	110	UART1RXD
111	GND	112	UART1TXD
113	VDIN6	114	UART1RTS
115	C24MOUT	116	UART1CTS
117	VDIN5	118	UART0RXD
119	VDIN7	120	UART0TXD
121	VVSYNC	122	SD3CMD
123	VHSYNC	124	SD3CLK
125	GPIO12	126	SD3DATA0
127	GPIO13	128	SD3DATA3
129	GND	130	SD3DATA2
131	SPK_OUT_R-	132	SD3DATA1
133	SPK_OUT_R+	134	SD3PWRSW
135	GND	136	SD3WP
137	SPK_OUT_L-	138	I2CSDA
139	SPK_OUT_L+	140	I2C1SCL
141	GND	142	I2C2SCL
143	HPOUTR	144	I2C2SDA
145	OUT3	146	I2C3SDA
147	HPOUTL	148	I2C3SCL
149	MICBIAS	150	SUS_GPIO0
151	GND	152	PWRGD
153	LINPUT3	154	WAKEUP0
155	LINPUT2	156	SPI1MOSI



Pin	Signal	Pin	Signal
157	LINPUT1	158	GND
159	GND	160	SPI1CLK
161	RINPUT1	162	SPI1SS0-
163	RINPUT2	164	SPI1MISO
165	GND	166	GPIO1
167	WAKEUP3	168	GPIO0
169	PWRENVCC	170	GPIO6
171	WAKEUP2	172	GPIO3
173	CIRIN	174	GPIO4
175	PWRENMEM	176	GPIO5
177	PWRENVDD	178	GPIO9
179	SUS_GPIO1	180	GPIO7
181	PWRBTN-	182	GPIO8
183	RSMRST-	184	VSUS33
185	PWMOUT3	186	VSUS33
187	PWMOUT2	188	VCC33
189	PWREN_MAIN	190	VCC33
191	VCC-BAT	192	VCC33
193	NC	194	NC
195	5VIN	196	GND
197	5VIN	198	GND
199	5VIN	200	GND
201	5VIN	202	GND
203	5VIN	204	GND

Table 5: SOM DDR3 SODIMM slot pinouts

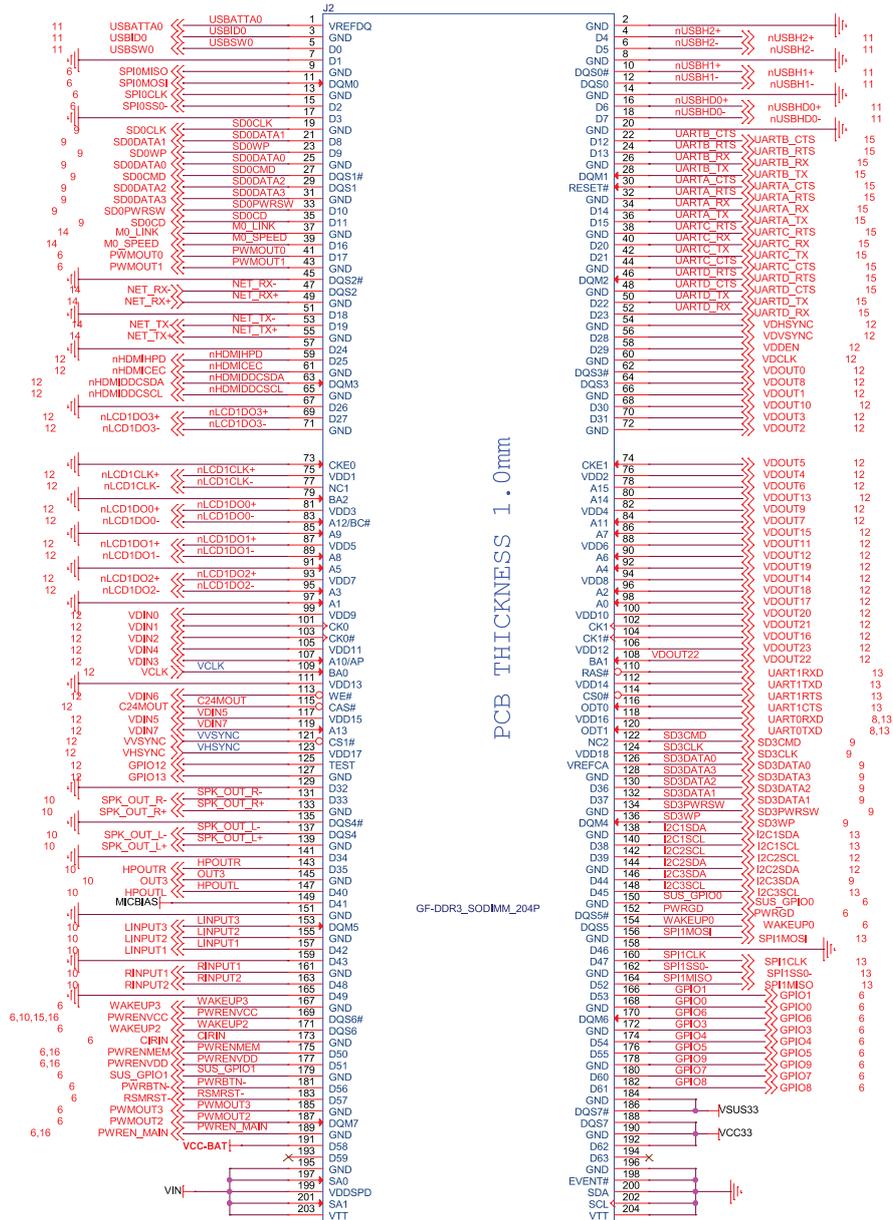


Figure 22: SOM DDR3 SODIMM slot schematics

4. Layout and Routing Recommendation

The information presented in this chapter includes the signal definition, topology, layout and routing guidelines for each bus interface, and reference schematics example. The information provided is intended for designing carrier boards that are compliant with the SOM-6X50 module.

4.1 HDMI Interface

The SOM-6X50 module features one HDMI interface. The HDMI interface uses four control signals, one differential clock, and three differential data pair signals that carry video and audio signals.

4.1.1 HDMI Signal Definition

The following table provides the definition of the HDMI signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
nHDMID0+	81	O	HDMI differential pair lines lane 0
nHDMID0-	83		
nHDMID1+	87	O	HDMI differential pair lines lane 1
nHDMID1-	89		
nHDMID2+	93	O	HDMI differential pair lines lane 2
nHDMID2-	95		
nHDMICLK+	75	O	HDMI differential pair clock lines
nHDMICLK-	77		
nHDMIDDCSCL	65	IO	HDMI DDC SCL
nHDMIDDCSDA	63	IO	HDMI DDC SDA
nHDMICEC	61	O	HDMI consumer electronics connector
nHDMIHPD	59	O	HDMI hot plug detect

Table 6: HDMI signal definition

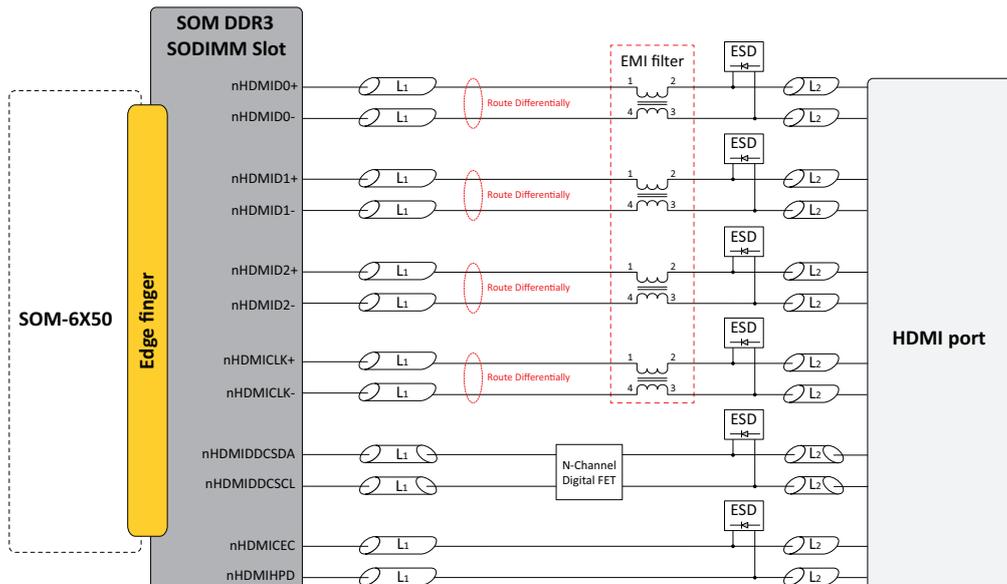


Figure 23: HDMI routing topology

Note:
The EMI filters and ESD components must be placed near the HDMI port.

4.1.2 HDMI Layout and Routing Recommendations

- Trace lengths should be kept to a minimum.
- Each trace of differential pairs should not have more than two via holes.
- Each differential pairs signal should route to parallel to each other with the same trace length.
- Differential pair should be all referenced to ground.
- Route the differential pairs on a single layer adjacent to a ground plane.
- The spacing between the differential pair signal and other signals should be at least three times the trace width.

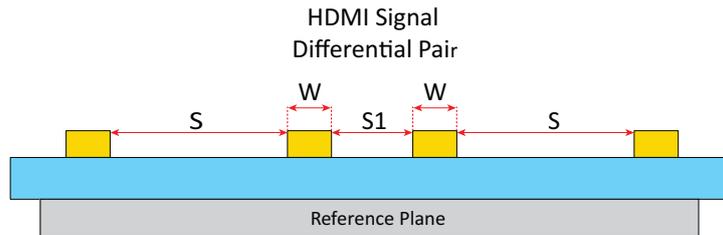


Figure 24: HDMI differential trace width and spacing example

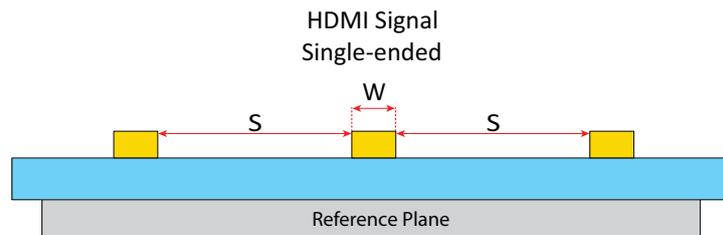


Figure 25: HDMI single-ended trace width and spacing example

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	nHDMID0+	100Ω ± 15% (Differential)	15 : 5 : 7 : 5 : 15	<5mil (Differential)	15mil
	nHDMID0-				
	nHDMID1+				
	nHDMID1-				
	nHDMID2+				
	nHDMID2-				
Clock	nHDMICLK+	100Ω ± 15% (Differential)	15 : 5 : 7 : 5 : 15	<5mil (Differential)	15mil
	nHDMICLK-				
Control	nHDMIDDCSCL	50Ω ± 15%	5 : 10 (W:S)	6mil	10mil
	nHDMIDDCSDA				
	nHDMICEC				
	nHDMIHPD				

Table 7: HDMI trace properties

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length (L _T + L ₂ = L _T)	Length Difference (mil)	
				To Clock	In Group
Data	nHDMID0+	Top/Bottom	L _T < 3"	<500	<1000
	nHDMID0-				
	nHDMID1+				
	nHDMID1-				
	nHDMID2+				
	nHDMID2-				
Clock	nHDMICLK+	Top/Bottom	L _T < 3"	<500	<1000
	nHDMICLK-				
Control	nHDMIDDCSCL	Top/Bottom	L _T < 3"	<500	<1000
	nHDMIDDCSDA				
	nHDMICEC				
	nHDMIHPD				

Table 8: HDMI layout guidelines

Signal Group	Signal Name	Reference Plane	Routing Topology	Signal Type
Data	nHDMID0+	Ground	Point-to-Point	Differential Pairs
	nHDMID0-			
	nHDMID1+			
	nHDMID1-			
	nHDMID2+			
	nHDMID2-			
Clock	nHDMICLK+	Ground	Point-to-Point	Differential Pairs
	nHDMICLK-			
Control	nHDMIDDCSCL	Ground	Point-to-Point	Single-ended
	nHDMIDDCSDA			
	nHDMICEC			
	nHDMIHPD			

Table 9: HDMI routing topology and signal type

4.1.3 HDMI Reference Schematics

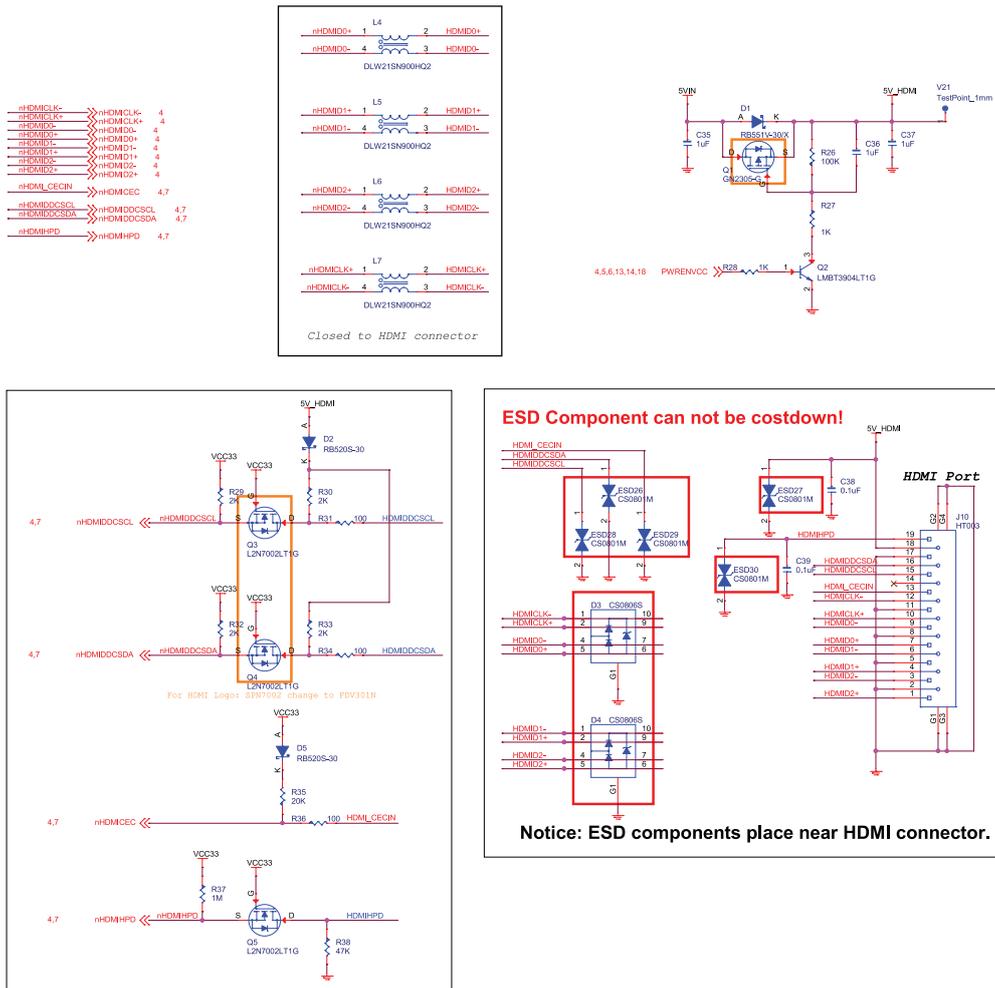


Figure 26: HDMI reference circuitry

4.2 Ethernet Interface

The SOM-6X50 module features one Ethernet (10/100Mbps) interface. The Ethernet interface consists of two differential data signals and two control signals for activity link and speed indicators.

4.2.1 Ethernet Signal Definition

The following table provides the definition of the Ethernet signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
NET_TX+	55	O	Ethernet differential pair lines Transmit
NET_TX-	53		
NET_RX+	49	O	Ethernet differential pair lines Receive
NET_RX-	47		
MO_SPEED	39	O	Ethernet controller 0 100Mbps speed indicator
MO_LINK	37	O	Ethernet controller 0 100Mbps link indicator

Table 10: Ethernet signal definition

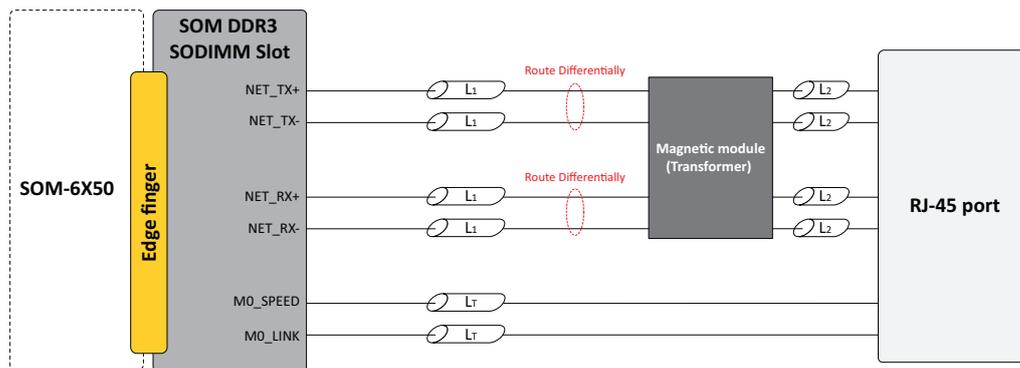


Figure 27: Ethernet routing topology

Note:

The magnetic module has to be placed as close as possible to the RJ-45 port. The distance must be less than 1".

4.2.2 Ethernet Layout and Routing Recommendations

- Route differential pairs close together and away from other signals.
- Route any other trace parallel to one of the differential trace.
- Keep trace length within each differential pair equal.
- Keep proper impedance between two traces within a differential pair.
- Each trace of differential pairs should not have more than two via holes.
- The spacing between the differential pair signal and other signals should be at least three times the trace width.
- Each differential pair of signals is required to be parallel to each other with the same trace length (Tolerance $\pm 50\text{mil}$) on the component (top) layer and to be parallel to a respective ground plane. The length difference between the shortest and longest pairs should be less than 200mil.
- The accumulated trace length of the differential signals pair between the SOM DDR3 SODIMM slot and magnetic module should be less than 1".
- The accumulated trace length of the differential signals pair between the magnetic module and RJ-45 connector should be less than 1". Isolate ground plane and connect to chassis.
- Keep each differential pair on the same plane.
- To prevent any noise from injecting into the differential pairs, be sure to keep digital signals or other signals away from the differential signals.
- The external magnetic module should be placed close to the RJ-45 connector to limit EMI emissions.

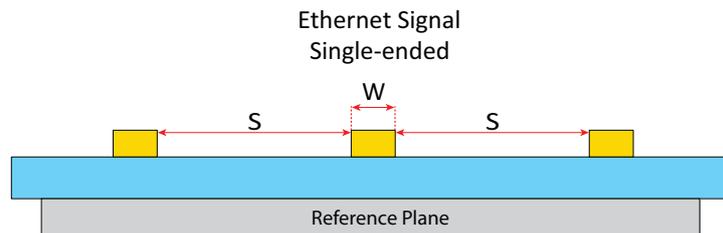


Figure 28: Ethernet single-ended trace width and spacing example

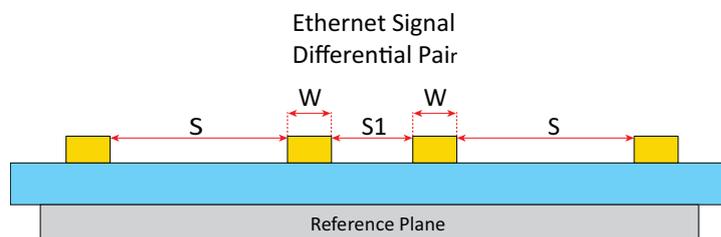


Figure 29: Ethernet differential trace width and spacing example

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	NET_TX+	100Ω ± 15% (Differential)	10 : 10 : 5 : 10 : 10	50mil	10mil
	NET_TX-				
	NET_RX+				
	NET_RX-				
Control	MO_SPEED	55Ω ± 15%	5:10	-	10mil
	MO_LINK				

Table 11: Ethernet trace properties

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length (L1+ L2 = Lt)	Length Difference (mil)
				To Clock
Data	NET_TX+	Top/Bottom	Lt < 3"	<1500
	NET_TX-			
	NET_RX+			
	NET_RX-			
Control	MO_SPEED	Top/Bottom	Lt < 3"	<1500
	MO_LINK			

Table 12: Ethernet layout guidelines

Signal Group	Signal Name	Reference Plane	Signal Type	Routing Topology
Data	NET_TX+	Ground/Power	Differential Pairs	Point-to-Point
	NET_TX-			
	NET_RX+			
	NET_RX-			
Control	MO_SPEED	Ground/Power	Single-ended	Point-to-Point
	MO_LINK			

Table 13: Ethernet reference plane, signal type and routing topology

4.2.3 Ethernet Reference Schematics

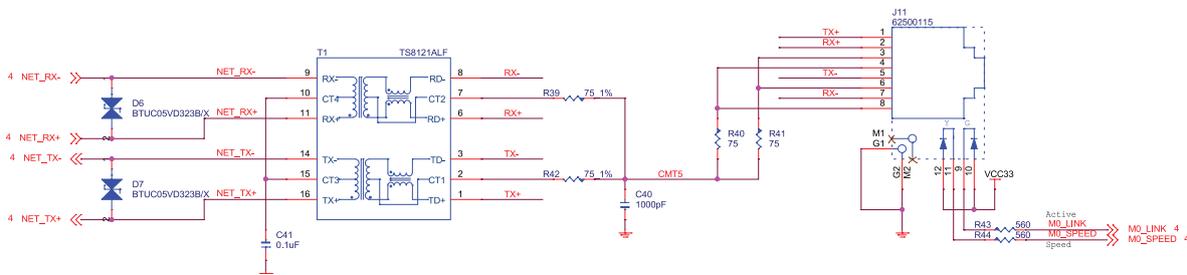


Figure 30: Ethernet reference circuitry

4.3 USB Interface

The SOM-6X50 module features three USB 2.0 interfaces. Two of the three USB interfaces can only be used as a host. The other interface can be configured to be used as either the host or client. The USB interface signals use three bi-directional differential data pairs.

4.3.1 USB Signal Definition

The following table provides the definition of the USB signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
nUSBHD0+	16	IO	OTG Universal Serial Bus port 0, data+
nUSBHD0-	18		OTG Universal Serial Bus port 0, data-
nUSBHD1+	10	IO	Universal Serial Bus port 1, data+
nUSBHD1-	12		Universal Serial Bus port 1, data-
nUSBHD2+	4	IO	Universal Serial Bus port 2, data+
nUSBHD2-	6		Universal Serial Bus port 2, data-
USBATTA0	1	I	Universal Serial Bus device attach detect
USBID0	3	I	Port ID pin
USBSW0	5	I	Universal Serial Bus power control pin

Table 14: USB signal definition

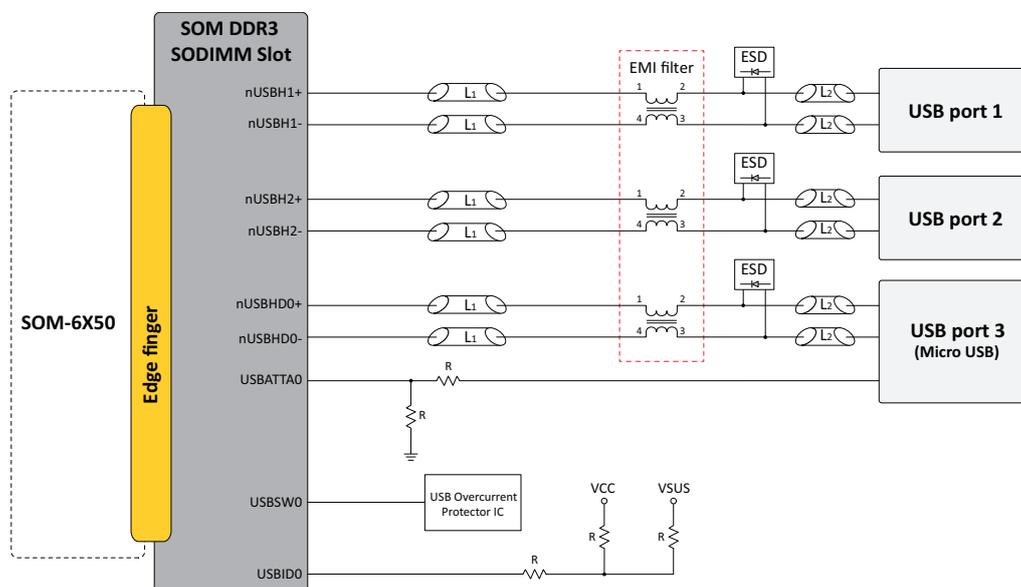


Figure 31: USB routing topology

4.3.2 USB Layout and Routing Recommendations

- The differential pair signals should be all referenced to ground.
- Each trace of differential pairs should not have more than two via holes.
- Differential pair route in parallel and in equal length.
- The amount of vias and corners used for the USB signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Each pair of USB data lines is required to be parallel to each other with the same trace length, and not parallel with other signals to minimize crosstalk.
- Separate the signal traces into similar groups and route similar signal traces together. In addition, it is recommended to have differential pairs routed together on the carrier board.
- Control trace signals impedance should maintain $55\Omega \pm 10\%$.
- For the USB traces, do not route them under oscillators, crystals, clock synthesizers, magnetic devices or IC's which could be using duplicate clocks.

The routing example for two pairs of USB data buses is shown in Figure 32.

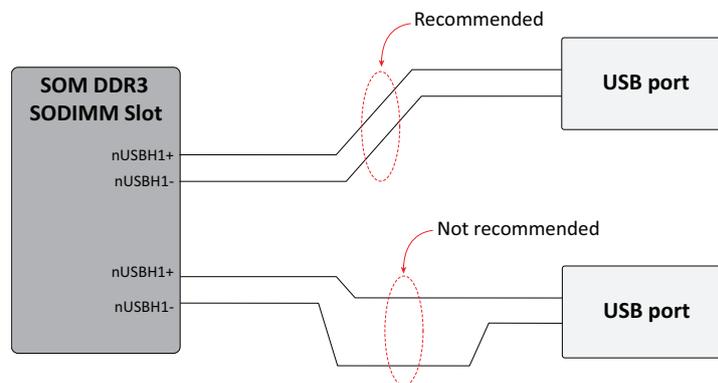


Figure 32: USB differential signal routing example

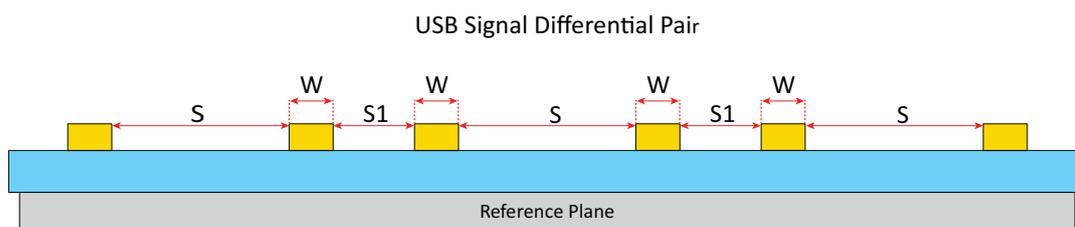


Figure 33: USB differential trace width and spacing example

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	nUSBH1+	90Ω ± 15%	20 : 7 : 7.5 : 7 : 20	100mil	20mil
	nUSBH1-				
	nUSBH2+				
	nUSBH2-				
	nUSBHD0+				
	nUSBHD0-				
Control	USBATTA0	55Ω ± 10%	5 : 10	-	10mil
	USBID0				
	USBSW0				

Table 15: USB trace properties

Signal Group	Signal Name	Termination Option	Signal Type	Topology	
Data	Port 1	90Ω	Differential Data Pairs	Point-to-Point	
					nUSBH1+
	nUSBH1-				
	Port 2				nUSBH2+
					nUSBH2-
	Port 3				nUSBHD0+
nUSBHD0-					
Control	USBATTA0	60Ω	-	Point-to-Point	
	USBID0				
	USBSW0				

Table 16: USB termination option, signal type and routing topology

Signal Group	Signal Name	Routing Layer	Length Difference (In Pair)	Accumulated Trace Length (L ₁ + L ₂ = L _T)	
Data	Port 1	Top/Bottom	<100mil	L _T < 12"	
					nUSBH1+
	nUSBH1-				
	Port 2				nUSBH2+
					nUSBH2-
	Port 3				nUSBHD0+
nUSBHD0-					
Control	USBATTA0	Top/Bottom	-	L _T < 12"	
	USBID0				
	USBSW0				

Table 17: USB layout guidelines

4.3.3 USB Reference Schematics

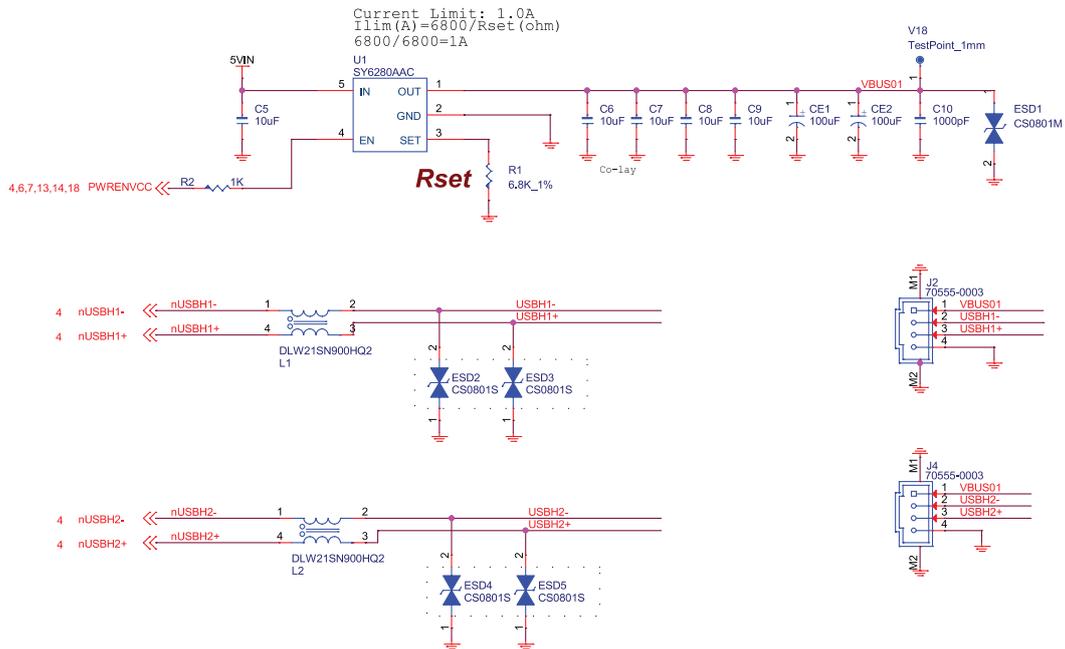


Figure 34: USB host reference circuitry

The USB port mode can be controlled by the signal USBID0. In the reference circuitry example below, the USBID0 signal is referenced to ground that makes the USB port mode as client USB (or USB OTG port).

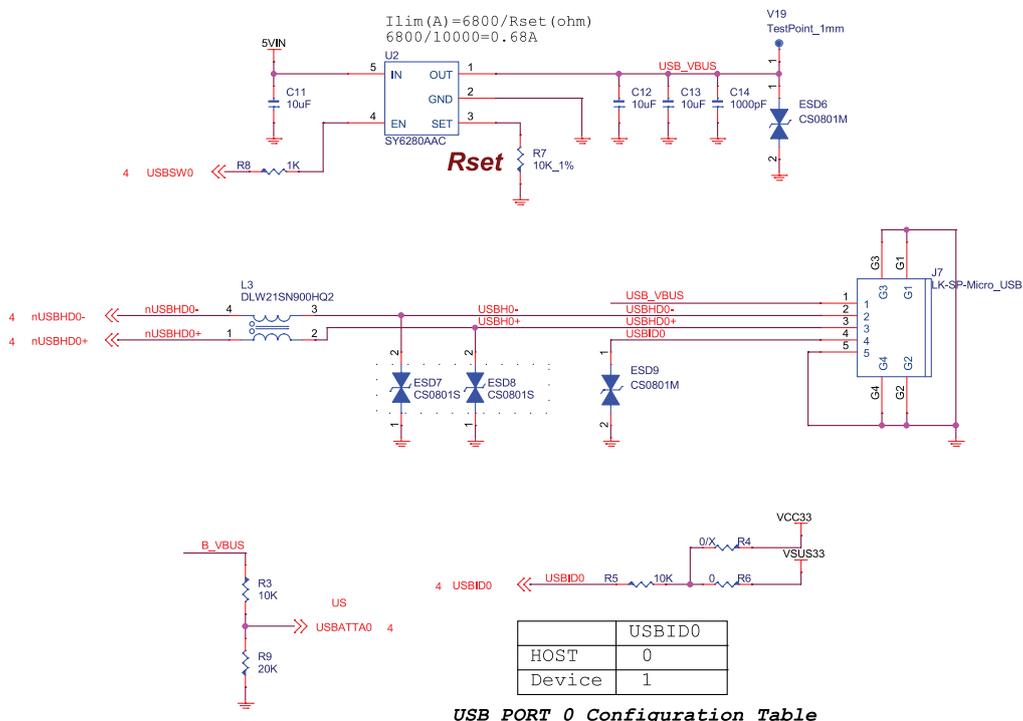


Figure 35: USB client reference circuitry

4.4 COM and UART Interface

The SOM-6X50 module features COM and UART interfaces that enable the interfacing of four COM or two UART on the carrier board. The four COM interfaces are used for RS-232 serial communications and the two UART can be used for TX/RX, RTS, CTS and debugging TX/RX.

4.4.1 COM and UART Signal Definition

The following table provides the definition of the COM and UART signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
UARTA_TX	36	O	UART Port-A transmit data
UARTA_RX	34	I	UART Port-A receive data
UARTA_RTS	32	O	UART Port-A request to send
UARTA_CTS	30	I	UART Port-A clear to send
UARTB_TX	28	O	UART Port-B transmit data
UARTB_RX	26	I	UART Port-B receive data
UARTB_RTS	24	O	UART Port-B request to send
UARTB_CTS	22	I	UART Port-B clear to send
UARTC_TX	42	O	UART Port-C transmit data
UARTC_RX	40	I	UART Port-C receive data
UARTC_RTS	38	O	UART Port-C request to send
UARTC_CTS	44	I	UART Port-C clear to send
UARTD_TX	50	O	UART Port-D transmit data
UARTD_RX	52	I	UART Port-D receive data
UARTD_RTS	46	O	UART Port-D request to send
UARTD_CTS	48	I	UART Port-D clear to send
UART1TXD	112	O	UART Port-1 transmit data
UART1RXD	110	I	UART Port-1 receive data
UART1CTS	116	O	UART Port-1 clear to send
UART1RTS	114	I	UART Port-1 request to send
UART0TXD	120	O	UART Port-0 transmit data
UART0RXD	118	I	UART Port-0 receive data

Table 18: COM and UART signal definition

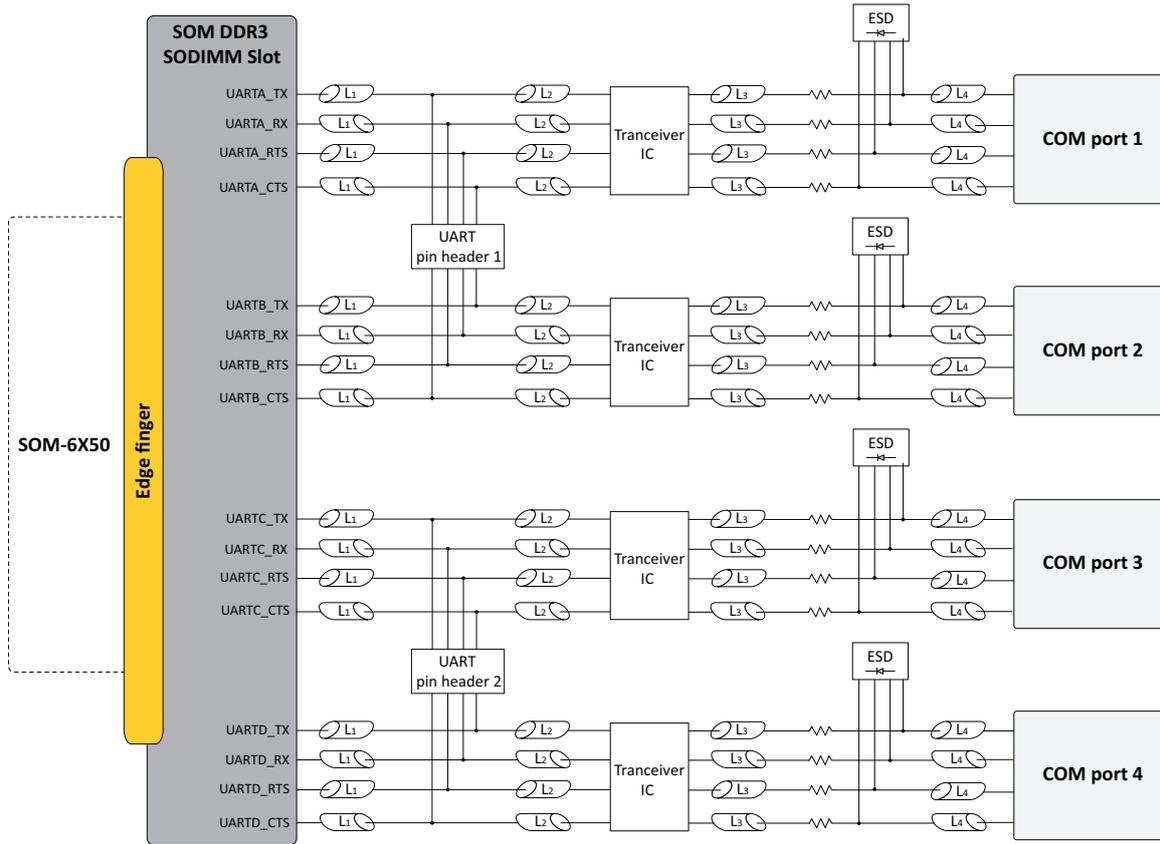


Figure 36: COM and UART routing topology

4.4.2 COM and UART Layout and Routing Recommendations

- The transmit and receive data trace signals should be routed in parallel and in equal length.
- The amount of vias and corners used for the COM and UART signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Control trace signals impedance should maintain $55\Omega \pm 10\%$.

Signal Group	Signal Name	Trace (mil) (Width : Spacing)	Trace Impedance	Spacing in Other Group
Data	UART[D:A]_TX	5 : 5	$55\Omega \pm 10\%$	5mil
	UART[D:A]_RX			
	UART[1:0]TXD			
	UART[1:0]RXD			
Control	UART[D:A]_CTS	5 : 5	$55\Omega \pm 10\%$	5mil
	UART[D:A]_RTS			
	UART1CTS			
	UART1RTS			

Table 19: COM and UART trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length (L1 + L2 + L3 + L4 = Lt)
Data	UART[D:A]_TX	Single-ended	Point-to-Point	Ground/Power	<10"
	UART[D:A]_RX				
	UART[1:0]TXD				
	UART[1:0]RXD				
Control	UART[D:A]_CTS	Single-ended	Point-to-Point	Ground/Power	<10"
	UART[D:A]_RTS				
	UART1CTS				
	UART1RTS				

Table 20: COM and UART topology, signal type and layout guidelines

4.4.3 COM and UART Reference Schematics

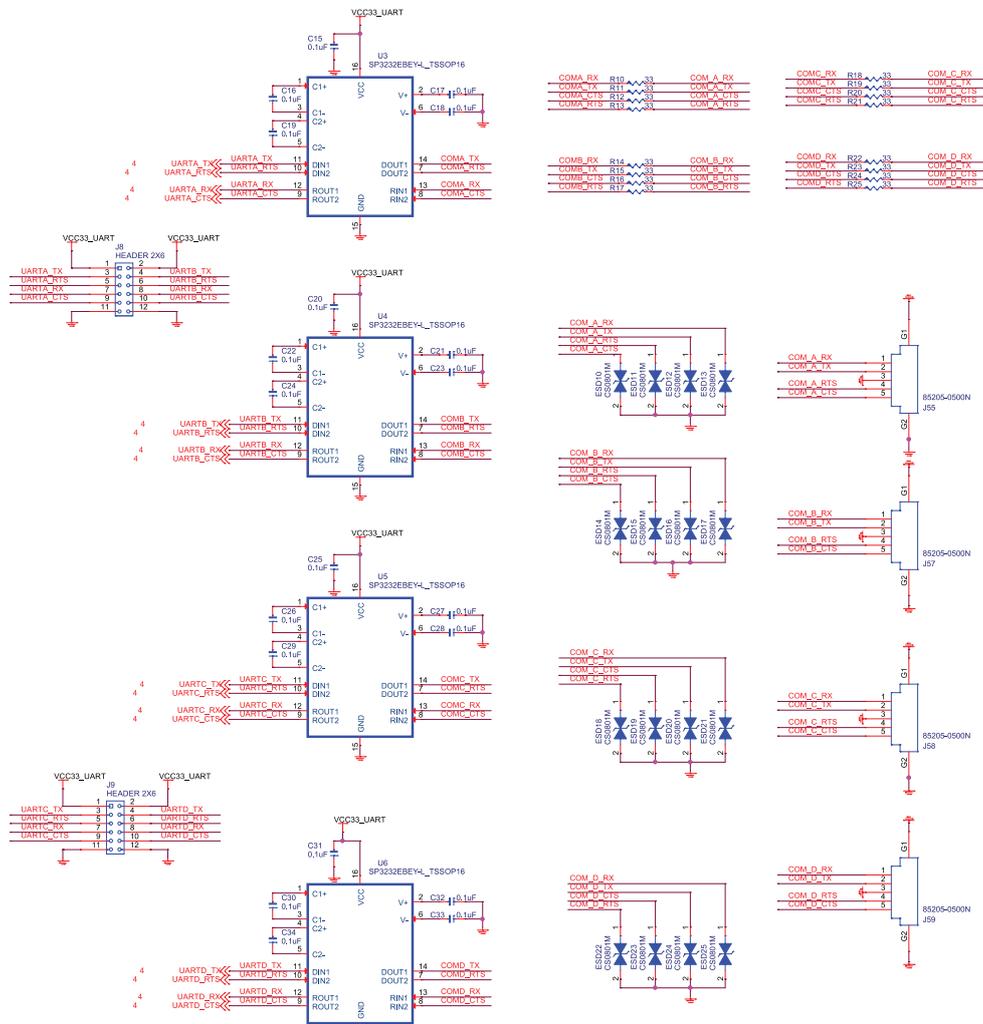


Figure 37: COM and UART reference circuitry

4.5 LCD Interface

The SOM-6X50 module features one (RGB) LCD interface. The LCD interface is a parallel bus signal provided for interfacing the LCD connector for LVDS LCD display as the main display interface. The LCD interface is a single-channel that supports 18-bit and 24-bit interfaces.

4.5.1 LCD Signal Definition

The following table provides the definition of the LCD signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
VDOUT0	62	O	Blue LCD data signal
VDOUT1	66	O	
VDOUT2	72	O	
VDOUT3	70	O	
VDOUT4	76	O	
VDOUT5	74	O	
VDOUT6	78	O	
VDOUT7	84	O	
VDOUT8	64	O	Green LCD data signal
VDOUT9	82	O	
VDOUT10	68	O	
VDOUT11	88	O	
VDOUT12	90	O	
VDOUT13	80	O	
VDOUT14	94	O	
VDOUT15	86	O	
VDOUT16	104	O	Red LCD data signal
VDOUT17	98	O	
VDOUT18	96	O	
VDOUT19	92	O	
VDOUT20	100	O	
VDOUT21	102	O	
VDOUT22	108	O	
VDOUT23	106	O	
VDHSYNC	54	O	LCD Line Horizontal Sync
VDVSYNC	56	O	LCD Frame Vertical Sync
VDDEN	58	O	LCD Data Enable
VDCLK	60	O	LCD Clock

Table 21: LCD signal definition

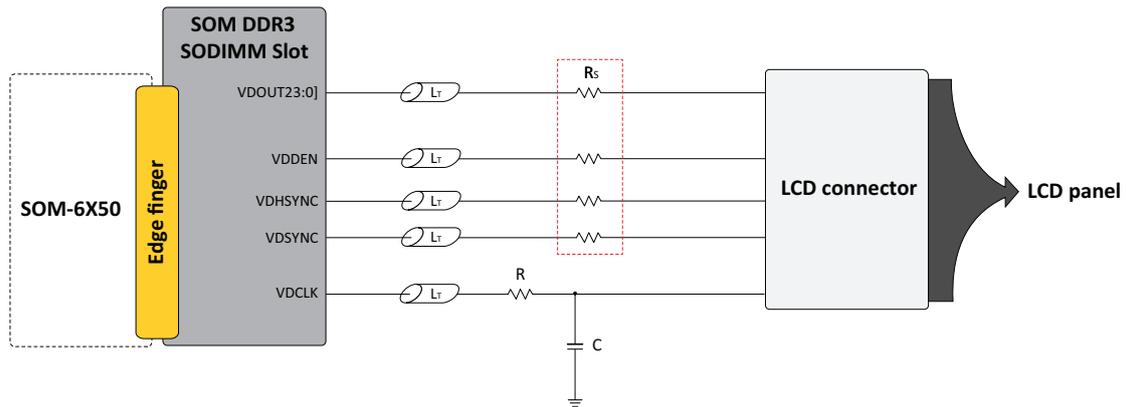


Figure 38: LCD routing topology

4.5.2 LCD Layout and Routing Recommendations

- RGB data signal traces should be designed to be as short as possible.
- In order to maximize the noise rejection characteristics of the RGB video outputs, it is then recommended to route the RGB video outputs on the top layer over a solid ground plane.
- The routing for the RGB signals should be as similar as possible (i.e., same routing layer, same number of vias, same routing length and same bends).
- Route the RGB data trace signals and two sync signals (VDHSYNC and VDVSINC) as a single-ended signal with a trace impedance of 55Ω .

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Trace Mismatch	Spacing to Other Signal
Data	VDOU[7:0]	55Ω ± 10%	5 : 10	1000mil	10mil
	VDOU[15:8]				
	VDOU[23:16]				
Control	VDHSYNC	55Ω ± 10%	5 : 10	1000mil	10mil
	VDVSINC				
Clock	VDCLK	55Ω ± 10%	5 : 15	-	-

Table 22: LCD trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane
Data	VDOU[7:0]	Single-ended	Point-to-Point	Ground/Power
	VDOU[15:8]			
	VDOU[23:16]			
Control	VDHSYNC	Single-ended	Point-to-Point	Ground/Power
	VDVSINC			
Clock	VDCLK	Single-ended	Point-to-Point	Ground/Power

Table 23: LCD signal type, topology and reference plane

Signal Group	Signal Name	Routing Layer	Length Difference (mil)		Accumulated Trace Length (Lr)
			To Clock	In Group	
Data	VDOUT[7:0]	Top/Bottom	<500	<1000	Route to Minimum (or <6")
	VDOUT[15:8]				
	VDOUT[23:16]				
Control	VDHSYNC	Top/Bottom	<500	<1000	Route to Minimum (or <6")
	VDVSYNC				
Clock	VDCLK	Top/Bottom	--	---	--

Table 24: LCD layout guidelines

4.5.3 LCD Reference Schematics

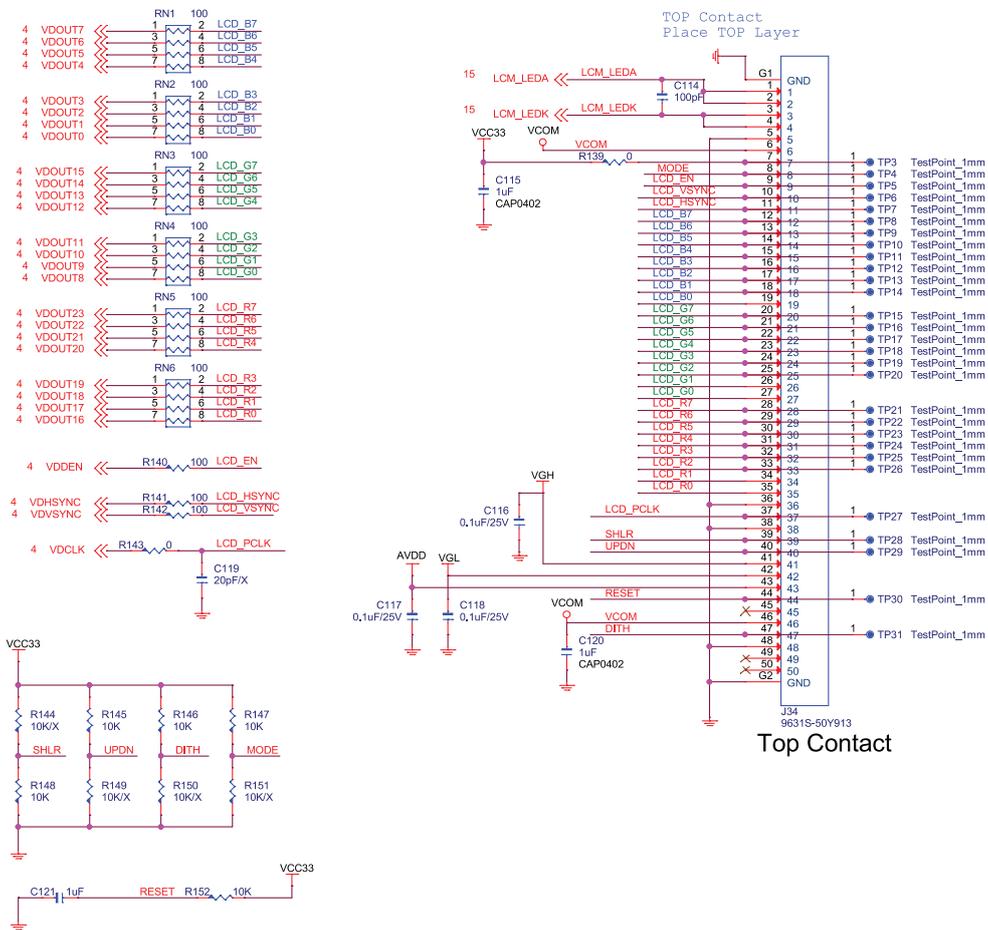


Figure 39: LCD reference circuitry

4.6 Touch Panel Interface

The SOM-6X50 module features a touch panel interface for capacitive touch screens. It allows the integration of the touch screen solution on the carrier board. The touch panel interface is an interface connection between the SOM DDR3 SODIMM slot, capacitive touch sensor controller, and touch panel connector. The touch panel interface supports 4-wire and 5-wire capacitive touch screens.

4.6.1 Touch Panel Signal Definition

The following table provides the definition of the touch panel signals.

From SOM DDR3 SODIMM Slot to Capacitive Touch Sensor Controller			
Signal Name	Pin #	I/O	Description
GPIO4	174	O	TP reset signal
GPIO5	176	O	TP interrupt signal
I2C3SDA	146	O	TP I ² C Data
I2C3SCL	148	O	TP I ² C Clock
From Capacitive Touch Sensor Controller to Touch Panel Connector			
Signal Name	Pin #	I/O	Description
DRIVE00	22	O	Capacitive touch IC drive line-0
DRIVE01	23	O	Capacitive touch IC drive line-1
DRIVE02	24	O	Capacitive touch IC drive line-2
DRIVE03	25	O	Capacitive touch IC drive line-3
DRIVE04	26	O	Capacitive touch IC drive line-4
DRIVE05	27	O	Capacitive touch IC drive line-5
DRIVE06	28	O	Capacitive touch IC drive line-6
DRIVE07	29	O	Capacitive touch IC drive line-7
DRIVE08	9	O	Capacitive touch IC drive line-8
DRIVE09	8	O	Capacitive touch IC drive line-9
DRIVE10	7	O	Capacitive touch IC drive line-10
DRIVE11	6	O	Capacitive touch IC drive line-11
DRIVE12	5	O	Capacitive touch IC drive line-12
DRIVE13	4	O	Capacitive touch IC drive line-13
DRIVE14	3	O	Capacitive touch IC drive line-14
DRIVE15	2	O	Capacitive touch IC drive line-15
SENSE00	31	I	Capacitive touch IC sense line-0
SENSE01	32	I	Capacitive touch IC sense line-1
SENSE02	33	I	Capacitive touch IC sense line-2
SENSE03	34	I	Capacitive touch IC sense line-3
SENSE04	35	I	Capacitive touch IC sense line-4
SENSE05	36	I	Capacitive touch IC sense line-5
SENSE06	37	I	Capacitive touch IC sense line-6
SENSE07	38	I	Capacitive touch IC sense line-7
SENSE08	39	I	Capacitive touch IC sense line-8
SENSE09	40	I	Capacitive touch IC sense line-9

Table 25: Touch panel signal definition

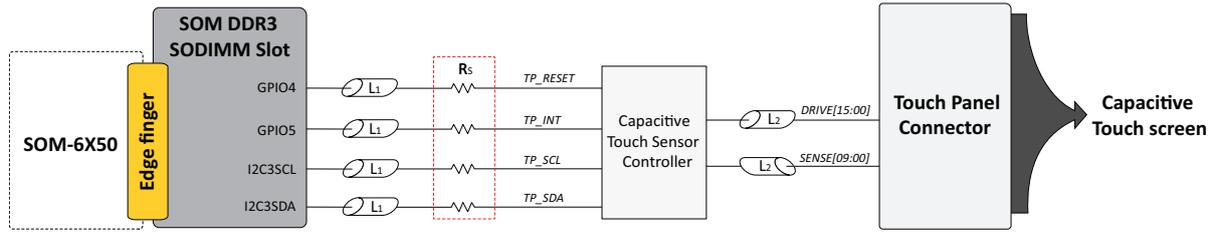


Figure 40: Touch panel routing topology

4.6.2 Touch Panel Layout and Routing Recommendations

- Keep trace lengths as short as possible.
- It is recommended to route the traces on the top layer.
- The amount of vias and corners used for the touch panel signal layout should be minimized.

Interface	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Trace Mismatch	Spacing to Other Signal
SOM DDR3 SODIMM slot to Touch Screen Controller	GPIO4	55Ω ± 10%	5 : 5	20mil	5mil
	GPIO5				
	I2C3SCL				
	I2C3SDA				
Touch screen controller to Touch panel connector	DRIVE[23:00]	55Ω ± 10%	5 : 5	20mil	5mil
	SENSE[09:00]				

Table 26: Touch panel trace properties

Interface	Signal Name	Signal Type	Topology	Reference Plane
SOM DDR3 SODIMM slot to Touch screen controller	GPIO4	Single-ended	Point-to-Point	Ground/Power
	GPIO5			
	I2C3SCL			
	I2C3SDA			
Touch screen controller to Touch panel connector	DRIVE[23:00]	Single-ended	Point-to-Point	Ground/Power
	SENSE[09:00]			

Table 27: Touch panel signal type, routing topology and reference plane

Interface	Signal Name	Routing Layer	Length Difference (mil)	Accumulated Trace Length (L1 + L2 = LT)
SOM DDR3 SODIMM slot to Touch Screen Controller	GPIO4	Top/Bottom	-	2"
	GPIO5			
	I2C3SCL			
	I2C3SDA			
Touch screen controller to Touch panel connector	DRIVE[23:00]	Top/Bottom	200mil	2"
	SENSE[09:00]			

Table 28: Touch panel layout guidelines

4.6.3 Touch Panel Reference Schematics

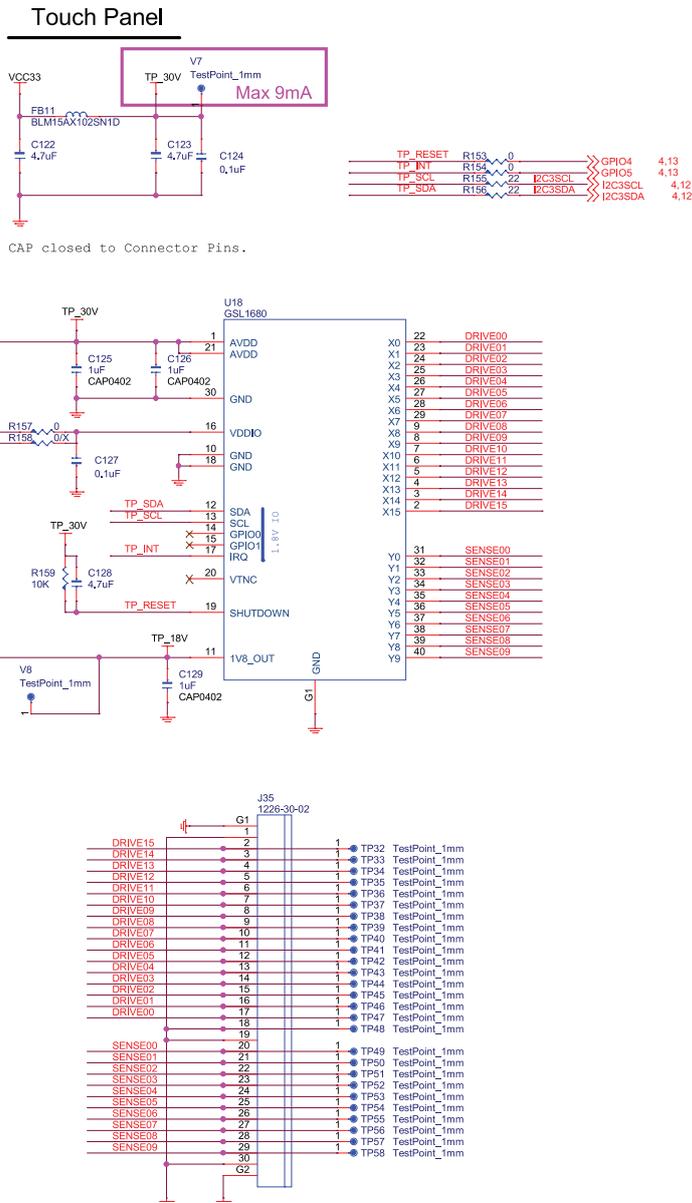


Figure 41: Touch panel reference circuitry

4.7 GPIO Interface

The SOM-6X50 module features a General Purpose Input and Output (GPIO) interface.

4.7.1 GPIO Signal Definition

The following table provides the definition of the GPIO signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
GPIO0	168	IO	General Purpose GPIO
GPIO1	166	IO	
GPIO3	172	IO	
GPIO4	174	IO	
GPIO5	176	IO	
GPIO6	170	IO	
GPIO7	180	IO	
GPIO8	182	IO	
GPIO9	178	IO	
SUS_GPIO0	150	IO	General Purpose GPIO for Suspend Power Domain
SUS_GPIO1	179	IO	

Table 29: GPIO signal definition

4.7.2 GPIO Layout and Routing Recommendation

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	GPIO[1:0]	55Ω	5 : 5	5mil
	GPIO[9:3]			
	SUS_GPIO0	55Ω	5 : 5	5mil
	SUS_GPIO1			

Table 30: GPIO trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
Data	GPIO[1:0]	Single-ended	Point-to-Point	Ground/Power	12"
	GPIO[9:3]				
	SUS_GPIO0	Single-ended	Point-to-Point	Ground/Power	12"
	SUS_GPIO1				

Table 31: GPIO signal type, topology and layout guidelines

4.8 I²C Interface

The SOM-6X50 module features an I²C interface that can support up to three I²C devices.

4.8.1 I²C Signal Definition

The following table provides the definition of the I²C signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
I2C1SDA	138	IO	I ² C1 serial data
I2C1SCL	140	IO	I ² C1 serial clock
I2C2SDA	144	IO	I ² C2 serial data
I2C2SCL	142	IO	I ² C2 serial clock
I2C3SDA	146	IO	I ² C3 serial data
I2C3SCL	148	IO	I ² C3 serial clock

Table 32: I²C signal definition

4.8.2 I²C Layout and Routing Recommendation

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	I2C[3:1]SDA	55Ω	5 : 5	5mil
Clock	I2C[3:1]SCL	55Ω	5 : 5	5mil

Table 33: I²C trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
Data	I2C[3:1]SDA	Single-ended	Daisy chain	Ground/Power	<12"
Clock	I2C[3:1]SCL	Single-ended	Daisy chain	Ground/Power	<12"

Table 34: I²C signal type, topology and layout guidelines

4.9 SPI Interface

The SOM-6X50 module features two SPI interfaces. Each SPI interface can support one master and one slave.

4.9.1 SPI Signal Definition

The following table provides the definition of the SPI signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
SPI0MISO	9	I	Master Input 0, Slave Output 0
SPI0MOSI	11	O	Master Output 0, Slave Input 0
SPI0CLK	13	O	Serial Clock 0
SPI0SS0-	15	O	Slave Select 0
SPI1MOSI	156	I	Master Output 1, Slave Input 1
SPI1MISO	164	O	Master Input 1, Slave Output 1
SPI1CLK	160	O	Serial Clock 1
SPI1SS0-	162	O	Slave Select 1

Table 35: SPI signal definition

4.9.2 SPI Layout and Routing Recommendation

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	SPI[1:0]MISO	55Ω	5 : 5	5mil
	SPI[1:0]MOSI			
	SPI[1:0]SS0-			
Clock	SPI[1:0]CLK	55Ω	5 : 10	5mil

Table 36: SPI trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
Data	SPI[1:0]MISO	Single-ended	Daisy chain	Ground/Power	<10"
	SPI[1:0]MOSI				
	SPI[1:0]SS0-				
Clock	SPI[1:0]CLK	Single-ended	Rs = 22Ω	Ground/Power	<10"

Table 37: SPI signal type, topology and layout guidelines

4.10 Audio Interface

The SOM-6X50 module features an audio interface for audio connectors such as two Line-in, headphone, mono speaker out, right and left channel speakers, and microphone.

4.10.1 Audio Signal Definition

The following table provides the definition of the audio signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
HPOUTR	143	O	Headphone right channel output
HPOUTL	147	O	Headphone left channel output
OUT3	145	O	Audio mono output
LINPUT1	157	I	Left channel single-ended Mic input/Left channel negative differential Mic input
LINPUT2	155	I	Left channel line input/Left channel positive differential Mic input
LINPUT3	153	I	Left channel line input/Left channel positive differential Mic input/Jack detect input pin
RINPUT1	161	I	Right channel single-ended Mic input/Right channel negative differential Mic input
RINPUT2	163	I	Right channel line input/Right channel positive differential Mic input
SPK_OUT_R+	133	O	Right speaker positive output
SPK_OUT_R-	131	O	Right speaker negative output
SPK_OUT_L+	139	O	Left speaker positive output
SPK_OUT_L-	137	O	Left speaker negative output

Table 38: Audio signal definition

4.10.2 Audio Layout and Routing Recommendations

- Route the analog and digital trace signals as far as possible from each other to prevent noise.
- Route the clock trace away from any analog input and voltage reference pins.
- Isolate the codec or put away from any major current path or ground bounce.
- Fill with copper the regions between the analog traces and attached it to the analog ground.
- Fill with copper the regions between the digital traces and attached it to the digital ground.
- Keep trace lengths as short as possible.

Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
HPOUTR	55Ω ± 10%	8 : 5	5mil
HPOUTL			
OUT3	55Ω ± 10%	8 : 5	5mil
LINPUT[3:1]	55Ω ± 10%	8 : 5	5mil
RINPUT[2:1]			
SPK_OUT_R[+/-]	55Ω ± 10%	8 : 5	5mil
SPK_OUT_L[+/-]			

Table 39: Audio trace properties

Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
LINPUT[3:1]	Single-ended	Point-to-Point	Ground	<10"
RINPUT[2:1]				
SPK_OUT_R[+/-]	Single-ended	Point-to-Point	Ground	<10"
SPK_OUT_L[+/-]				

Table 40: Audio signal type, topology and layout guidelines

4.10.3 Audio Interface Reference Schematics

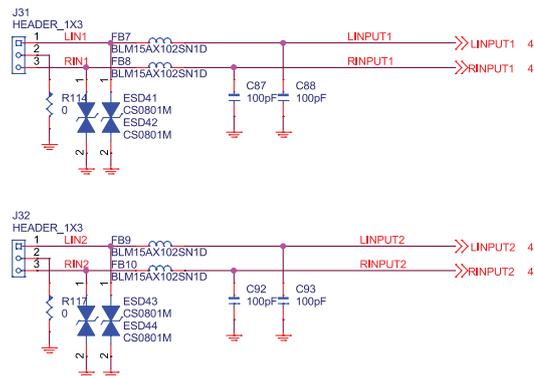


Figure 42: Line-in 1 & 2 reference circuitry

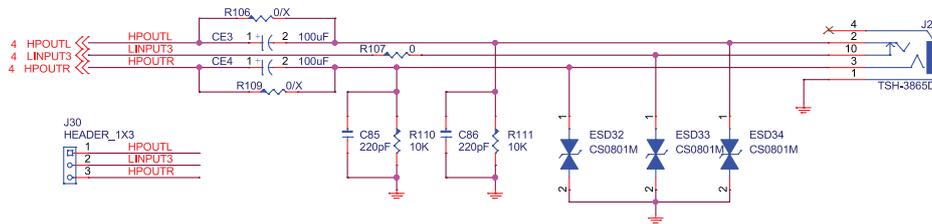


Figure 43: Headphone reference circuitry

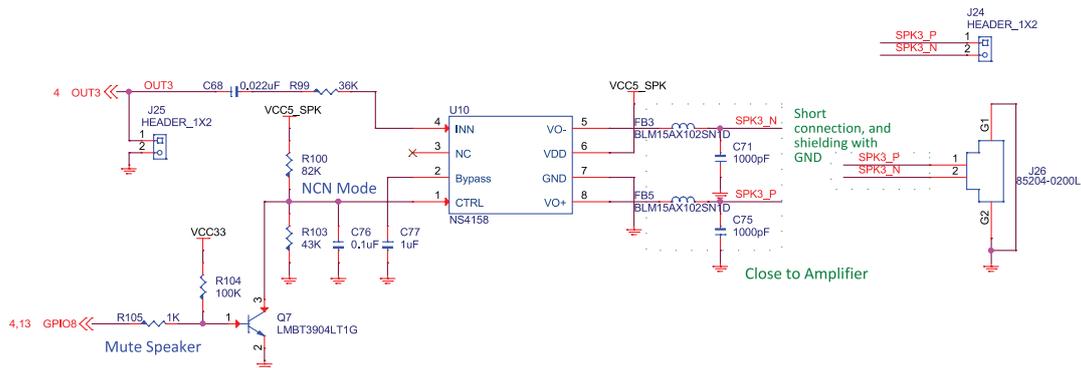


Figure 44: Mono speaker out reference circuitry

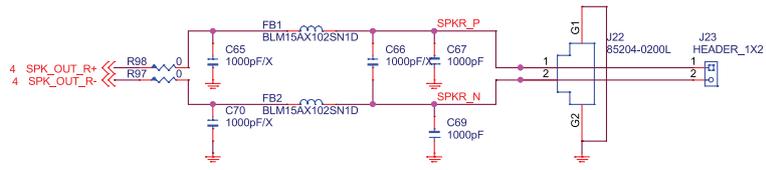


Figure 45: Right channel speaker reference circuitry

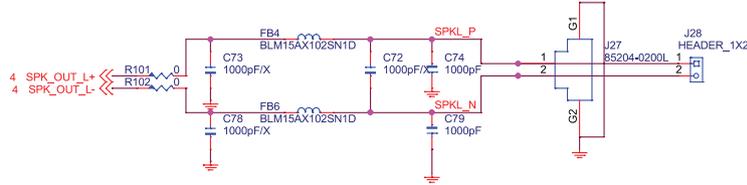


Figure 46: Left channel speaker reference circuitry

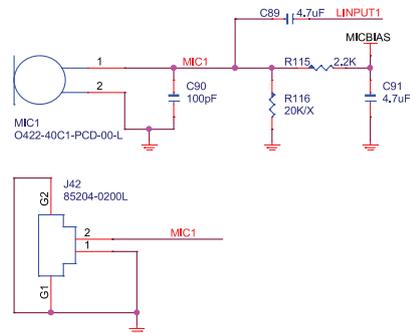


Figure 47: Onboard microphone reference circuitry

4.11 SD Interface

The SOM-6X50 module features an SD interface for SD storage.

4.11.1 SD Signal Definition

The following table provides the definition of the SD signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
SD0DATA0	25	IO	Data signal 0, used for SD interface
SD0DATA1	21	IO	Data signal 1, used for SD interface
SD0DATA2	29	IO	Data signal 2, used for SD interface
SD0DATA3	31	IO	Data signal 3, used for SD interface
SD0CMD	27	IO	Command signal, add external pull-up resistor
SD0CLK	19	O	SD0 bus clock
SD0CD	35	I	SD0 Command
SD0PWRSW	33	O	SD0 Power switch
SD0WP	23	I	SD0 write protect

Table 41: SD signal definition

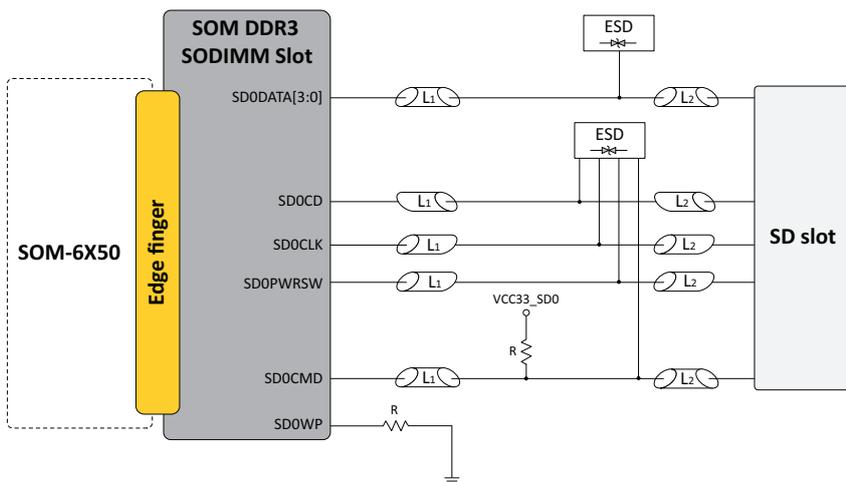


Figure 48: SD routing topology

4.11.2 SD Layout and Routing Recommendations

- Signal traces should be above a solid and continuous ground plane along the path from SOM DDR3 SODIMM slot to SD slot.
- SD0CMD trace signal must have pull-up resistor of 4.7KΩ.
- SD0WP trace signal must have pull-down resistor of 1KΩ to the ground.
- The ESD protection of trace signal SD0PWRSW must be placed near the SD slot.

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	SD0DATA[3:0]	55Ω ± 15%	5 : 5	5mil
Control	SD0CMD	55Ω ± 15%	5 : 5	5mil
	SD0CD			
	SD0WP			
	SD0PWRSW			
Clock	SD0CLK	55Ω ± 15%	5 : 15	15mil

Table 42: SD trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length (L ₁ + L ₂ = L _T)
Data	SD0DATA[3:0]	Single-ended	Point-to-Point	Ground/Power	<8"
Control	SD0CMD	Single-ended	Point-to-Point	Ground/Power	<8"
	SD0CD				
	SD0WP				
	SD0PWRSW				
Clock	SD0CLK	Single-ended	Point-to-Point	Ground/Power	<8"

Table 43: SD signal type, topology and layout guidelines

4.11.3 SD Interface Reference Schematics

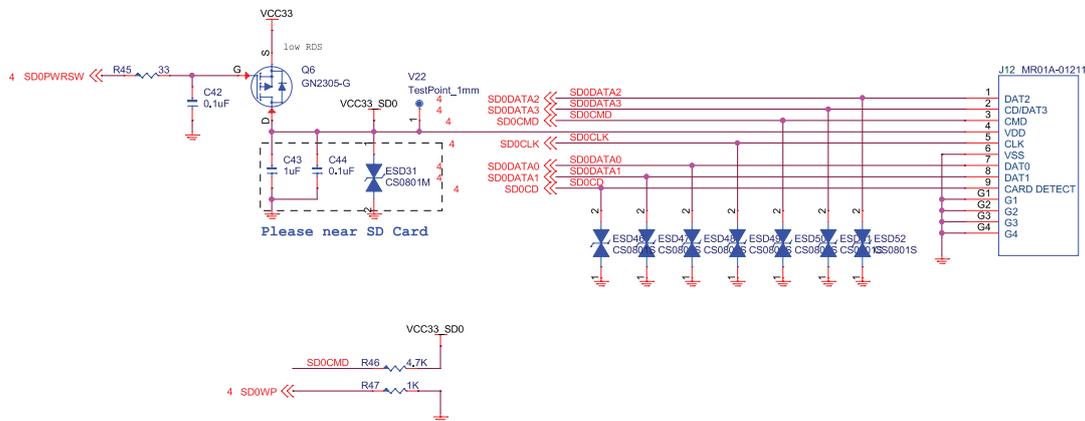


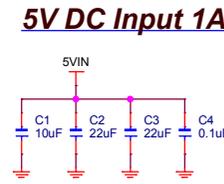
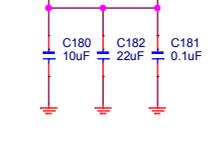
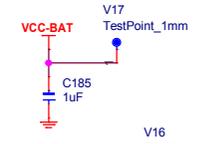
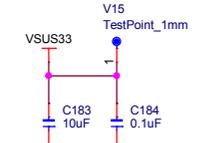
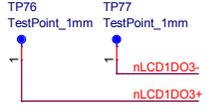
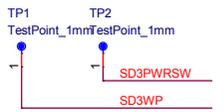
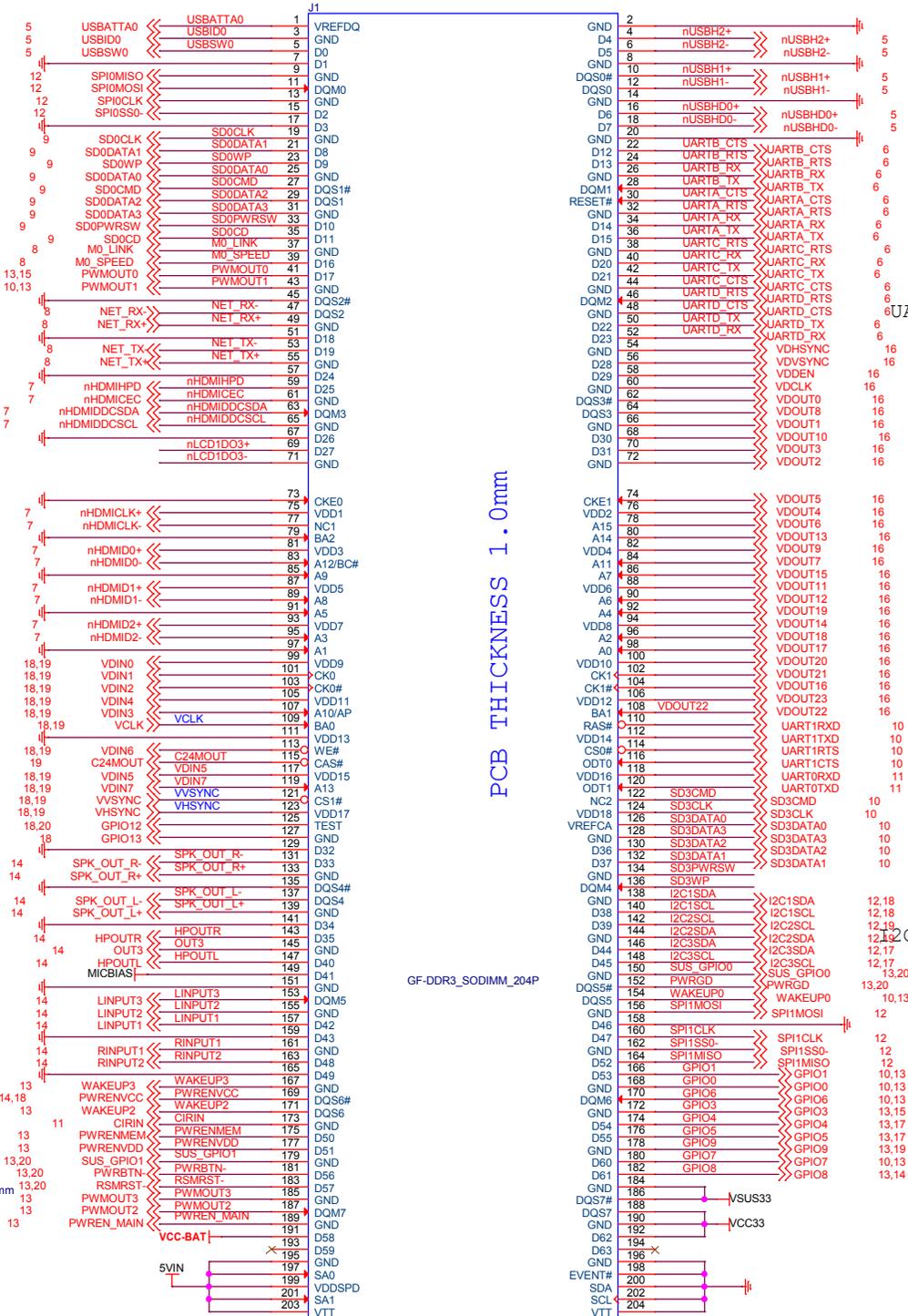
Figure 49: SD reference circuitry



Appendix A. SOMDB1 Carrier Board Reference Schematics

The SOMDB1 is the evaluation carrier board for SOM-6X50 module. The schematics of the SOMDB1 carrier board can be used as an example of how to design a carrier board that provides optimal performance when used with the SOM-6X50 module. The reference designs are only for referencing and not to be copied.

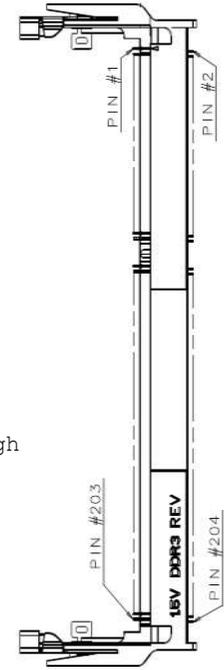
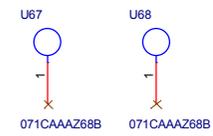
DDR3 SODIMM Golden finger



UART 3 has lower throughput rates than UARTS 0-2

UART0 and 1 from WM8850

I2C Signal need external pull high



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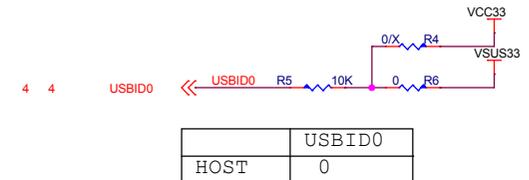
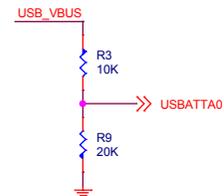
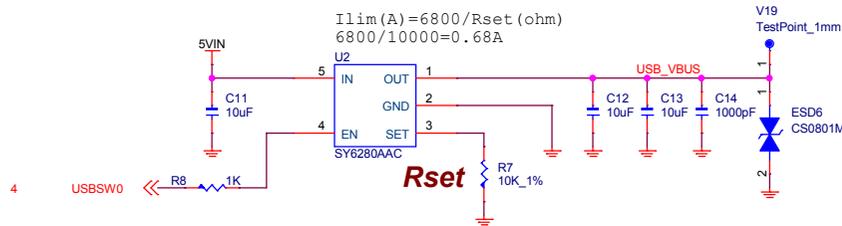
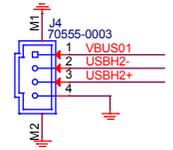
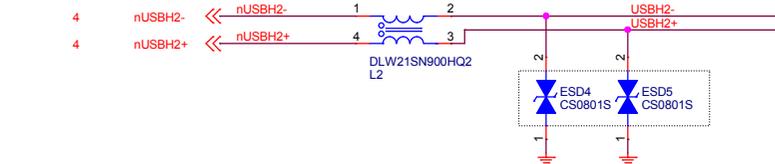
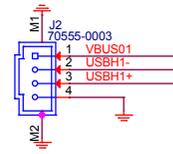
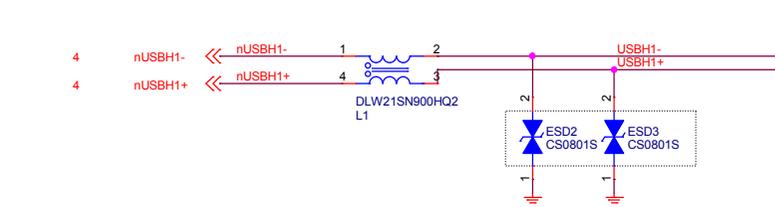
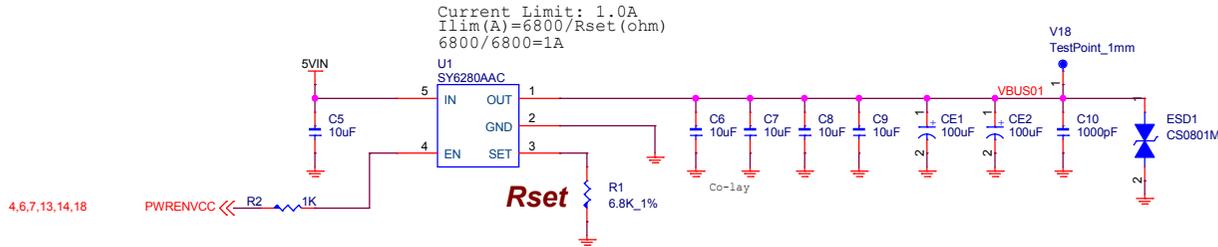
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Size: Document Number **VTS8666C** Rev: 1.0

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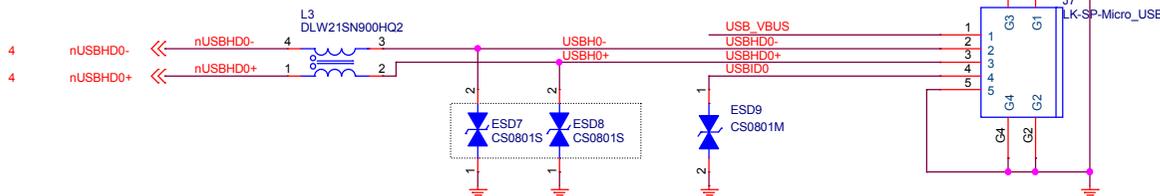
USB

Current Limit: 1.0A
 $I_{lim}(A) = 6800 / R_{set}(\text{ohm})$
 $6800 / 6800 = 1A$



	USBID0
HOST	0
Device	1

USB PORT 0 Configuration Table



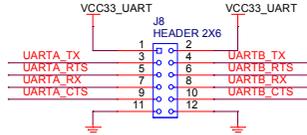
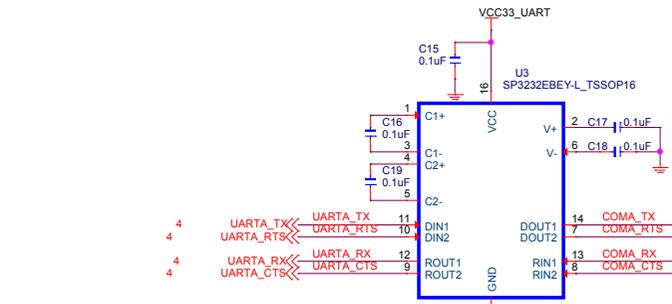
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Title: **USB I/F**

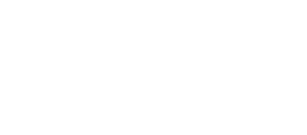
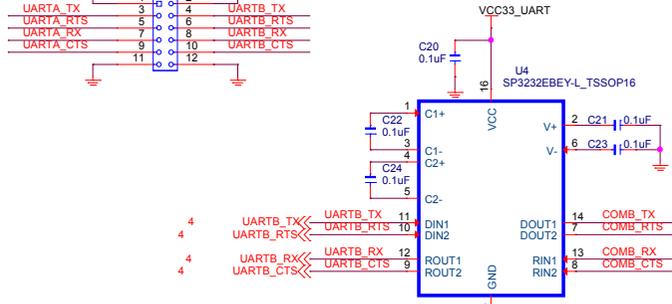
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Date: Wednesday, November 29, 2017 Sheet 5 of 24

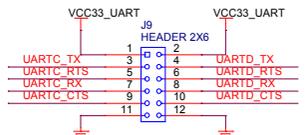
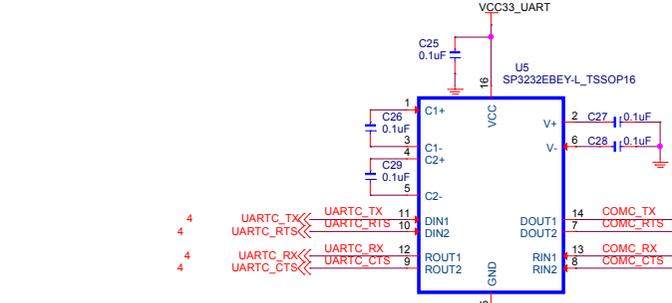
UART



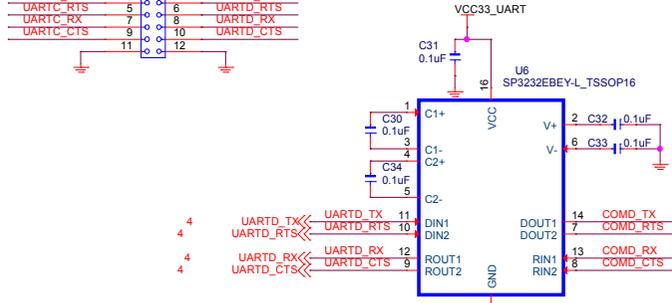
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COMA_CTS	R12	33	COM_A_CTS
COMA_RTS	R13	33	COM_A_RTS



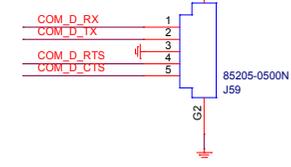
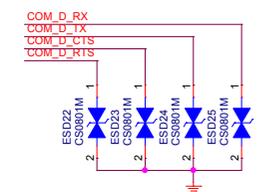
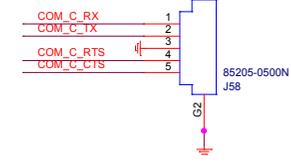
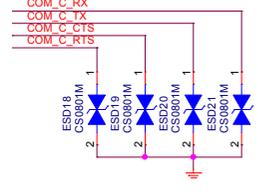
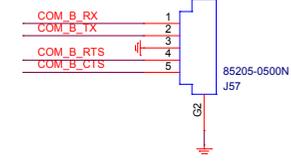
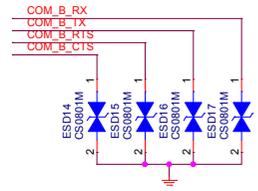
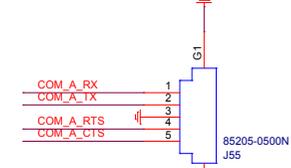
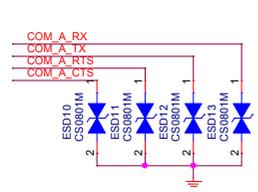
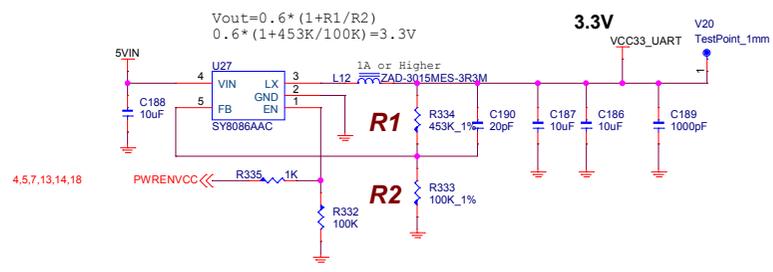
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COMB_TX	R15	33	COM_B_TX
COMB_CTS	R16	33	COM_B_CTS
COMB_RTS	R17	33	COM_B_RTS



COMC_RX	R18	33	COM_C_RX
COMC_TX	R19	33	COM_C_TX
COMC_CTS	R20	33	COM_C_CTS
COMC_RTS	R21	33	COM_C_RTS



COMD_RX	R22	33	COM_D_RX
COMD_TX	R23	33	COM_D_TX
COMD_CTS	R24	33	COM_D_CTS
COMD_RTS	R25	33	COM_D_RTS



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RS-232 Output Conn

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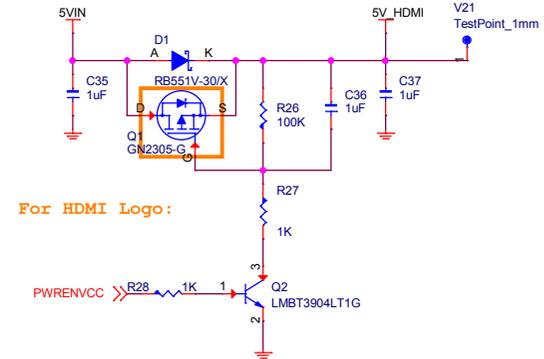
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HDMI

nHDMICLK-	nHDMICLK-	4
nHDMICLK+	nHDMICLK+	4
nHDMIDO-	nHDMIDO-	4
nHDMIDO+	nHDMIDO+	4
nHDMID1-	nHDMID1-	4
nHDMID1+	nHDMID1+	4
nHDMID2-	nHDMID2-	4
nHDMID2+	nHDMID2+	4
nHDMI_CECIN	nHDMICEC	4.7
nHDMIDDCSCL	nHDMIDDCSCL	4.7
nHDMIDDCSDA	nHDMIDDCSDA	4.7
nHDMIHPD	nHDMIHPD	4.7

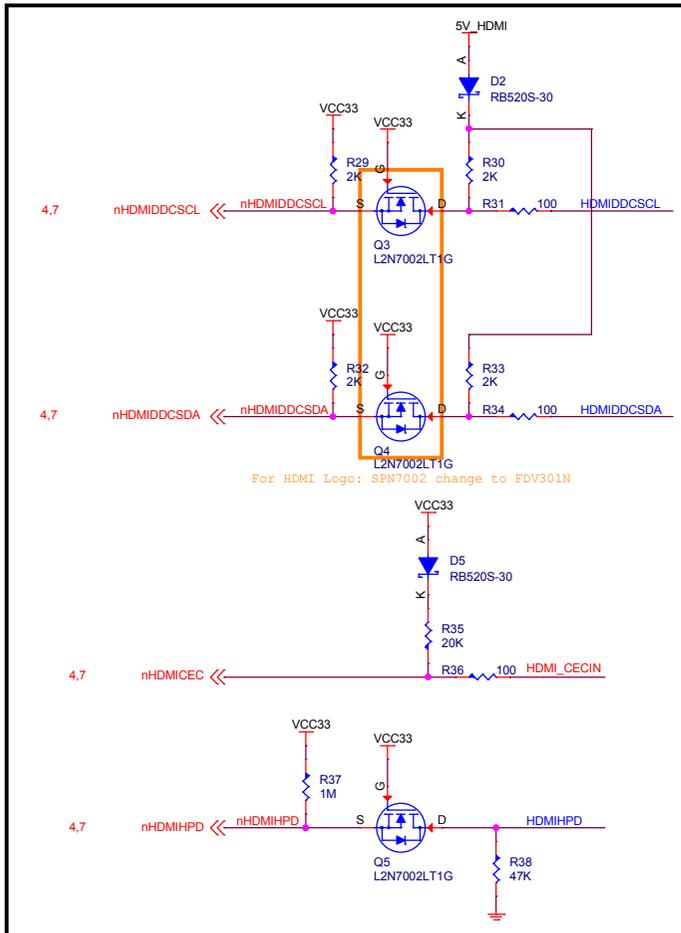
For HDMI Logo:

Signal Name	Length Mismatch (mils)		Total Length (Width : Spacing)
	In Pair	Pair to Pair	
nHDMID[2:0]+/- HDMID[2:0]+/-	< 5	< 100	LT < 3" (5:7:5)
nHDMICLK+/- HDMICLK+/-			

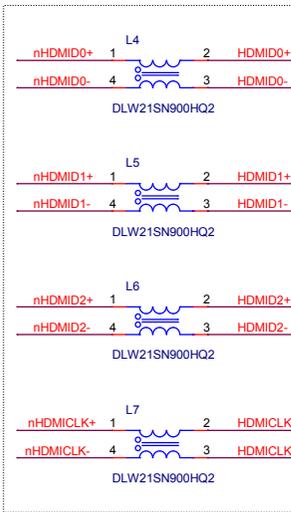


For HDMI Logo:

4,5,6,13,14,18

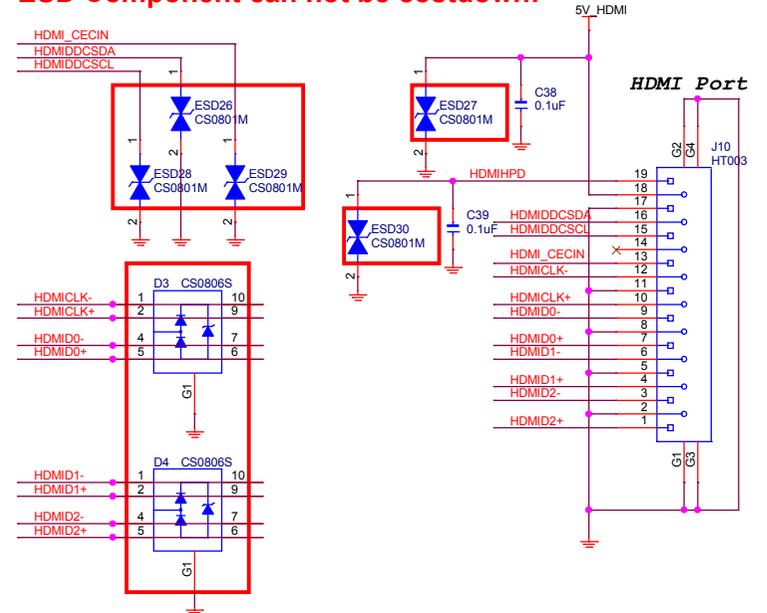


Do not change.



Closed to HDMI connector

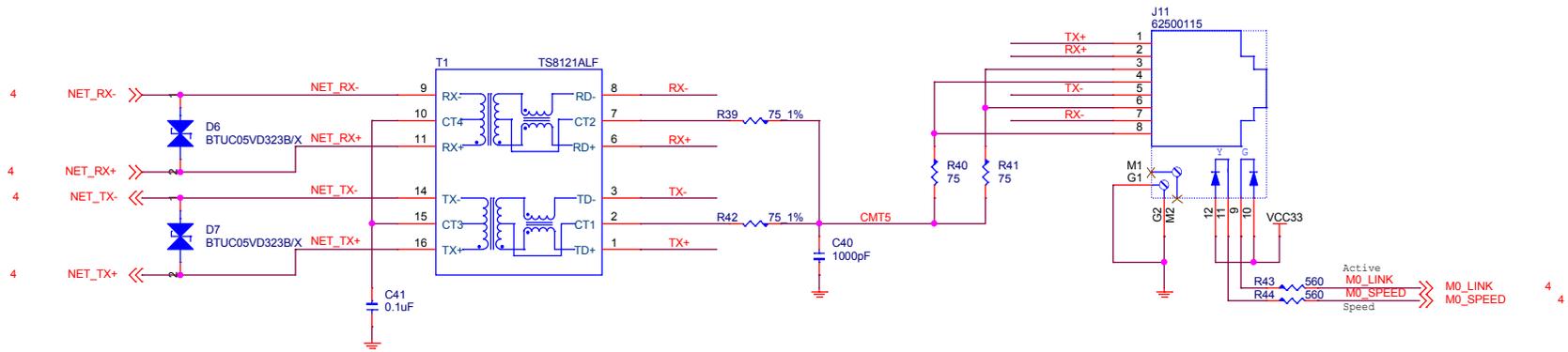
ESD Component can not be costdown!



Notice: ESD components place near HDMI connector.

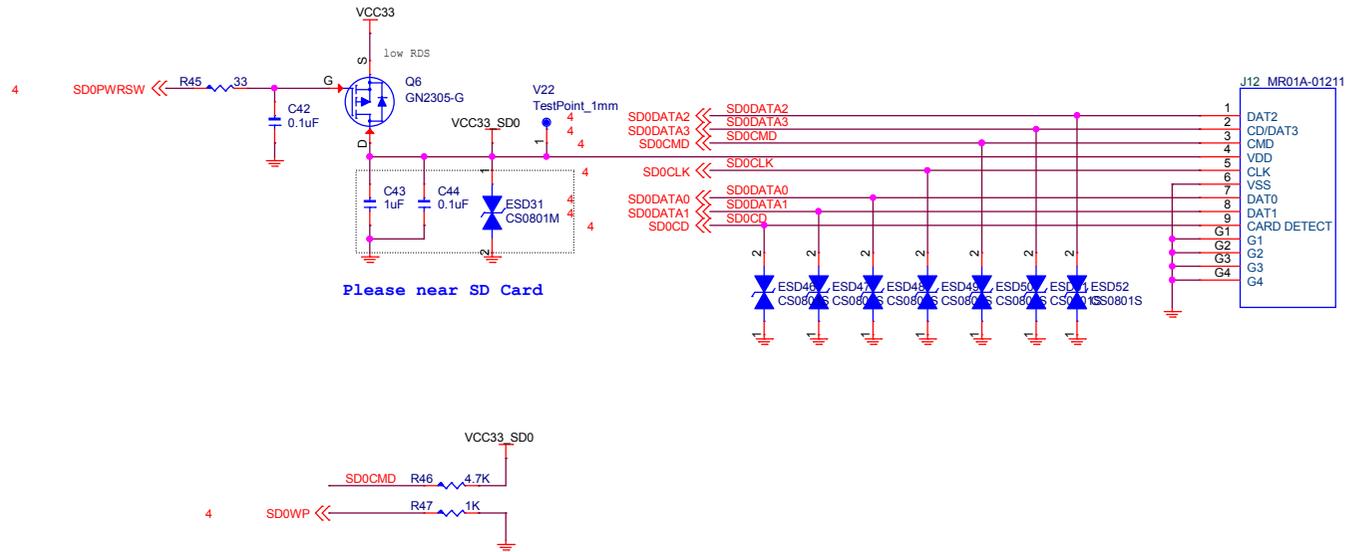
Do not change.

Ethernet

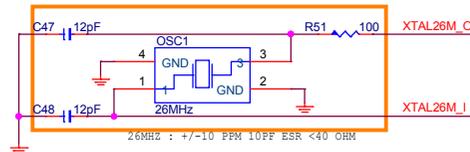
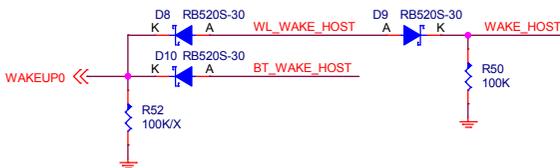
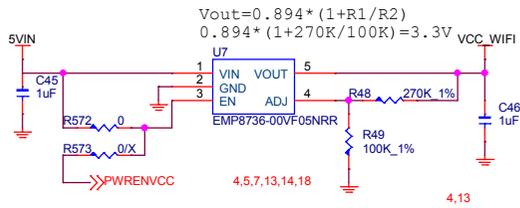


Ethernet		
Title		
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Micro SD

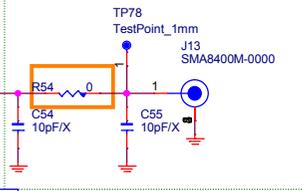


Wi-Fi

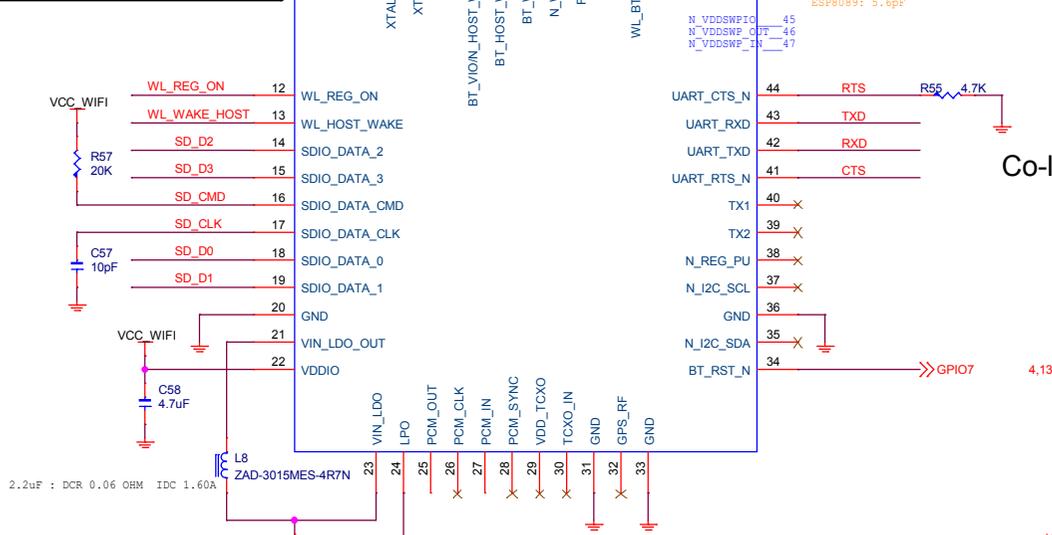


- AP6181/AP6330 :
- OSC2 : 26MHz
- C35/C36 : 3.9pF
- R232 : 100
- ESP8089 :
- OSC2 : 40MHz
- C35/C36 : 15pF
- R232 : 0

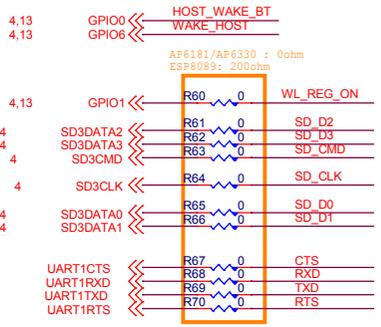
Place close, route short.



Ampak 12*12 Module



Co-layer Design



- ESP8089 (COB) : 2.4GHz WiFi - default
- AP6181 : 2.4GHz WiFi
- AP6330 : 3-in-1 combo 2.4GHz/5GHz WiFi+BT+FM

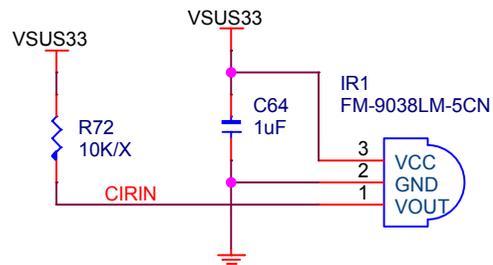
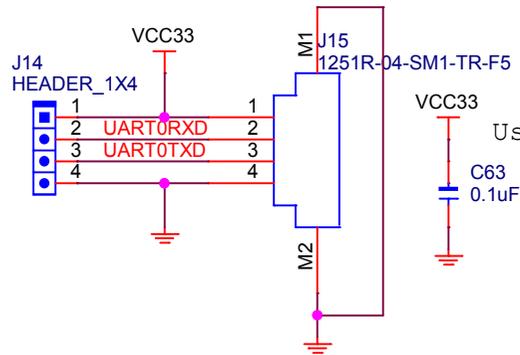
VIA Technologies, Inc.

Title: **SDIO WiFi**

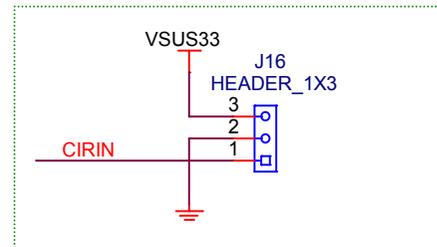
Size: Document Number **VTS8666C** Rev: 1.0

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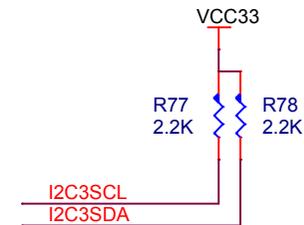
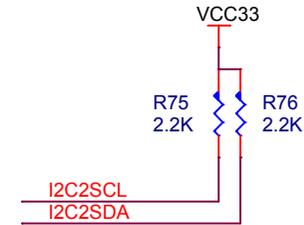
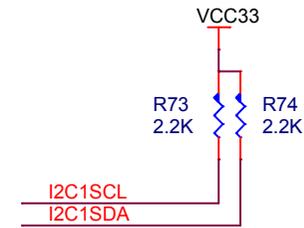
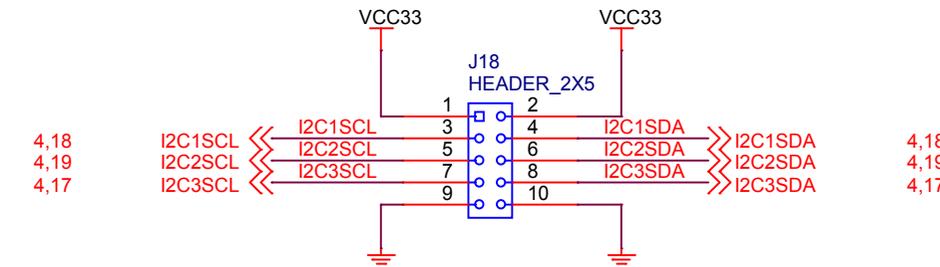
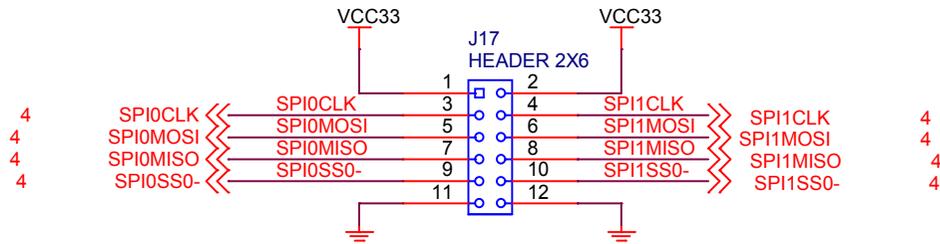
Debug Port and IR



Co-lay With IR1.



Title		
Debug Port and IR		
Size	Document Number	Rev
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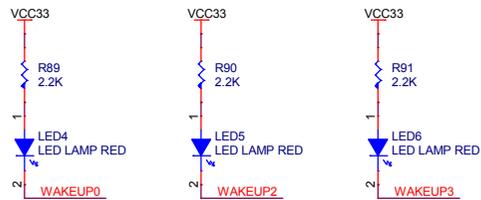
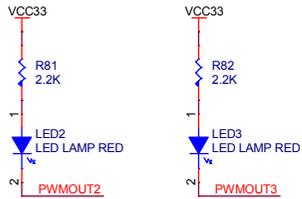
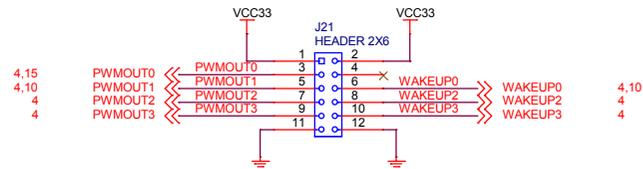
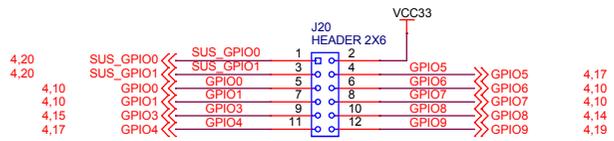
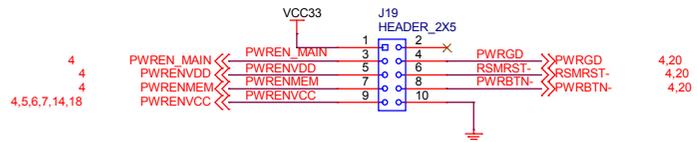


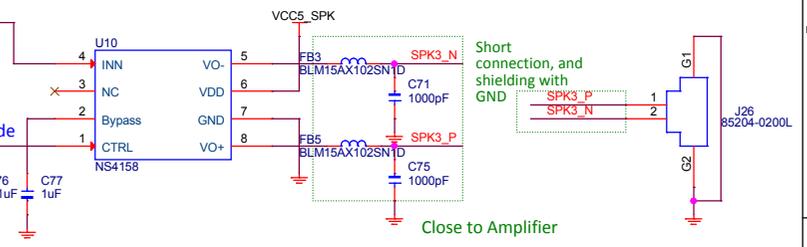
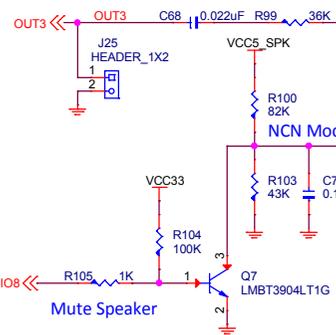
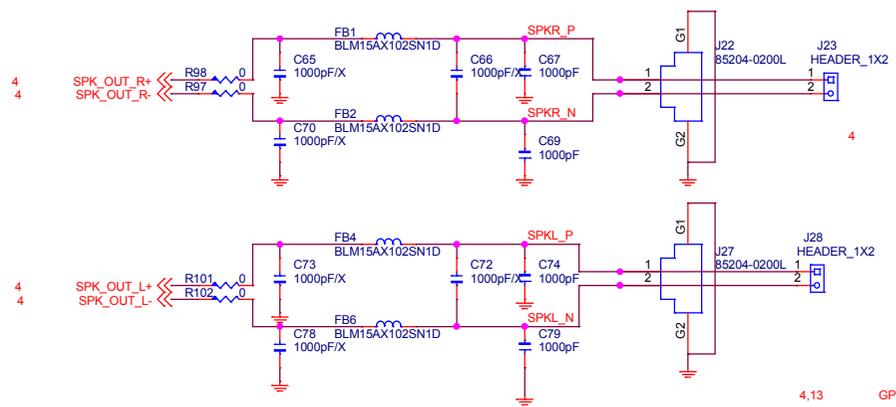
VIA VIA Technologies, Inc. we connect

Title: **SPI & I2C**

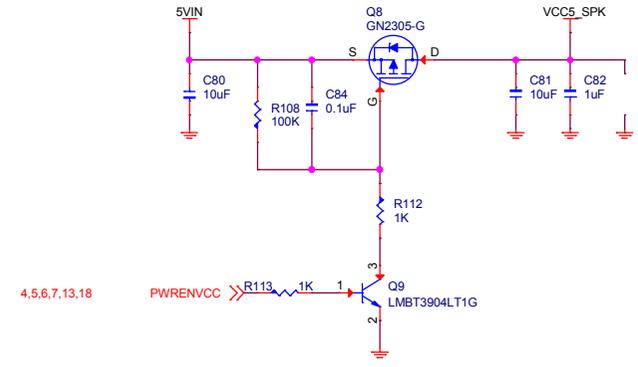
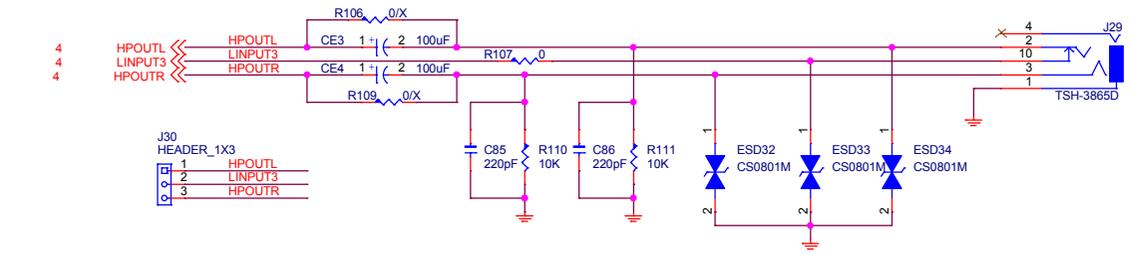
Size	Document Number	Rev
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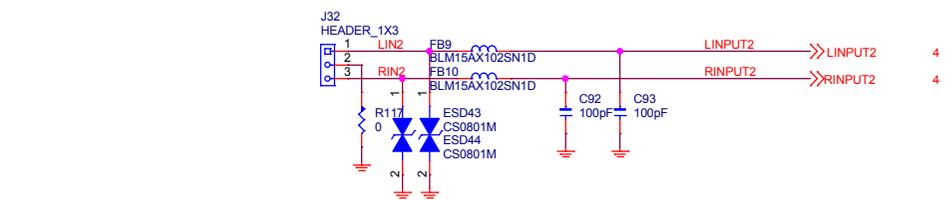
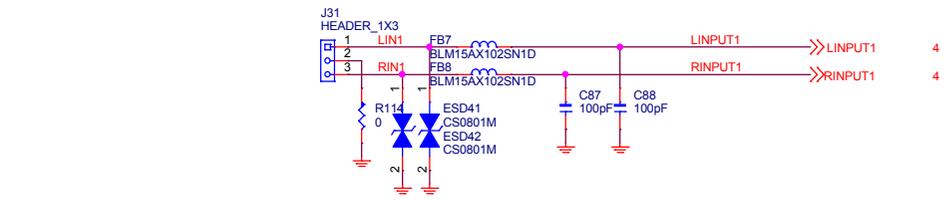




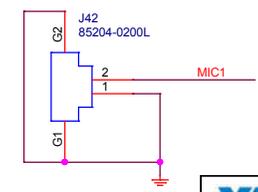
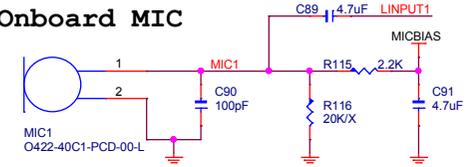
Short connection, and shielding with GND
Close to Amplifier



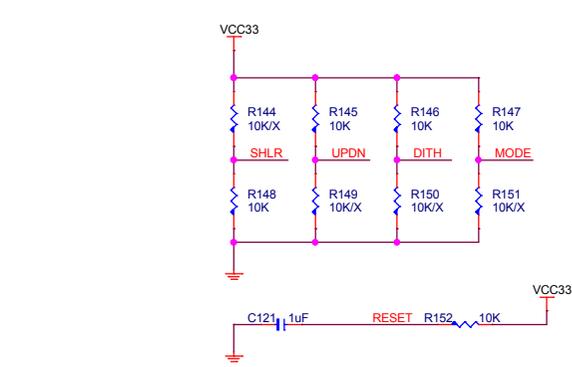
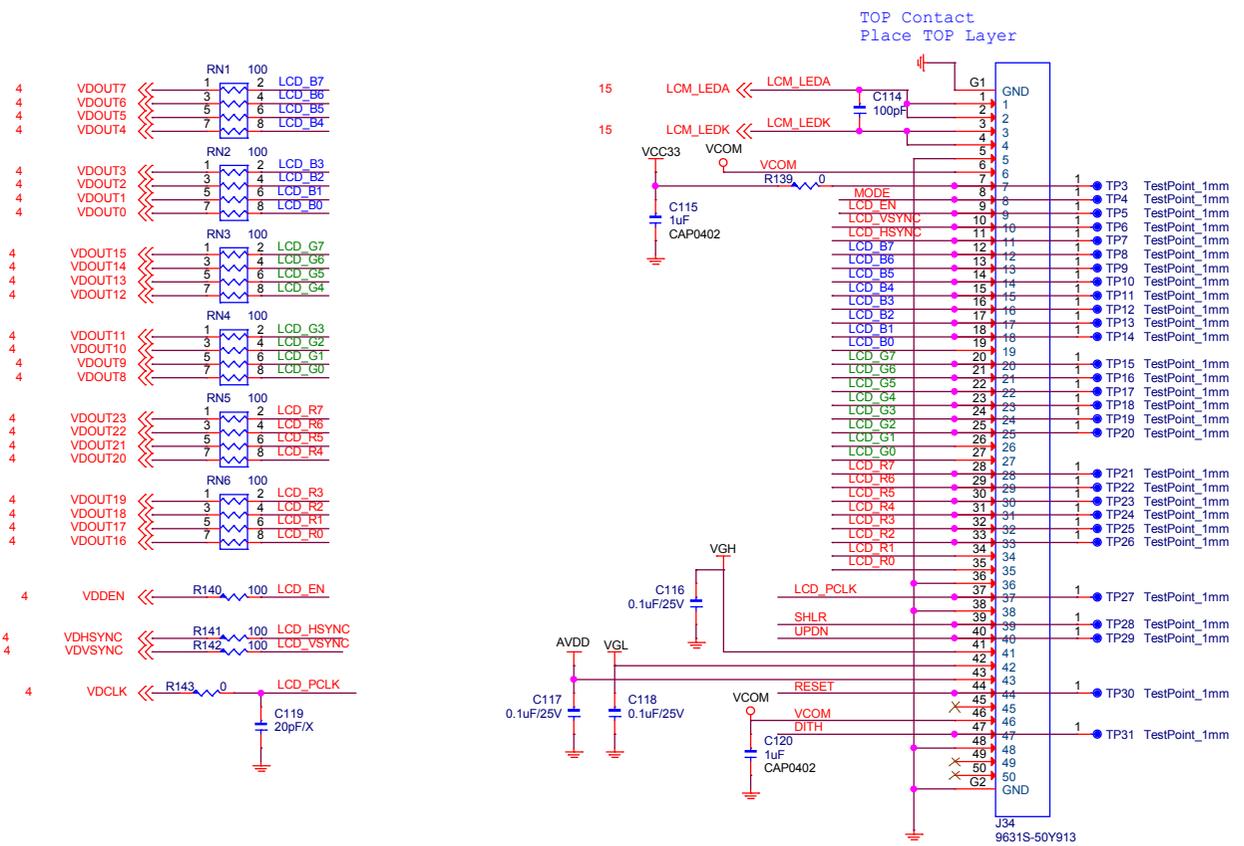
4.5,6,7,13,18



Onboard MIC



Title	SPK & MIC	
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Top Contact

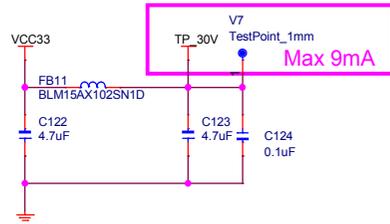
VIA Technologies, Inc.

Title: **LCD I/F**

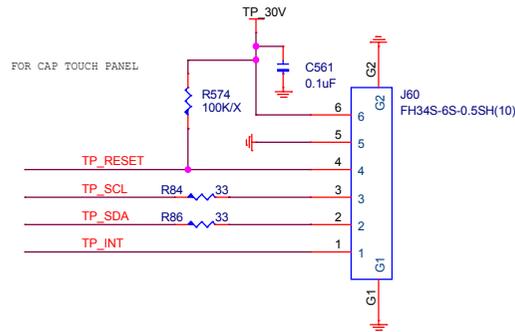
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Touch Panel



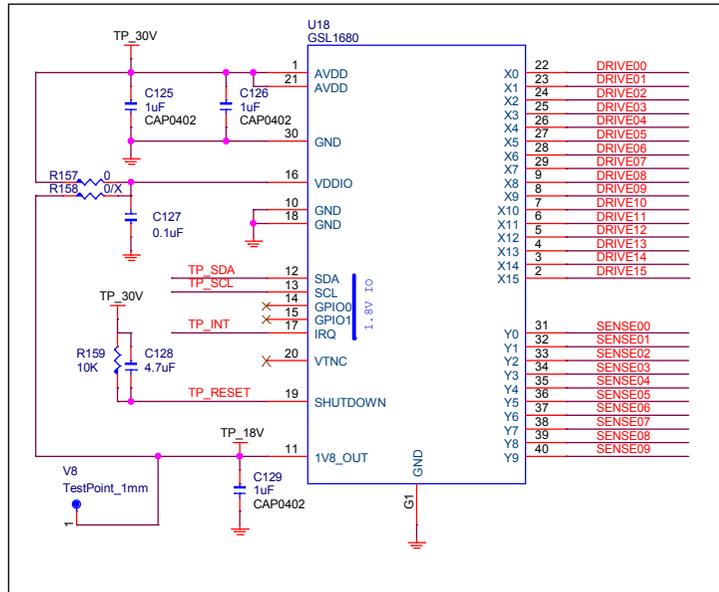
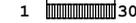
CAP closed to Connector Pins.



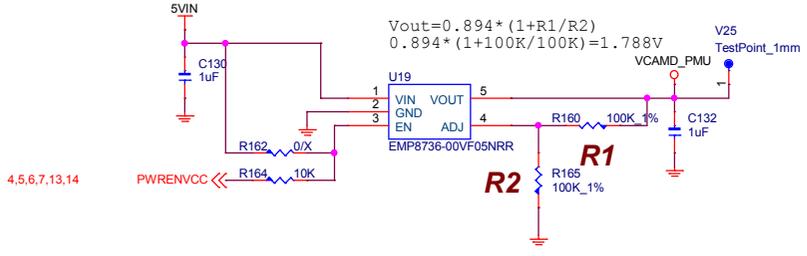
TP_RESET	R153	0	GPIO4	4, 13
TP_INT	R154	0	GPIO5	4, 13
TP_SCL	R155	22	I2C3SCL	4, 12
TP_SDA	R156	22	I2C3SDA	4, 12



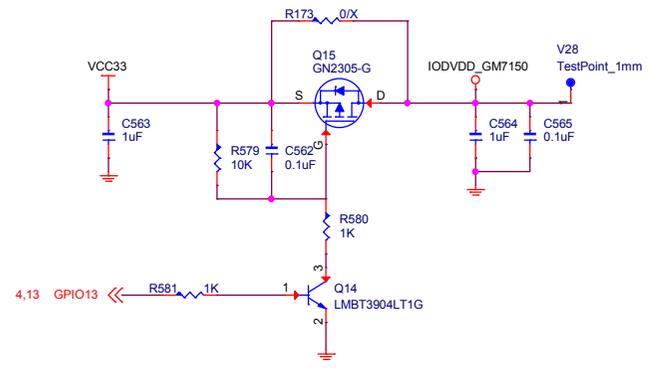
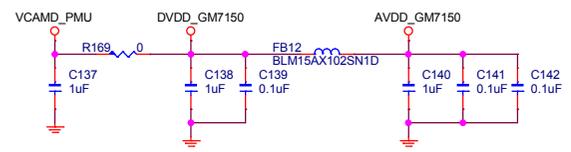
F1 GND
P2-P11 Y9-Y0
P12, P13 GND
P14-P29 X0-X15
P30 GND



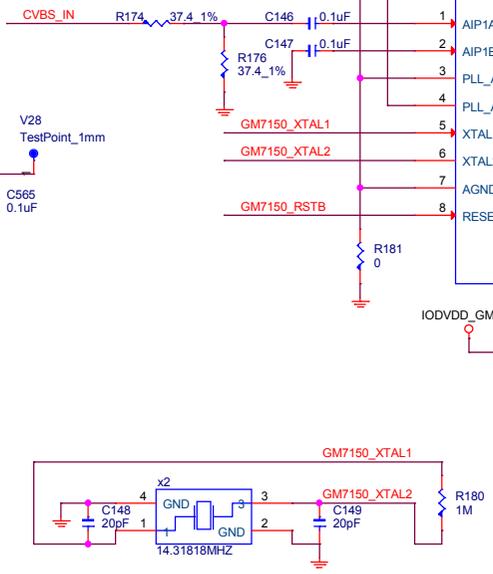
Top Contact



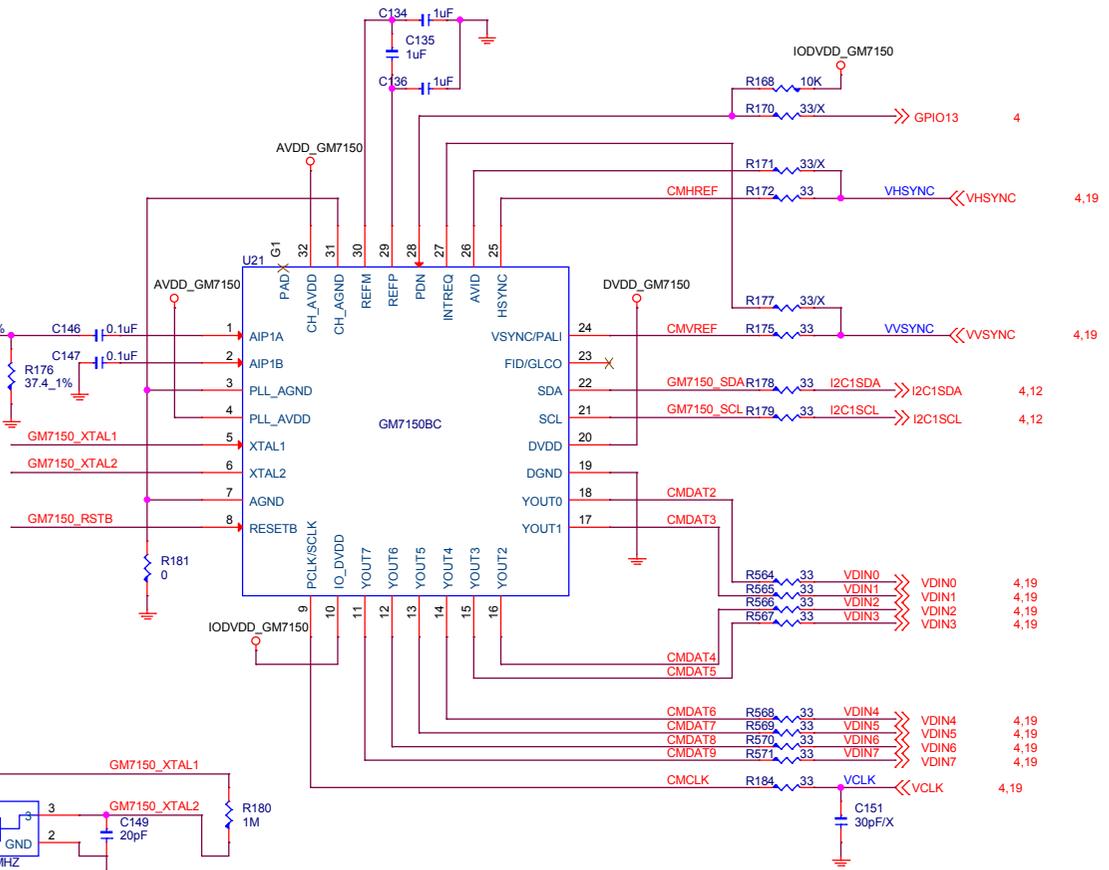
4.5,6,7,13,14



4.13



4.20



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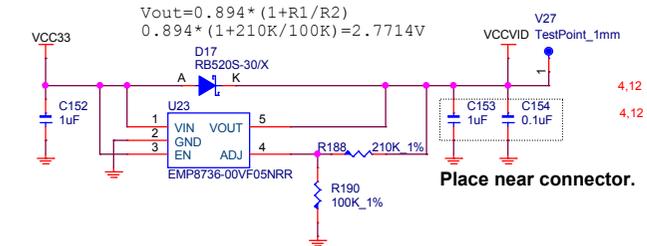
Title: **GM7150BC_Video_Decoder**

Size: Document Number **VTS8666C** Rev: 1.0

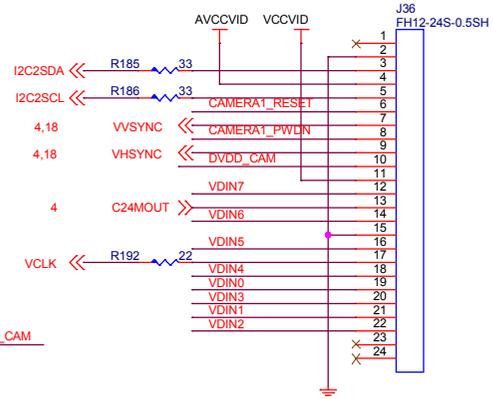
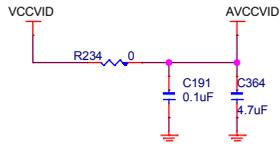
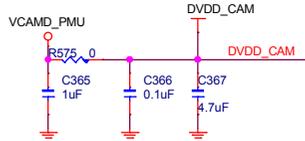
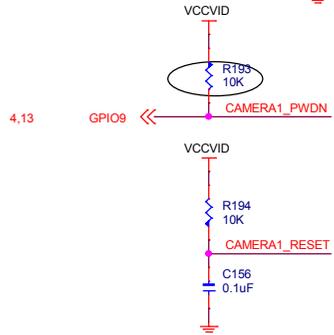
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CCIR656 Camera

I2C Address:
0x42



Place near connector.



- I2C2SDA 1 ● TP60 TestPoint_1mm
- I2C2SCL 1 ● TP62 TestPoint_1mm
- VVSYN 1 ● TP61 TestPoint_1mm
- VHSYN 1 ● TP63 TestPoint_1mm
- CAMERA1_RESET 1 ● TP64 TestPoint_1mm
- C24MOUT 1 ● TP65 TestPoint_1mm
- VCLK 1 ● TP66 TestPoint_1mm
- VDIN7 1 ● TP67 TestPoint_1mm
- VDIN6 1 ● TP68 TestPoint_1mm
- VDIN5 1 ● TP70 TestPoint_1mm
- VDIN4 1 ● TP71 TestPoint_1mm
- VDIN3 1 ● TP72 TestPoint_1mm
- VDIN2 1 ● TP73 TestPoint_1mm
- VDIN1 1 ● TP74 TestPoint_1mm
- VDIN0 1 ● TP75 TestPoint_1mm

VIA Technologies, Inc.

Title: **CCIR656 Camera**

Size: Document Number **VTS8666C** Rev

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