DESIGN GUIDE

Carrier Board

for VIA SOM-6X80 Module

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Revision History

Revision	Date	Description
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1.01	04/24/2020	Updated the reference schematics

Table of Contents

1. Introduction 1
   1.1 Document Overview 1
   1.2 Acronyms Used 2
   1.3 Schematic Conventions 3
2. General Carrier Board Recommendations 4
   2.1 PCB Stackup 4
      2.1.1 4-Layer PCB Stackup Example 5
      2.1.2 4-Layer PCB Impedance Control 5
   2.2 General Layout and Routing Guidelines 6
      2.2.1 Routing Styles and Topology 6
      2.2.2 General Trace Attribute Recommendation 7
      2.2.3 General Clock Routing Considerations 8
3. VIA SOM-6X80 Module and SOM DDR3 SODIMM Slot Specification Overview 9
   3.1 VIA SOM-6X80 Module Placement 9
   3.2 VIA SOM-6X80 Module Mechanical Characteristics 9
   3.3 VIA SOM-6X80 Module and Carrier Board Dimensions 10
   3.4 SOM DDR3 SODIMM Slot 11
      3.4.1 SOM DDR3 SODIMM Slot Dimensions 11
      3.4.2 SOM DDR3 SODIMM Slot Footprint 12
   3.5 SOM DDR3 SODIMM Slot Pin Assignments 13
4. Layout and Routing Recommendation 16
   4.1 HDMI Interface 16
      4.1.1 HDMI Signal Definition 16
      4.1.2 HDMI Layout and Routing Recommendations 17
      4.1.3 HDMI Reference Schematics 19
   4.2 Ethernet Interface 20
      4.2.1 Ethernet Signal Definition 20
      4.2.2 Ethernet Layout and Routing Recommendations 21
      4.2.3 Ethernet Reference Schematics 22
   4.3 USB Interface 23
      4.3.1 USB Signal Definition 23
      4.3.2 USB Layout and Routing Recommendations 24
      4.3.3 USB Reference Schematics 26
   4.4 COM and UART Interface 27
      4.4.1 COM and UART Signal Definition 27
      4.4.2 COM and UART Layout and Routing Recommendations 28
      4.4.3 COM and UART Reference Schematics 29
   4.5 LCD Interface 30
      4.5.1 LCD Signal Definition 30
      4.5.2 LCD Layout and Routing Recommendations 31
      4.5.3 LCD Reference Schematics 32
   4.6 Touch Panel Interface 33
      4.6.1 Touch Panel Signal Definition 33
      4.6.2 Touch Panel Layout and Routing Recommendations 33
      4.6.3 Touch Panel Reference Schematics 34
   4.7 GPIO Interface 35
      4.7.1 GPIO Signal Definition 35
      4.7.2 GPIO Layout and Routing Recommendation 35
   4.8 I²C Interface 36
      4.8.1 I²C Signal Definition 36
      4.8.2 I²C Layout and Routing Recommendation 36
   4.9 SPI Interface 37

4.9.1 SPI Signal Definition 37
4.9.2 SPI Layout and Routing Recommendation 37
4.10 Audio Interface 38
4.10.1 Audio Signal Definition 38
4.10.2 Audio Layout and Routing Recommendations 38
4.10.3 Audio Interface Reference Schematics 39
4.11 SD Interface 41
4.11.1 SD Signal Definition 41
4.11.2 SD Layout and Routing Recommendations 41
4.11.3 SD Interface Reference Schematics 42

List of Figures

Figure 1: Schematic conventions 3
Figure 2: Microstrip PCB stackup example 4
Figure 3: Stripline PCB stackup example 4
Figure 4: 4-Layer PCB board stackup detail 5
Figure 5: Point-to-point and multi-drop examples 6
Figure 6: Daisy-chain example 6
Figure 7: Alternate multi-drop example 6
Figure 8: Signal trace width and spacing example 7
Figure 9: Differential signal trace width and spacing example 7
Figure 10: Suggested clock trace spacing 8
Figure 11: Clock trace layout in relation to the ground plane 8
Figure 12: Series termination for multiple clock loads 8
Figure 13: VIA SOM-6X80 module placement example on the carrier board 9
Figure 14: Carrier board with VIA SOM-6X80 module (side view) 9
Figure 15: Carrier board and VIA SOM-6X80 module height distribution (side view) 9
Figure 16: Dimensions of the VIA SOM-6X80 module 10
Figure 17: Dimensions of the reference carrier board 10
Figure 18: Dimensions of the SOM DDR3 SODIMM slot (top view) 11
Figure 19: Dimensions of the SOM DDR3 SODIMM slot (side view) 11
Figure 20: PCB footprint of the SOM DDR3 SODIMM slot 12
Figure 21: PCB footprint of the SOM DDR3 SODIMM slot with VIA SOM-6X80 module 12
Figure 22: SOM DDR3 SODIMM slot schematics 15
Figure 23: HDMI routing topology 16
Figure 24: HDMI differential trace width and spacing example 17
Figure 25: HDMI single-ended trace width and spacing example 17
Figure 26: HDMI reference circuitry 19
Figure 27: Ethernet routing topology 20
Figure 28: Ethernet single-ended trace width and spacing example 21
Figure 29: Ethernet differential trace width and spacing example 21
Figure 30: Ethernet reference circuitry 22
Figure 31: USB routing topology 23
Figure 32: USB differential signal routing example 24
Figure 33: USB differential trace width and spacing example 24
Figure 34: USB host reference circuitry 26
Figure 35: USB client reference circuitry 26
Figure 36: COM and UART routing topology 28
Figure 37: COM and UART reference circuitry 29
Figure 38: LCD routing topology 30
Figure 39: LCD reference circuitry 32
Figure 40: Touch panel routing topology 33
Figure 41: Touch panel reference circuitry 34
Figure 42: Line-in 1 & 2 reference circuitry 39
Figure 43: Headphone reference circuitry 39
Figure 44: Mono speaker out reference circuitry 39
Figure 45: Right channel speaker out reference circuitry 40
Figure 46: Left channel speaker out reference circuitry 40
Figure 47: Onboard microphone reference circuitry 40
Figure 48: SD routing topology 41
Figure 49: SD reference circuitry 42

List of Tables

Table 1: Acronyms used 2
Table 2: 4-Layer PCB impedance control 5
Table 3: Recommended trace width and spacing 7
Table 4: SOM DDR3 SODIMM slot sample 11
Table 5: SOM DDR3 SODIMM slot pinouts 14
Table 6: HDMI signal definition 16
Table 7: HDMI trace properties 17
Table 8: HDMI layout guidelines 18
Table 9: HDMI routing topology and signal type 18
Table 10: Ethernet signal definition 20
Table 11: Ethernet trace properties 22
Table 12: Ethernet layout guidelines 22
Table 13: Ethernet reference plane, signal type and routing topology 22
Table 14: USB signal definition 23
Table 15: USB trace properties 25
Table 16: USB termination option, signal type and routing topology 25
Table 17: USB layout guidelines 25
Table 18: COM and UART signal definition 27
Table 19: COM and UART trace properties 28
Table 20: COM and UART topology, signal type and layout guidelines 29
Table 21: LCD signal definition 30
Table 22: LCD trace properties 31
Table 23: LCD signal type, topology and reference plane 31
Table 24: LCD layout guidelines 32
Table 25: Touch panel signal definition 33
Table 26: Touch panel trace properties 33
Table 27: Touch panel signal type, routing topology and reference plane 33
Table 28: Touch panel layout guidelines 34
Table 29: GPIO signal definition 35
Table 30: GPIO trace properties 35
Table 31: GPIO signal type, topology and layout guidelines 35
Table 32: I²C signal definition 36
Table 33: I²C trace properties 36
Table 34: I²C signal type, topology and layout guidelines 36
Table 35: SPI signal definition 37
Table 36: SPI trace properties 37
Table 37: SPI signal type, topology and layout guidelines 37
Table 38: Audio signal definition 38
Table 39: Audio trace properties 38
Table 40: Audio signal type, topology and layout guidelines 39
Table 41: SD signal definition 41
Table 42: SD trace properties 42
Table 43: SD signal type, topology and layout guidelines 42

1. Introduction

This document provides design guidelines and rule recommendations for the developers of a carrier board that supports the features of the VIA SOM-6X80 module. This document includes the layout and routing guidelines for general board designs and major underlying interfaces (e.g. HDMI, Ethernet, USB). In addition, the document includes the placement and mechanical information on the SOM DDR3 SODIMM slot which is used to provide high-speed interfaces between the carrier board and the module.

Please note that this document is considered to be a reference guide only. This document is not intended to be a specification. All information and examples listed below are considered to be accurate as of the publication date. However, developers must be aware that this document is only a reference guide.

1.1 Document Overview

A brief description of each chapter is given below.

Chapter 1: Introduction

This chapter briefly introduces the structure of the design guide document.

Chapter 2: General Carrier Board Recommendations

The general design schemes and recommended layout rules are shown in this chapter.

Chapter 3: VIA SOM-6X80 Module and SOM DDR3 SODIMM Slot Specification Overview

Detailed information about the VIA SOM-6X80 module and SOM DDR3 SODIMM slot placement and dimensions are described in this chapter.

Chapter 4: Layout and Routing Recommendations

Detailed layout and routing guidelines for each major interface are described in this chapter.

1.2 Acronyms Used

Term	Description
ASIC	Application-specific Integrated Circuit
DDR	Double Data Rate
EMI	Electromagnetic Interference
ESD	Electrostatic-discharge
GPIO	General Purpose Input/Output
HDMI	High-Definition Multimedia Interface
I^2C	Inter-IC
IC	Integrated Circuit
LCD	Liquid-Crystal Display
LVDS	Low-Voltage Differential Signaling
P2P	Point-to-Point
PCB	Printed Circuit Board
RGB	Red, Green and Blue
RJ-45	Registered Jack 45
RS-232	Recommend Standard number 232
SD	Secure Digital
SODIMM	Small Outline Dual In-line Memory Module
SMT	Surface Mount Technology
SOM	System-On-Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USB OTG	USB On-The-Go

Table 1: Acronyms used

1.3 Schematic Conventions

The reference schematics depicted in this document show the directional flow of the signals. Directional flow is indicated by the pointed ends of the arrow shapes.

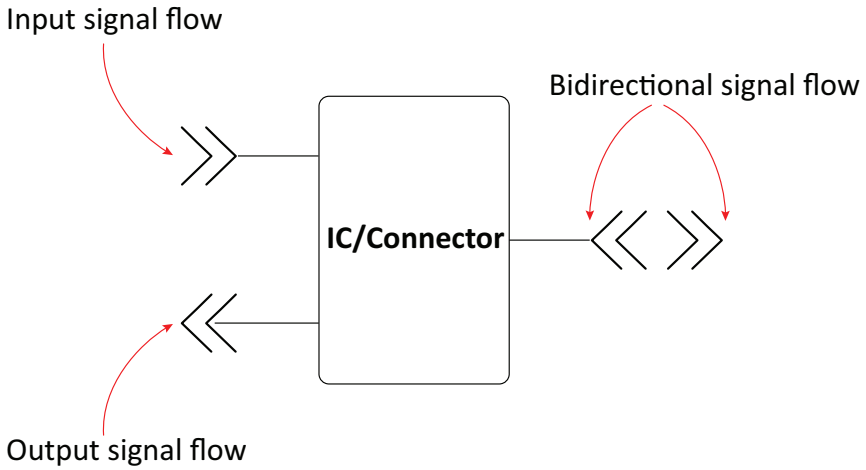

Figure 1: Schematic conventions

2. General Carrier Board Recommendations

This section contains general guidelines for the PCB stackup and the layout of traces. The general guidelines for routing style, topology, and trace attribute recommendations are also discussed.

2.1 PCB Stackup

The PCB stackup consists of signal layers and reference layers (power and ground). The signal layers are referred to as the component layer (top), inner layer and solder layer (bottom).

The carrier board designers can choose between two basic categories of PCB stackup design: microstrip and stripline. The microstrip designs have the outer signal layers exposed. The stripline designs have the outermost signal layers shielded by reference layers.

The following figures show an example of microstrip and stripline designs.

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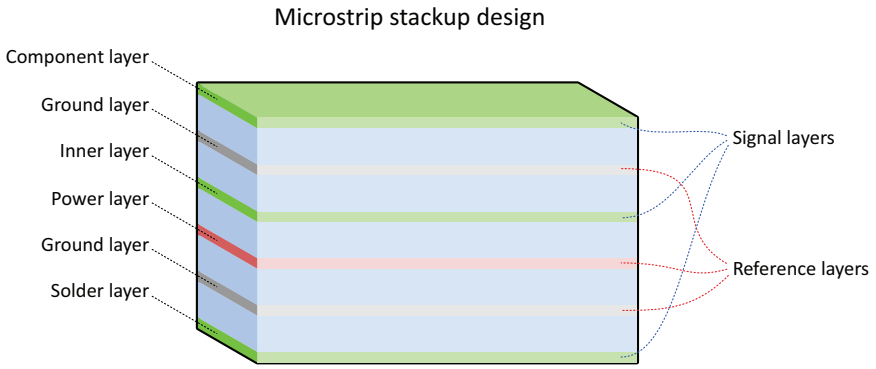


Figure 2: Microstrip PCB stackup example

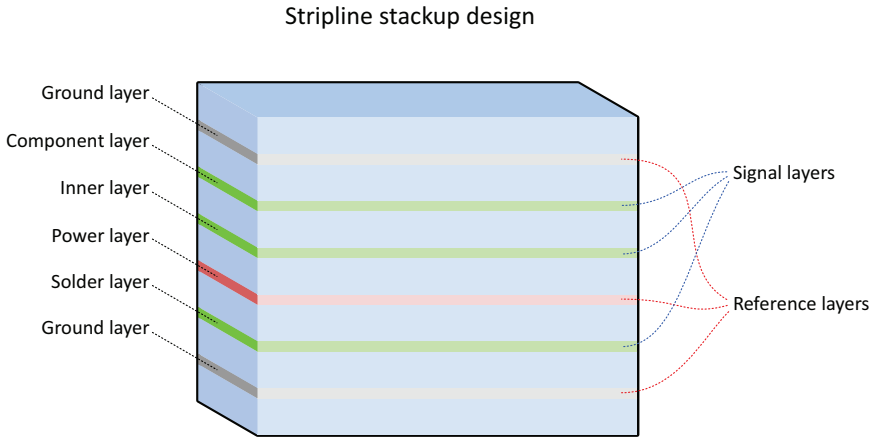


Figure 3: Stripline PCB stackup example

The choice of microstrip or stripline design depends on the application for which the carrier board is being designed. If the carrier board is being designed for locations where sensitivity to EMI is an issue, a stripline design is recommended for reducing EMI and noise coupling. For applications where the tolerance for EMI levels is greater, a microstrip design is recommended to reduce costs. Due to the inherent nature of stripline PCB stacks, broad-side coupling is possible.

2.1.1 4-Layer PCB Stackup Example

The following figure shows the recommended 4-layer PCB stackup design for the carrier board of the VIA SOM-6X80 module.

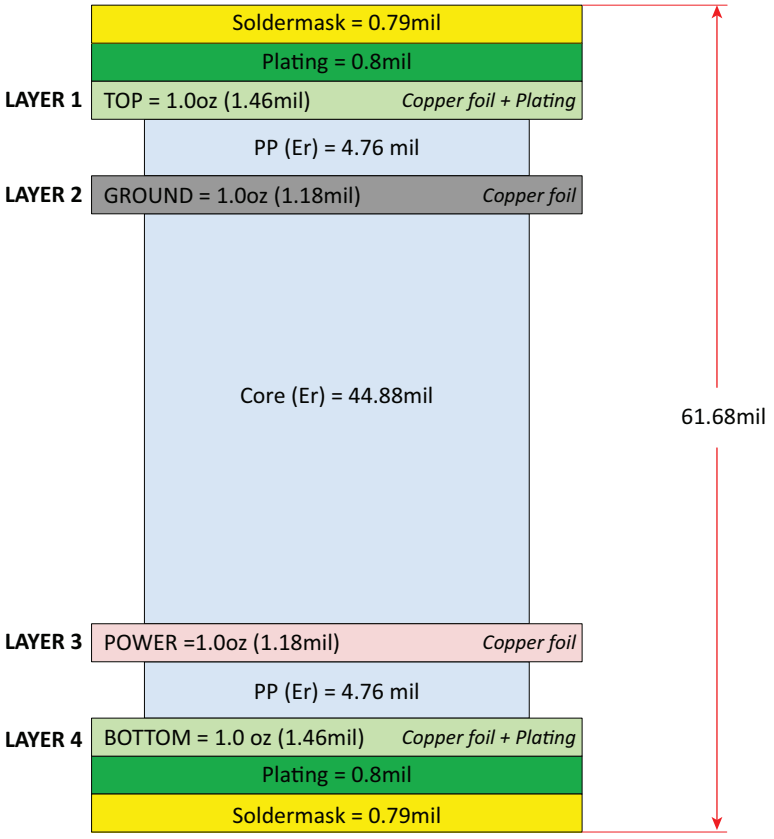


Figure 4: 4-Layer PCB board stackup detail

2.1.2 4-Layer PCB Impedance Control

± 10%	40Ω Single-end	50Ω Single-end	55Ω Single-end	85Ω Differential	90Ω Differential	90Ω Differential
Layer 1	12mil	8mil	7mil	7.8 : 9 : 7.8 mil	7.6 : 8 : 7.6 mil	7 : 7.5 : 7 mil
Layer 4	12mil	8mil	7mil	7.8 : 9 : 7.8 mil	7.6 : 8 : 7.6 mil	7 : 7.5 : 7 mil

Table 2: 4-Layer PCB impedance control

2.2 General Layout and Routing Guidelines

This section provides general layout rules and routing guidelines for designing carrier boards for the VIA SOM-6X80 module.

2.2.1 Routing Styles and Topology

Topology is the physical connectivity of a net or a group of nets. There are two types of topologies for a carrier board layout: point-to-point (P2P) and multi-drop. An example of these topologies is shown in Figure 5.

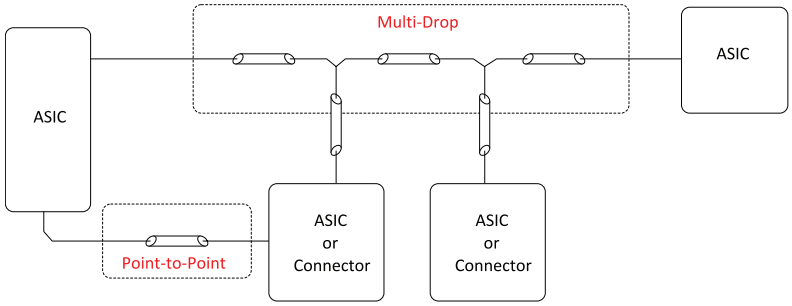


Figure 5: Point-to-point and multi-drop examples

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept as short as possible (less than 1.5”). Therefore, daisy chain style routing is strongly recommended for these signals. Figure 6 below shows an example of daisy chain routing.

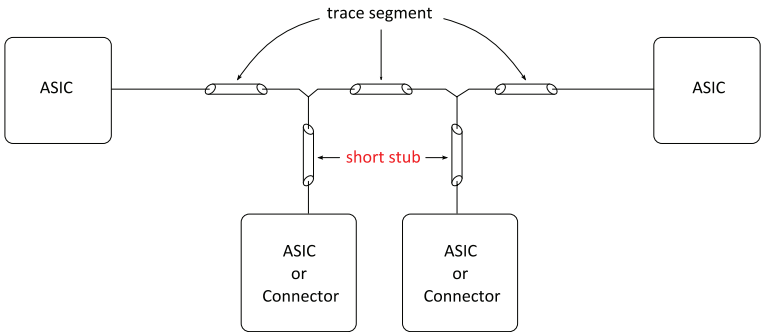


Figure 6: Daisy-chain example

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 7. In this case, the branch point is somewhere between both ends. It may be near the source or near the loads, but being close to the load side is best. The separated traces should be equal in length.

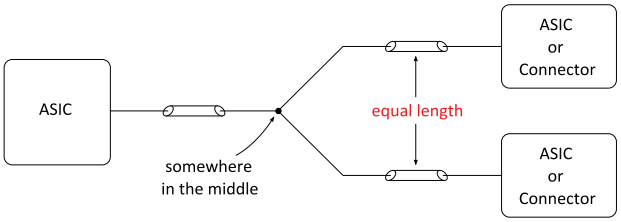


Figure 7: Alternate multi-drop example

2.2.2 General Trace Attribute Recommendation

A 5mil trace width and 10mil spacing are generally advised for most signal traces on a carrier board layout. To reduce trace inductance the minimum power trace width is recommended to be 30mil.

As a quick reference, the overall recommended trace width and spacing for different trace types are listed in Table 3, and the recommended trace width and spacing for each signal group is shown in Chapter 4.

Trace Type	Trace Width (mil)	Spacing (mil)
Regular Signal	5 or wider	10 or wider
Interface or Bus Reference Voltage Signal	20 or wider	20 or wider
Power	30 or wider	20 or wider

Table 3: Recommended trace width and spacing

General rules for minimizing crosstalk in high-speed bus designs are listed below:

- Maximize the distance between traces. Maintain 10mil minimum spaces between traces wherever possible.
- Maximize the distance (30mil minimum) between two adjacent routing areas of different signal groups wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Provide stable reference planes for all high-speed signals.
- Never route high-speed signals over splits in their perspective reference planes.
- Select a board stack-up that minimizes coupling between adjacent traces.

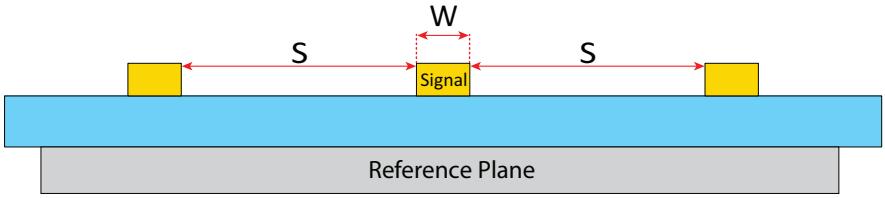


Figure 8: Signal trace width and spacing example

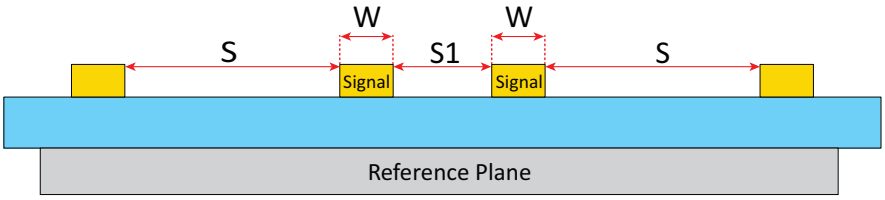


Figure 9: Differential signal trace width and spacing example

Notes:
1. W: Trace width
2. S: The spacing to other traces
3. S1: Differential pair spacing

2.2.3 General Clock Routing Considerations

The clock routing guidelines are listed below:

- The recommended clock trace width is 5mil.
- The minimum space between one clock trace and adjacent clock traces is 20mil. The minimum space from one segment of a clock trace to other segments of the same clock trace is at least two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 10).
- The clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 11).
- The series terminations (damping resistors) are needed for all clock signals (typically 0Ω to 47Ω). When two loads are driven by one clock signal, the series termination layout is shown in Figure 12. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20mil to 50mil wide) is preferred.
- No clock traces on the internal layer if a six-layer board is used.

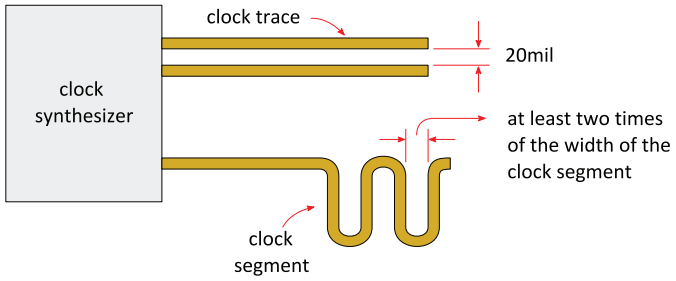


Figure 10: Suggested clock trace spacing

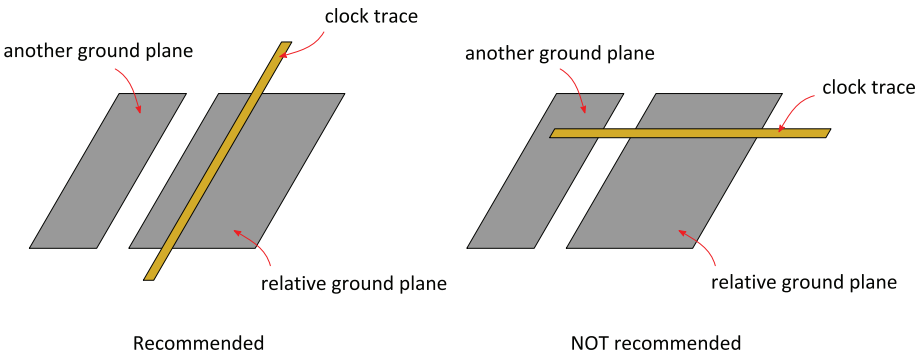


Figure 11: Clock trace layout in relation to the ground plane

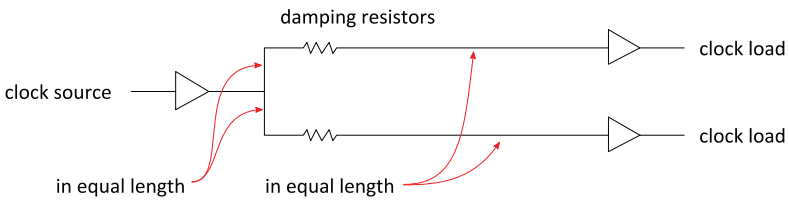


Figure 12: Series termination for multiple clock loads

3. VIA SOM-6X80 Module and SOM DDR3 SODIMM Slot Specification Overview

3.1 VIA SOM-6X80 Module Placement

The following figure shows the depiction of the top view of the carrier board PCB (SOMDB3) with the appropriate amount of space reserved for the VIA SOM-6X80 module.

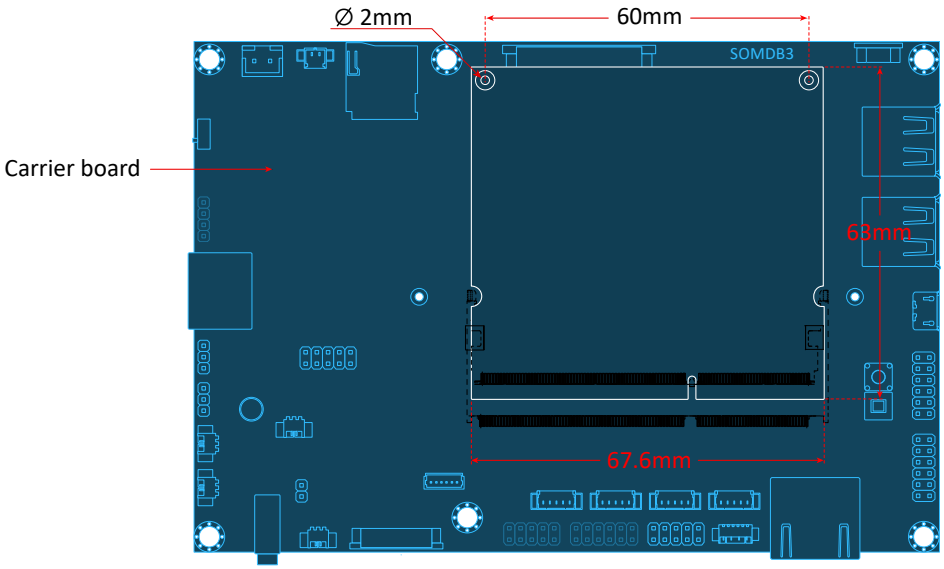


Figure 13: VIA SOM-6X80 module placement example on the carrier board

3.2 VIA SOM-6X80 Module Mechanical Characteristics

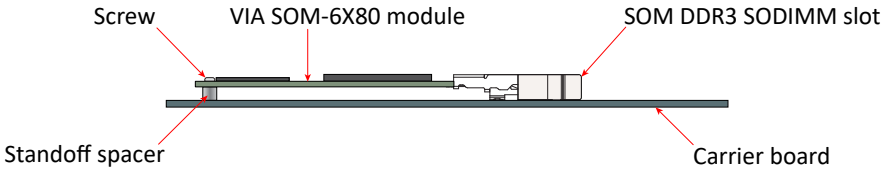


Figure 14: Carrier board with VIA SOM-6X80 module (side view)

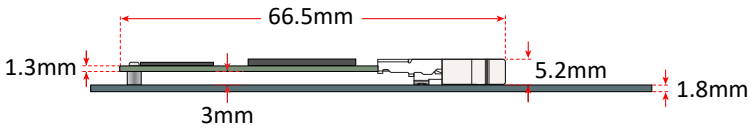


Figure 15: Carrier board and VIA SOM-6X80 module height distribution (side view)

3.3 VIA SOM-6X80 Module and Carrier Board Dimensions

The following figures show the mechanical dimensions of the VIA SOM-6X80 module and the reference carrier board (SOMDB3).

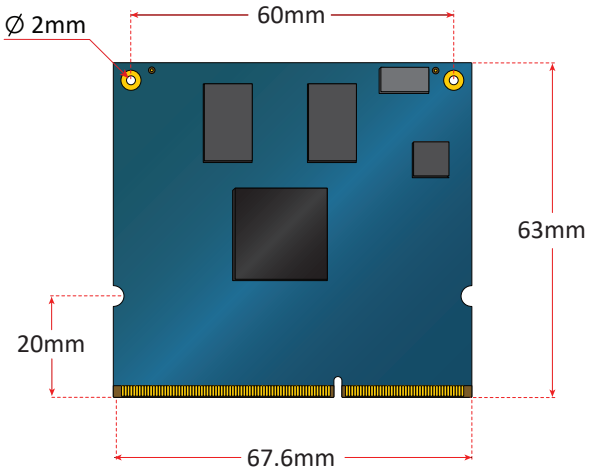


Figure 16: Dimensions of the VIA SOM-6X80 module

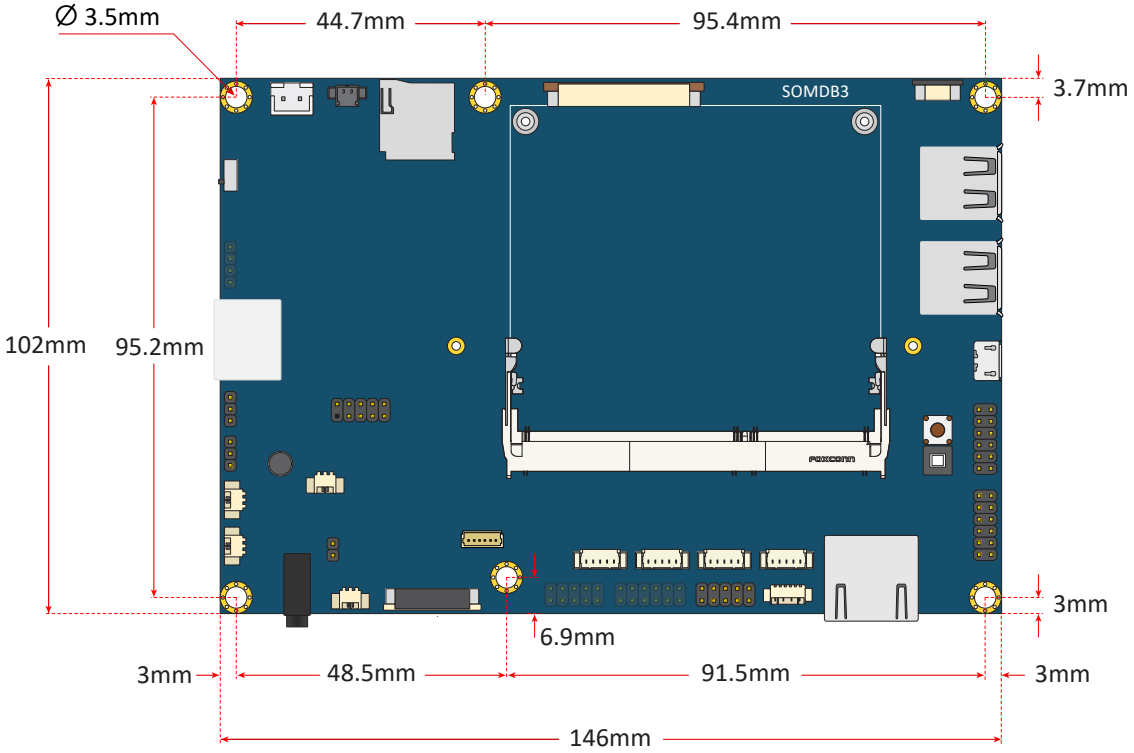


Figure 17: Dimensions of the reference carrier board

3.4 SOM DDR3 SODIMM Slot

The SOM DDR3 SODIMM slot can handle high-speed signals and comprises 204 pins to connect the VIA SOM-6X80 module. Table 4 shows the specification sample of the SOM DDR3 SODIMM slot.

Part Number	Description	Height	Vendor
AS0A626-H2R6-7H	DDR3 SODIMM 10u" Gold Plating 5.2mmH Connector	5.2mm	Foxconn

Table 4: SOM DDR3 SODIMM slot sample

3.4.1 SOM DDR3 SODIMM Slot Dimensions

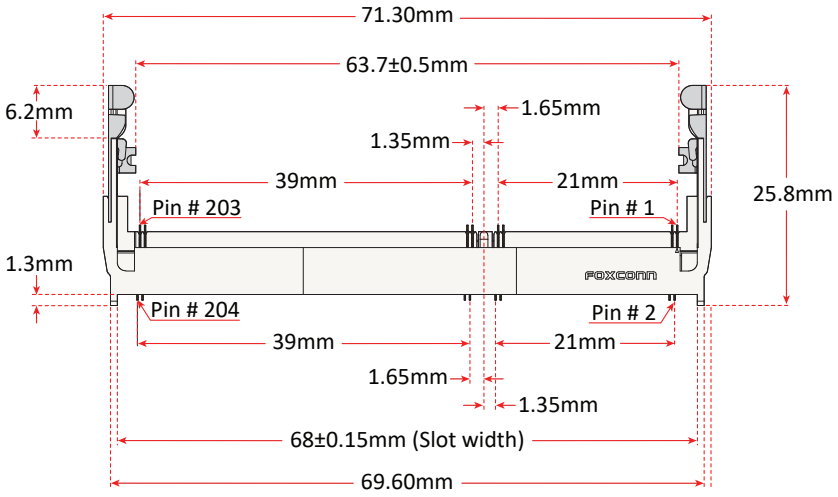


Figure 18: Dimensions of the SOM DDR3 SODIMM slot (top view)

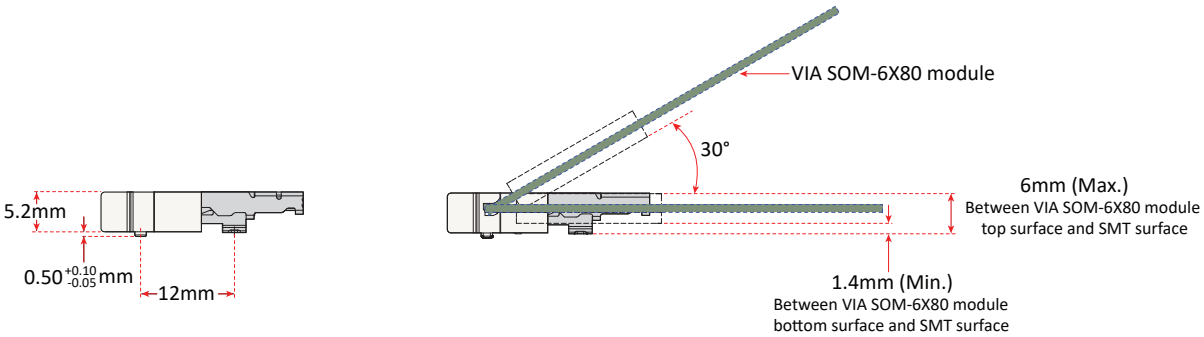


Figure 19: Dimensions of the SOM DDR3 SODIMM slot (side view)

3.4.2 SOM DDR3 SODIMM Slot Footprint

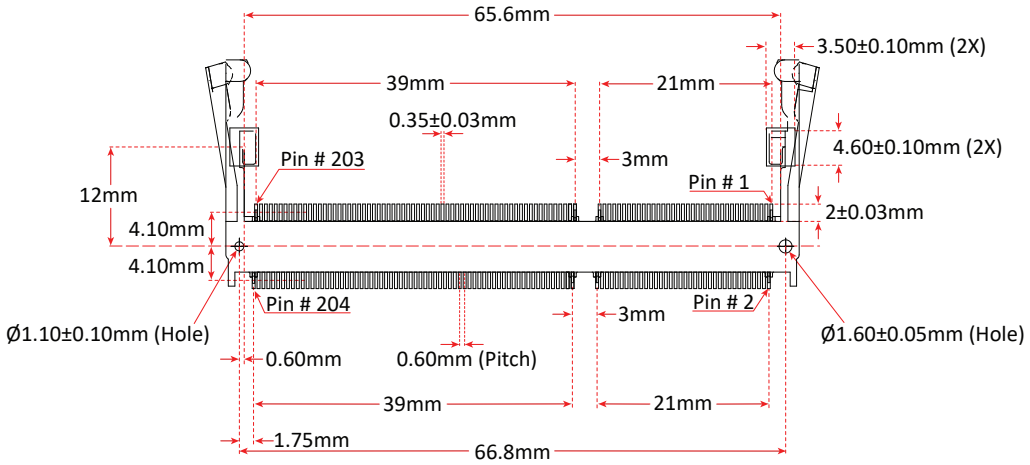


Figure 20: PCB footprint of the SOM DDR3 SODIMM slot

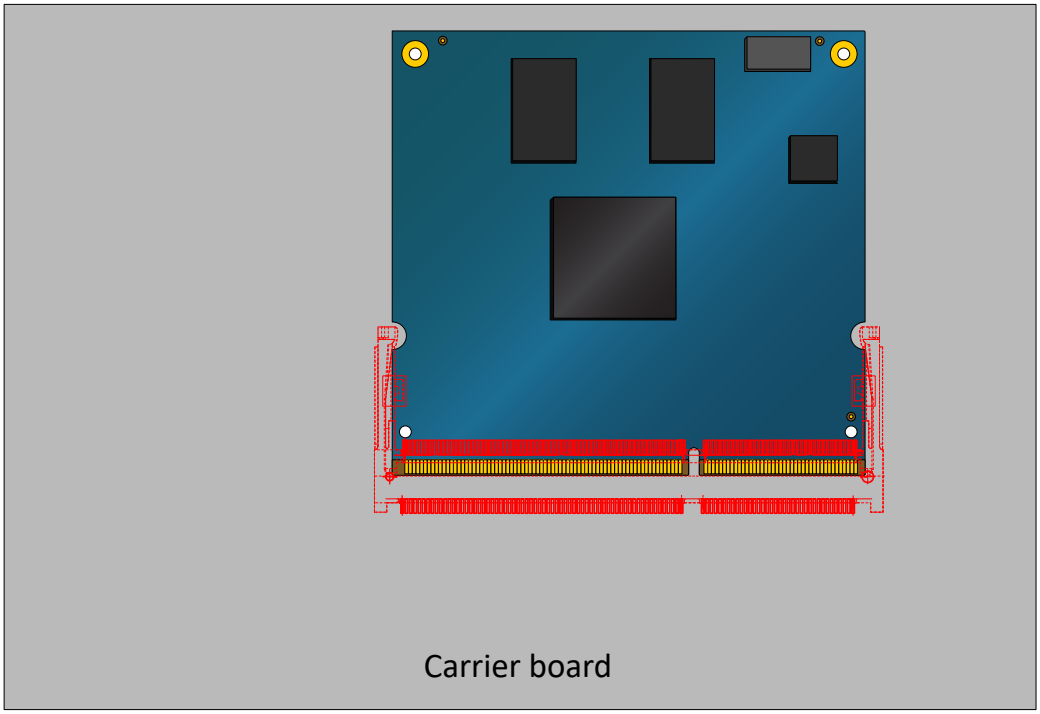


Figure 21: PCB footprint of the SOM DDR3 SODIMM slot with VIA SOM-6X80 module

3.5 SOM DDR3 SODIMM Slot Pin Assignments

The SOM DDR3 SODIMM slot consists of 204 pins. The pinouts of the SOM DDR3 SODIMM slot are shown below.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SPK_OUT_R-	4	MICBIAS
5	SPK_OUT_R+	6	GND
7	SPK_OUT_L-	8	LINPUT2
9	SPK_OUT_L+	10	LINPUT3
11	HPOUTR	12	LINPUT1
13	OUT3	14	RINPUT2
15	HPOUTL	16	RINPUT1
17	GND	18	GND
19	GND	20	GND
21	GND	22	GND
23	I2C0SCL	24	nUSBHB+
25	I2C0SDA	26	nUSBHB-
27	USBSW0	28	GND
29	USBATTA0	30	nUSBHA+
31	USBID0	32	nUSBHA-
33	GND	34	GND
35	GPIO2	36	nUSBHD0-
37	M0_LINK	38	nUSBHD0+
39	M0_SPEED	40	GND
41	GPIO1	42	nUSB2+
43	GPIO5	44	nUSB2-
45	GPIO3	46	GND
47	GND	48	VCC-BAT
49	NET_RX+	50	GND
51	NET_RX-	52	SPI0MOSI
53	GND	54	SPI0CLK
55	NET_TX+	56	SPI0MISO
57	NET_TX-	58	SPI0SS0-
59	GND	60	GND
61	SUS_GPIO0	62	UART1RTS
63	WAKEUP0	64	UART1CTS
65	SUS_GPIO1	66	NC
67	NC	68	NC
69	GPIO4	70	NC
71	WAKEUP3	72	GND
73	WAKEUP2	74	GND
75	GPIO0	76	LCD1CLK-
77	GPIO6	78	LCD1CLK+

Pin	Signal	Pin	Signal
79	GND	80	GND
81	UART1RXD	82	LCD1DO0-
83	UART1TXD	84	LCD1DO0+
85	GND	86	GND
87	SPI1CLK	88	LCD1DO1-
89	SPI1SS0-	90	LCD1DO1+
91	SPI1MISO	92	GND
93	SPI1MOSI	94	LCD1DO3+
95	GND	96	LCD1DO3-
97	NC	98	GND
99	NC	100	LCD1DO2+
101	PWRENVCC	102	LCD1DO2-
103	PWREN_MAIN	104	GND
105	NC	106	PWMOUT1
107	GPIO14	108	PWMOUT2
109	GPIO10	110	PWMOUT3
111	GPIO8	112	PWMOUT0
113	RSMRST-	114	GPIO9
115	PWRBTN-	116	GPIO7
117	GND	118	GND
119	UART0TXD	120	UARTB_485
121	UART0RXD	122	UARTA_485
123	GND	124	GND
125	NC	126	UARTC_485
127	SD0CD	128	UARTD_485
129	SD0PWRSW	130	GND
131	SD0DATA2	132	I2C1SDA
133	GND	134	I2C1SCL
135	SD0CLK	136	GPIO13
137	SD0DATA3	138	GPIO12
139	SD0DATA1	140	I2C2SDA
141	SD0DATA0	142	I2C2SCL
143	SD0CMD	144	GND
145	SD0WP	146	C24MOUT
147	GND	148	VCLK
149	nHDMIDDCSDA	150	VVSYNC
151	GND	152	VHSYNC
153	nHDMIDDCSCL	154	VDIN7
155	nHDMIHPD	156	VDIN5

Pin	Signal	Pin	Signal
157	nHDMICEC	158	VDIN6
159	GND	160	VDIN4
161	UARTD_RX	162	VDIN0
163	UARTD_TX	164	VDIN2
165	UARTD_CTS	166	VDIN3
167	UARTD_RTS	168	VDIN1
169	UARTC_CTS	170	GND
171	UARTC_RTS	172	nHDMID2+
173	UARTC_RX	174	nHDMID2-
175	UARTC_TX	176	GND
177	UARTB_CTS	178	nHDMID1+
179	UARTB_RTS	180	nHDMID1-
181	UARTB_RX	182	GND
183	UARTB_TX	184	nHDMID0+
185	UARTA_CTS	186	nHDMID0-
187	UARTA_RTS	188	GND
189	UARTA_RX	190	nHDMICLK-
191	UARTA_TX	192	nHDMICLK+
193	GND	194	GND
195	GND	196	GND
197	GND	198	GND
199	5VIN	200	5VIN
201	5VIN	202	5VIN
203	5VIN	204	5VIN

Table 5: SOM DDR3 SODIMM slot pinouts

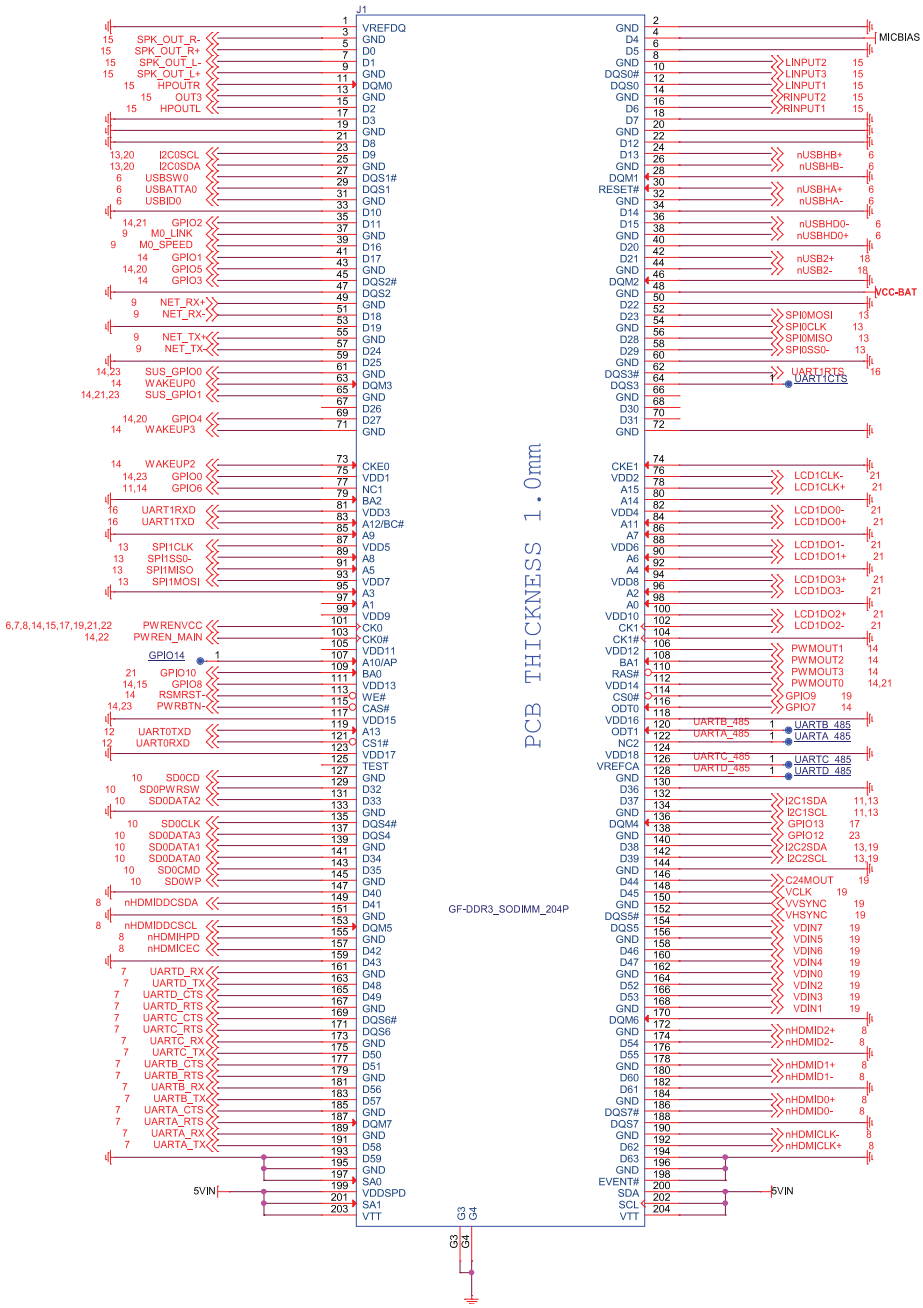


Figure 22: SOM DDR3 SODIMM slot schematics

4. Layout and Routing Recommendation

The information presented in this chapter includes the signal definition, topology, layout and routing guidelines for each bus interface, and reference schematics example. The information provided is intended for designing carrier boards that are compliant with the VIA SOM-6X80 module.

4.1 HDMI Interface

The VIA SOM-6X80 module features one HDMI interface. The HDMI interface uses four control signals, one differential clock, and three differential data pair signals that carry video and audio signals.

4.1.1 HDMI Signal Definition

The following table provides the definition of the HDMI signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
nHDMID0+	184	O	HDMI differential pair lines lane 0
nHDMID0-	186		
nHDMID1+	178	O	HDMI differential pair lines lane 1
nHDMID1-	180		
nHDMID2+	172	O	HDMI differential pair lines lane 2
nHDMID2-	174		
nHDMICLK+	192	O	HDMI differential pair clock lines
nHDMICLK-	190		
nHDMIDDCSCL	153	IO	HDMI DDC SCL
nHDMIDDCSDA	149	IO	HDMI DDC SDA
nHDMICEC	157	O	HDMI consumer electronics connector
nHDMIHPD	155	O	HDMI hot plug detect

Table 6: HDMI signal definition

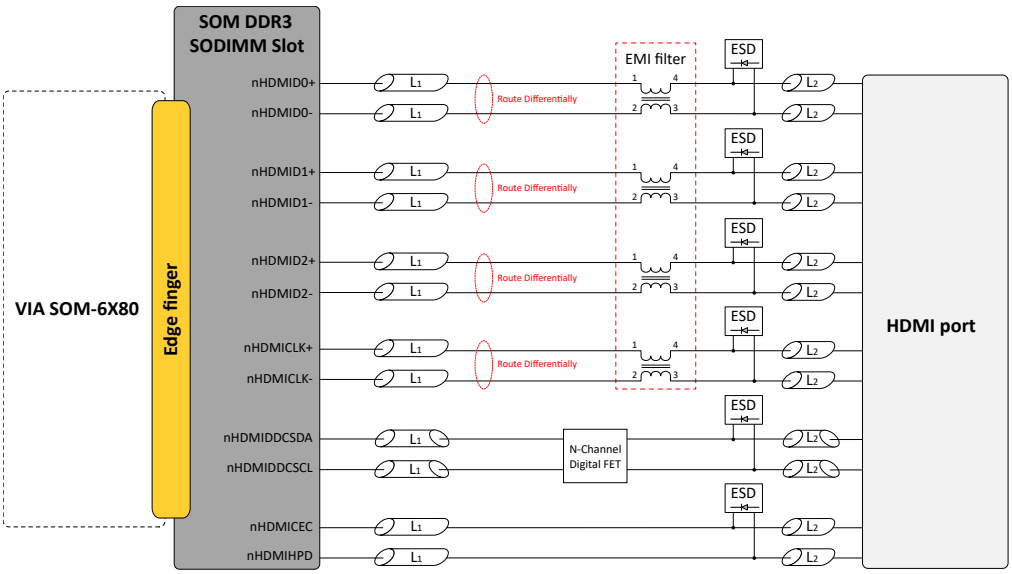


Figure 23: HDMI routing topology

Note:
The EMI filters and ESD components must be placed near the HDMI port.

4.1.2 HDMI Layout and Routing Recommendations

- Trace lengths should be kept to a minimum.
- Each trace of differential pairs should not have more than two via holes.
- Each differential pairs signal should route to parallel to each other with the same trace length.
- Differential pair should be all referenced to ground.
- Route the differential pairs on a single layer adjacent to a ground plane.
- The spacing between the differential pair signal and other signals should be at least three times the trace width.

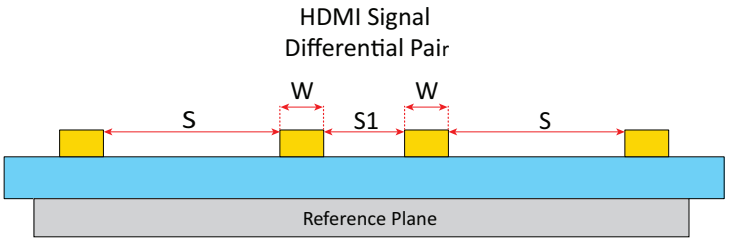


Figure 24: HDMI differential trace width and spacing example

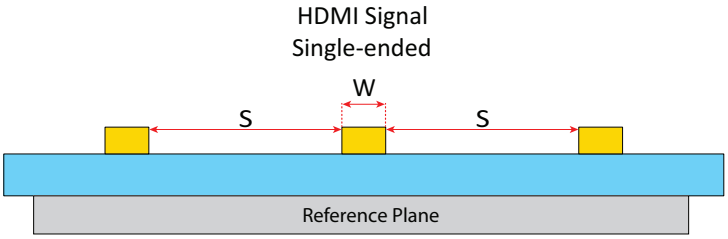


Figure 25: HDMI single-ended trace width and spacing example

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	nHDMID0+	100Ω ± 15% (Differential)	15 : 5 : 7 : 5 : 15	<5mil (Differential)	15mil
	nHDMID0-				
	nHDMID1+				
	nHDMID1-				
	nHDMID2+				
	nHDMID2-				
Clock	nHDMICLK+	100Ω ± 15% (Differential)	15 : 5 : 7 : 5 : 15	<5mil (Differential)	15mil
	nHDMICLK-				
Control	nHDMIDDCSCL	50Ω ± 15%	5 : 10 (W:S)	6mil	10mil
	nHDMIDDCSDA				
	nHDMICEC				
	nHDMIHPD				

Table 7: HDMI trace properties

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length (L_1+ L_2 = L_T)	Length Difference (mil)	
				To Clock	In Group
Data	nHDMID0+	Top/Bottom	L_T < 3"	<500	<1000
	nHDMID0-				
	nHDMID1+				
	nHDMID1-				
	nHDMID2+				
	nHDMID2-				
Clock	nHDMICLK+	Top/Bottom	L_T < 3"	<500	<1000
	nHDMICLK-				
Control	nHDMIDDCSCL	Top/Bottom	L_T < 3"	<500	<1000
	nHDMIDDCSDA				
	nHDMICEC				
	nHDMIHPD				

Table 8: HDMI layout guidelines

Signal Group	Signal Name	Reference Plane	Routing Topology	Signal Type
Data	nHDMID0+	Ground	Point-to-Point	Differential Pairs
	nHDMID0-			
	nHDMID1+			
	nHDMID1-			
	nHDMID2+			
	nHDMID2-			
Clock	nHDMICLK+	Ground	Point-to-Point	Differential Pairs
	nHDMICLK-			
Control	nHDMIDDCSCL	Ground	Point-to-Point	Single-ended
	nHDMIDDCSDA			
	nHDMICEC			
	nHDMIHPD			

Table 9: HDMI routing topology and signal type

4.1.3 HDMI Reference Schematics

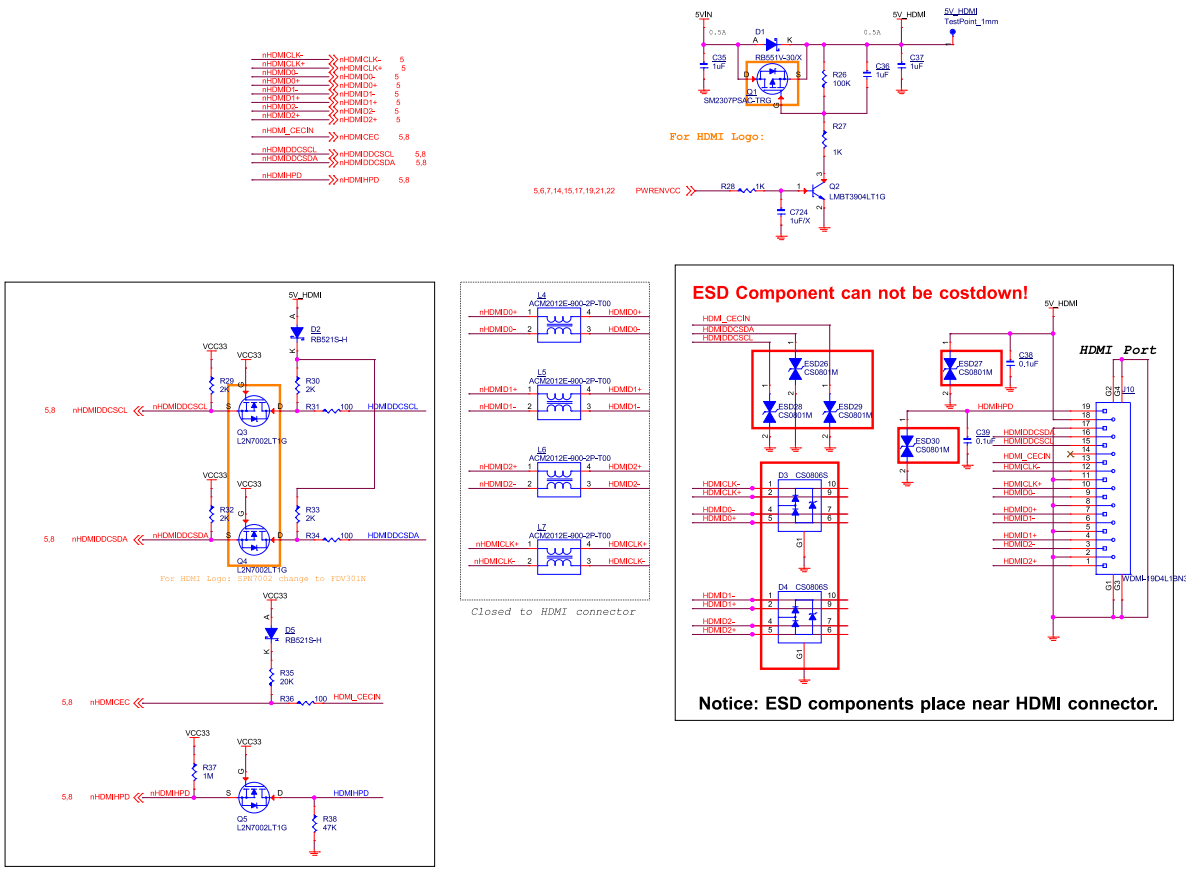


Figure 26: HDMI reference circuitry

4.2 Ethernet Interface

The VIA SOM-6X80 module features one Ethernet (10/100Mbps) interface. The Ethernet interface consists of two differential data signals and two control signals for activity link and speed indicators.

4.2.1 Ethernet Signal Definition

The following table provides the definition of the Ethernet signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
NET_TX+	55	O	Ethernet differential pair lines Transmit
NET_TX-	57		
NET_RX+	49	O	Ethernet differential pair lines Receive
NET_RX-	51		
M0_SPEED	39	O	Ethernet controller 0 100Mbps speed indicator
M0_LINK	37	O	Ethernet controller 0 100Mbps link indicator

Table 10: Ethernet signal definition

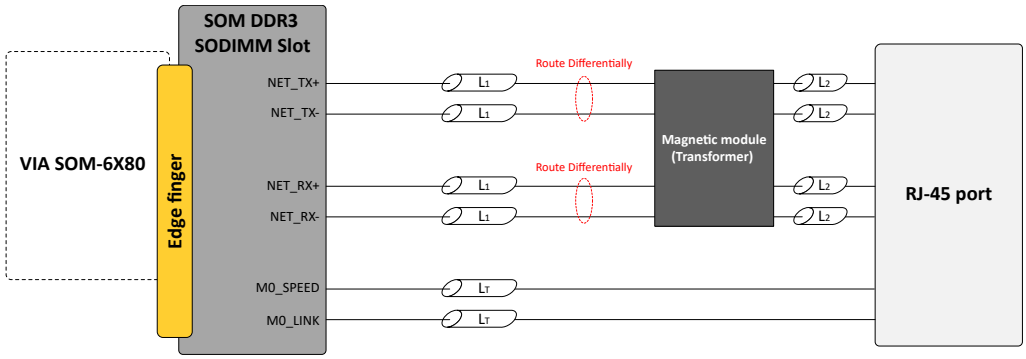


Figure 27: Ethernet routing topology

Note:
The magnetic module has to be placed as close as possible to the RJ-45 port. The distance must be less than 1".

4.2.2 Ethernet Layout and Routing Recommendations

- Route differential pairs close together and away from other signals.
- Route any other trace parallel to one of the differential trace.
- Keep trace length within each differential pair equal.
- Keep proper impedance between two traces within a differential pair.
- Each trace of differential pairs should not have more than two via holes.
- The spacing between the differential pair signal and other signals should be at least three times the trace width.
- Each differential pair of signals is required to be parallel to each other with the same trace length (Tolerance ±50mil) on the component (top) layer and to be parallel to a respective ground plane. The length difference between the shortest and longest pairs should be less than 200mil.
- The accumulated trace length of the differential signals pair between the SOM DDR3 SODIMM slot and magnetic module should be less than 1".
- The accumulated trace length of the differential signals pair between the magnetic module and RJ-45 connector should be less than 1". Isolate ground plane and connect to chassis.
- Keep each differential pair on the same plane.
- To prevent any noise from injecting into the differential pairs, be sure to keep digital signals or other signals away from the differential signals.
- The external magnetic module should be placed close to the RJ-45 connector to limit EMI emissions.

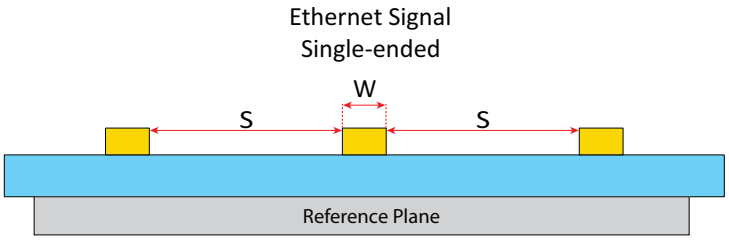


Figure 28: Ethernet single-ended trace width and spacing example

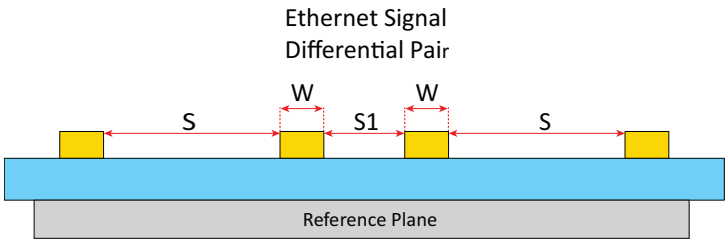


Figure 29: Ethernet differential trace width and spacing example

.

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	NET_TX+	100Ω ± 15% (Differential)	10 : 10 : 5 : 10 : 10	50mil	10mil
	NET_TX-				
	NET_RX+				
	NET_RX-				
Control	M0_SPEED	55Ω ± 15%	5:10	-	10mil
	M0_LINK				

Table 11: Ethernet trace properties

Signal Group	Signal Name	Routing Layer	Accumulated Trace Length (L_1+ L_2 = L_T)	Length Difference (mil)
				To Clock
Data	NET_TX+	Top/Bottom	L_T < 3"	<1500
	NET_TX-			
	NET_RX+			
	NET_RX-			
Control	M0_SPEED	Top/Bottom	L_T < 3"	<1500
	M0_LINK			

Table 12: Ethernet layout guidelines

Signal Group	Signal Name	Reference Plane	Signal Type	Routing Topology
Data	NET_TX+	Ground/Power	Differential Pairs	Point-to-Point
	NET_TX-			
	NET_RX+			
	NET_RX-			
Control	M0_SPEED	Ground/Power	Single-ended	Point-to-Point
	M0_LINK			

Table 13: Ethernet reference plane, signal type and routing topology

4.2.3 Ethernet Reference Schematics

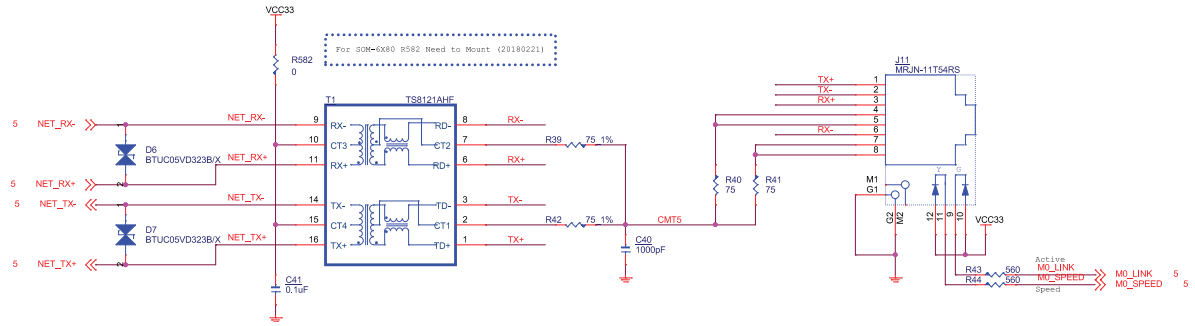


Figure 30: Ethernet reference circuitry

4.3 USB Interface

The VIA SOM-6X80 module features three USB 2.0 interfaces. Two of the three USB interfaces can only be used as a host. The other interface can be configured to be used as either the host or client. The USB interface signals use three bi-directional differential data pairs.

4.3.1 USB Signal Definition

The following table provides the definition of the USB signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
nUSBHD0+	38	IO	OTG Universal Serial Bus port 0, data+
nUSBHD0-	36		OTG Universal Serial Bus port 0, data-
nUSBHA+	30	IO	Universal Serial Bus port 1, data+
nUSBHA-	32		Universal Serial Bus port 1, data-
nUSBHB+	24	IO	Universal Serial Bus port 2, data+
nUSBHB-	26		Universal Serial Bus port 2, data-
USBATTA0	29	I	Universal Serial Bus device attach detect
USBID0	31	I	Port ID pin
USBSW0	27	I	Universal Serial Bus power control pin

Table 14: USB signal definition

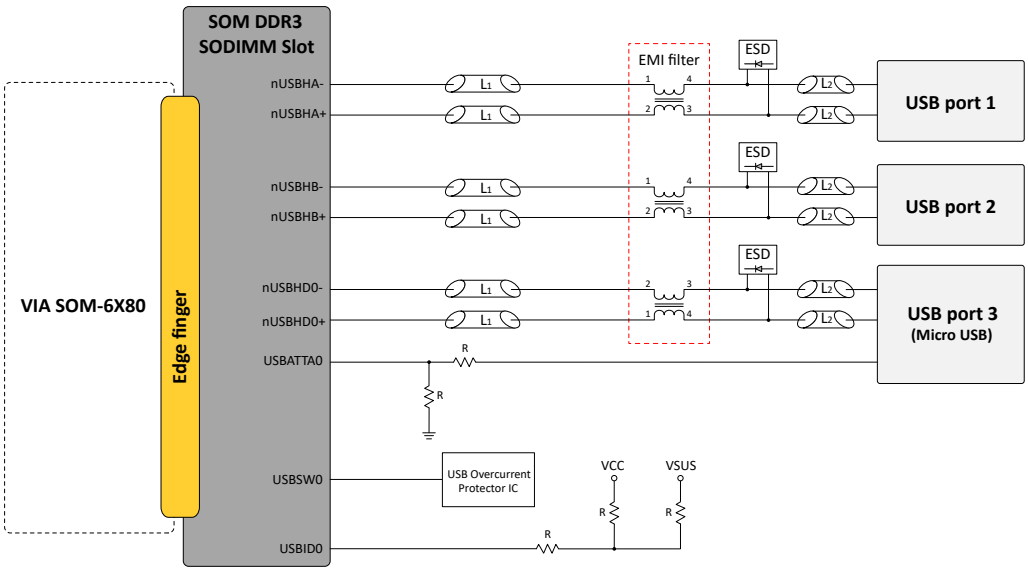


Figure 31: USB routing topology

4.3.2 USB Layout and Routing Recommendations

- The differential pair signals should be all referenced to ground.
- Each trace of differential pairs should not have more than two via holes.
- Differential pair route in parallel and in equal length.
- The amount of vias and corners used for the USB signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Each pair of USB data lines is required to be parallel to each other with the same trace length, and not parallel with other signals to minimize crosstalk.
- Separate the signal traces into similar groups and route similar signal traces together. In addition, it is recommended to have differential pairs routed together on the carrier board.
- Control trace signals impedance should maintain 55Ω ± 10%.
- For the USB traces, do not route them under oscillators, crystals, clock synthesizers, magnetic devices or IC's which could be using duplicate clocks.

The routing example for two pairs of USB data buses is shown in Figure 32.

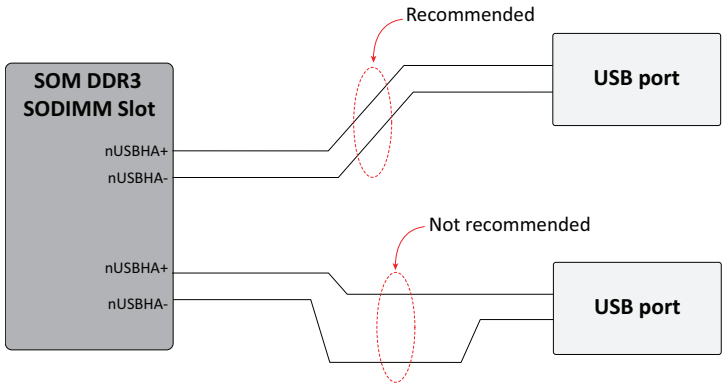


Figure 32: USB differential signal routing example

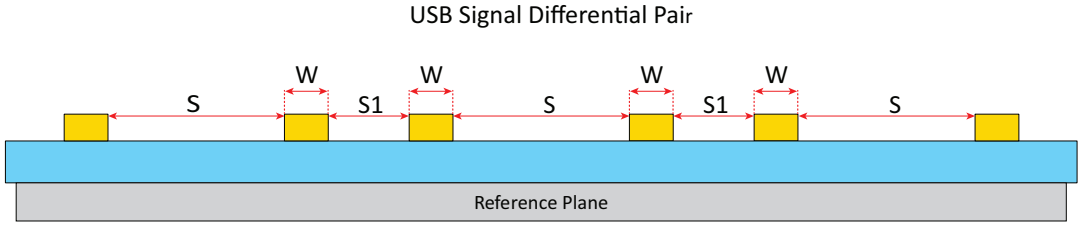


Figure 33: USB differential trace width and spacing example

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	nUSBHA+	90Ω ± 15%	20 : 7: 7.5 : 7 : 20	100mil	20mil
	nUSBHA-				
	nUSBHB+				
	nUSBHB-				
	nUSBHD0+				
	nUSBHD0-				
Control	USBATTA0	55Ω ± 10%	5 : 10	-	10mil
	USBID0				
	USBSW0				

Table 15: USB trace properties

Signal Group		Signal Name	Termination Option	Signal Type	Topology
Data	Port 1	nUSBHA+	90Ω	Differential Data Pairs	Point-to-Point
		nUSBHA-			
	Port 2	nUSBHB+			
		nUSBHB-			
	Port 3	nUSBHD0+			
		nUSBHD0-			
Control		USBATTA0	60Ω	-	Point-to-Point
		USBID0			
		USBSW0			

Table 16: USB termination option, signal type and routing topology

Signal Group		Signal Name	Routing Layer	Length Difference (In Pair)	Accumulated Trace Length ($L_1 + L_2 = L_T$)
Data	Port 1	nUSBHA+	Top/Bottom	<100mil	L_T < 12"
		nUSBHA-			
	Port 2	nUSBHB+			
		nUSBHB-			
	Port 3	nUSBHD0+			
		nUSBHD0-			
Control		USBATTA0	Top/Bottom	-	L_T < 12"
		USBID0			
		USBSW0			

Table 17: USB layout guidelines

4.3.3 USB Reference Schematics

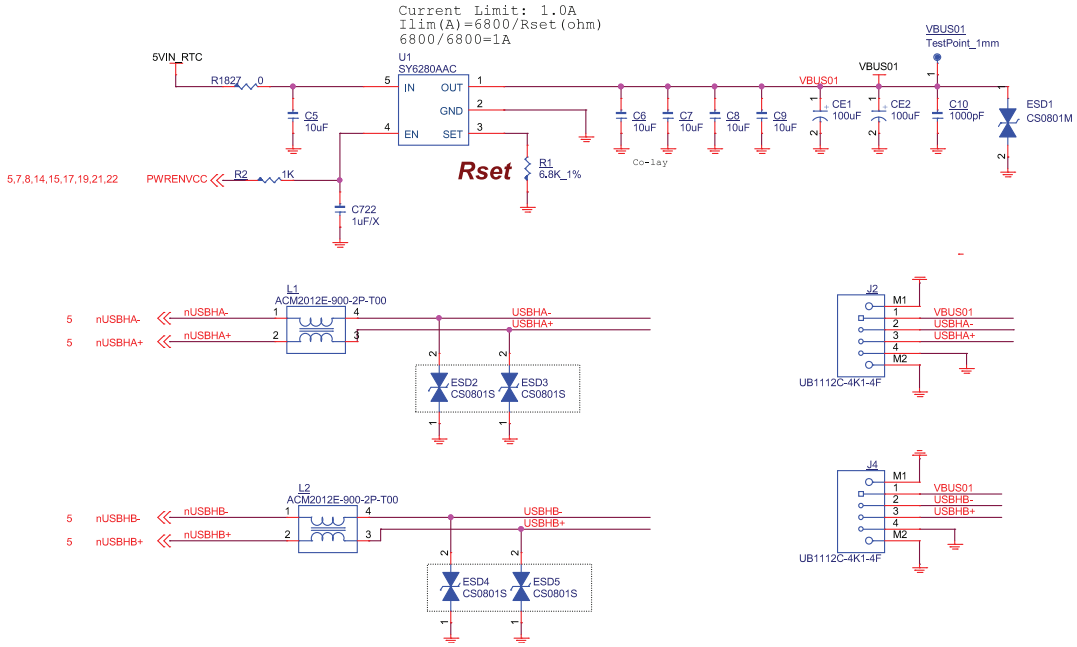
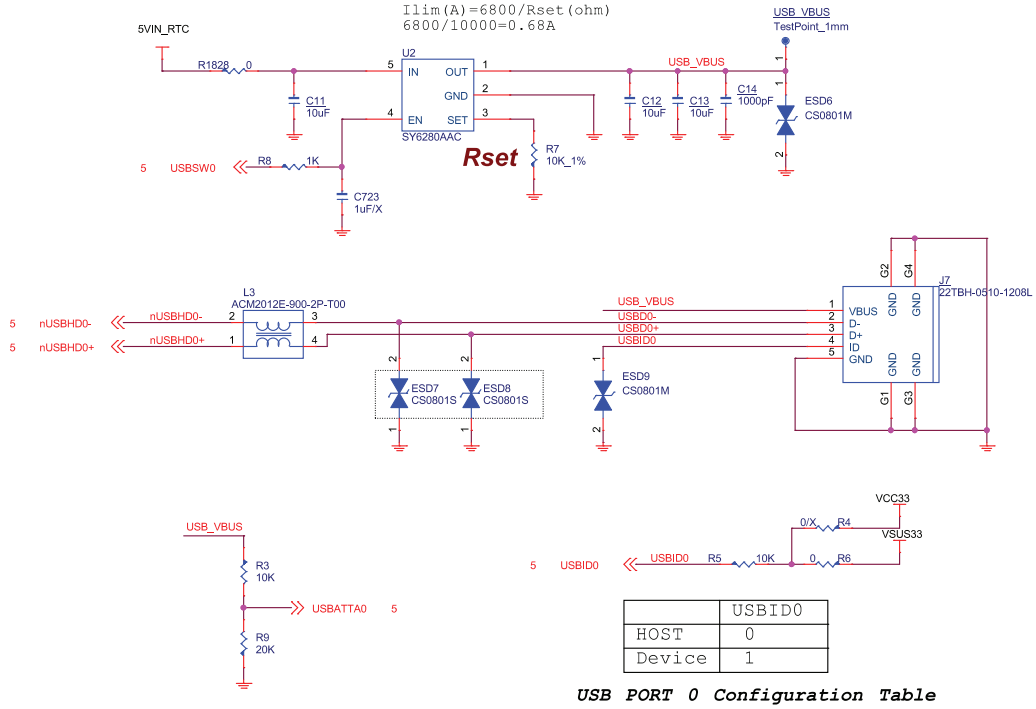


Figure 34: USB host reference circuitry

The USB port mode can be controlled by the signal USBID0. In the reference circuitry example below, the USBID0 signal is referenced to ground that makes the USB port mode as client USB (or USB OTG port).



	USBID0
HOST	0
Device	1

USB PORT 0 Configuration Table

Figure 35: USB client reference circuitry

4.4 COM and UART Interface

The VIA SOM-6X80 module features COM and UART interfaces that enable the interfacing of four COM or two UART on the carrier board. The four COM interfaces are used for RS-232 serial communications and the two UART can be used for TX/RX, RTS, CTS and debugging TX/RX.

4.4.1 COM and UART Signal Definition

The following table provides the definition of the COM and UART signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
UARTA_TX	191	O	UART Port-A transmit data
UARTA_RX	189	I	UART Port-A receive data
UARTA_RTS	187	O	UART Port-A request to send
UARTA_CTS	185	I	UART Port-A clear to send
UARTB_TX	183	O	UART Port-B transmit data
UARTB_RX	181	I	UART Port-B receive data
UARTB_RTS	179	O	UART Port-B request to send
UARTB_CTS	177	I	UART Port-B clear to send
UARTC_TX	175	O	UART Port-C transmit data
UARTC_RX	173	I	UART Port-C receive data
UARTC_RTS	171	O	UART Port-C request to send
UARTC_CTS	169	I	UART Port-C clear to send
UARTD_TX	163	O	UART Port-D transmit data
UARTD_RX	161	I	UART Port-D receive data
UARTD_RTS	167	O	UART Port-D request to send
UARTD_CTS	165	I	UART Port-D clear to send
UART1TXD	83	O	UART Port-1 transmit data
UART1RXD	81	I	UART Port-1 receive data
UART0TXD	119	O	UART Port-0 transmit data
UART0RXD	121	I	UART Port-0 receive data

Table 18: COM and UART signal definition

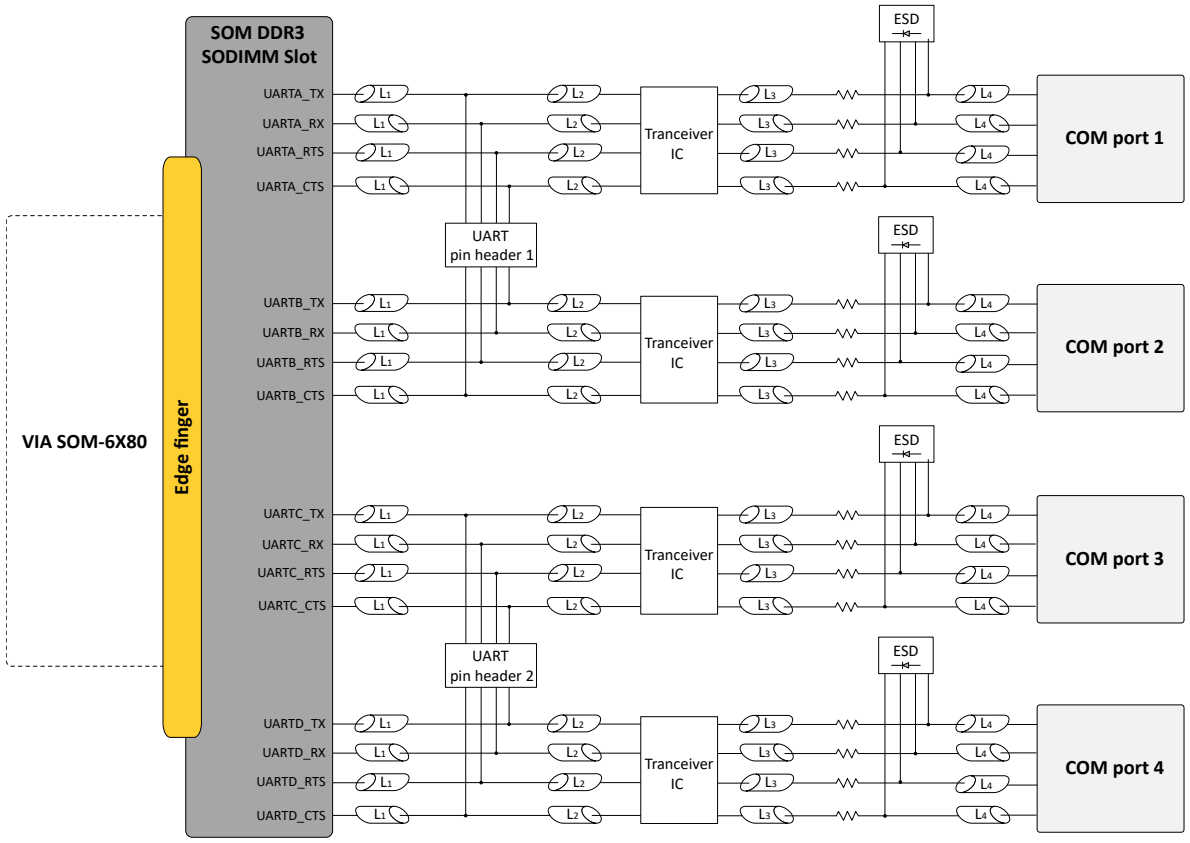


Figure 36: COM and UART routing topology

4.4.2 COM and UART Layout and Routing Recommendations

- The transmit and receive data trace signals should be routed in parallel and in equal length.
- The amount of vias and corners used for the COM and UART signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Control trace signals impedance should maintain 55Ω ± 10%.

Signal Group	Signal Name	Trace (mil) (Width : Spacing)	Trace Impedance	Spacing in Other Group
Data	UART[D:A]_TX	5 : 5	55Ω ± 10%	5mil
	UART[D:A]_RX			
	UART[1:0]TXD			
	UART[1:0]RXD			
Control	UART[D:A]_CTS	5 : 5	55Ω ± 10%	5mil
	UART[D:A]_RTS			

Table 19: COM and UART trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length ($L_1 + L_2 + L_3 + L_4 = L_T$)
Data	UART[D:A]_TX	Single-ended	Point-to-Point	Ground/Power	<10"
	UART[D:A]_RX				
	UART[1:0]TXD				
	UART[1:0]RXD				
Control	UART[D:A]_CTS	Single-ended	Point-to-Point	Ground/Power	<10"
	UART[D:A]_RTS				

Table 20: COM and UART topology, signal type and layout guidelines

4.4.3 COM and UART Reference Schematics

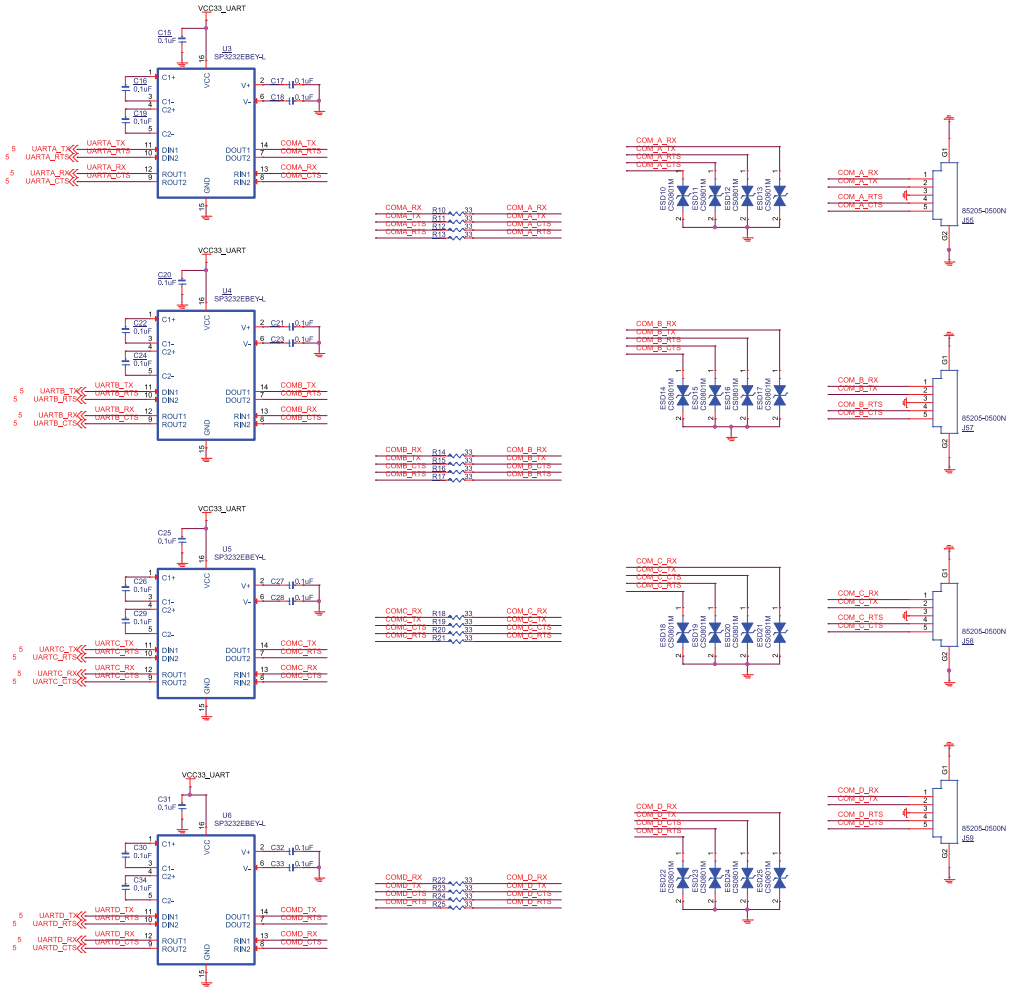


Figure 37: COM and UART reference circuitry

4.5 LCD Interface

The VIA SOM-6X80 module features one LCD interface. The LCD interface is a parallel bus signal provided for interfacing the LCD connector for LVDS LCD display as the main display interface. The LCD interface is a single-channel that supports 18-bit and 24-bit interfaces.

4.5.1 LCD Signal Definition

The following table provides the definition of the LCD signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
LCD1DO0-	82	O	LCD differential pair data 0 signals
LCD1DO0+	84		
LCD1DO1-	88	O	LCD differential pair data 1 signals
LCD1DO1+	90		
LCD1DO2-	102	O	LCD differential pair data 2 signals
LCD1DO2+	100		
LCD1DO3-	96	O	LCD differential pair data 3 signals
LCD1DO3+	94		
LCD1CLK-	76	O	LCD differential pair clock lines
LCD1CLK+	78		

Table 21: LCD signal definition

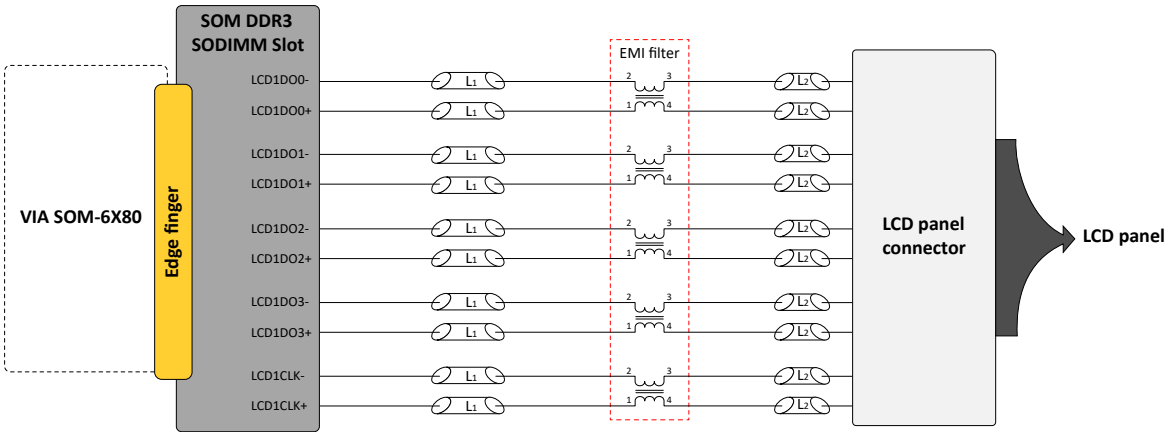


Figure 38: LCD routing topology

4.5.2 LCD Layout and Routing Recommendations

- LCD data signal traces should be designed to be as short as possible.
- In order to maximize the noise rejection characteristics of the LCD video outputs, it is then recommended to route the LCD video outputs on the top layer over a solid ground plane.
- The routing for the LCD signals should be as similar as possible (i.e., same routing layer, same number of vias, same routing length and same bends).
- Route the LCD data trace signals as a differential signal with a trace impedance of 100Ω .

Signal Group	Signal Name	Trace Impedance	Trace & Spacing (mil) (S : W : S1 : W : S)	Pair to Pair Trace Mismatch	Spacing to Other Signal
Data	LCD1DO0-	100Ω ± 15% (Differential)	15 : 5 : 7 : 5 : 15	<5mil (Differential)	15mil
	LCD1DO0+				
	LCD1DO1-				
	LCD1DO1+				
	LCD1DO2-				
	LCD1DO2+				
	LCD1DO3-				
	LCD1DO3+				
Clock	LCD1CLK-	100Ω ± 15% (Differential)	15 : 5 : 7 : 5 : 15	<5mil (Differential)	15mil
	LCD1CLK+				

Table 22: LCD trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane
Data	LCD1DO0-	Differential pairs	Point-to-Point	Ground
	LCD1DO0+			
	LCD1DO1-			
	LCD1DO1+			
	LCD1DO2-			
	LCD1DO2+			
	LCD1DO3-			
	LCD1DO3+			
Clock	LCD1CLK-	Differential pairs	Point-to-Point	Ground
	LCD1CLK+			

Table 23: LCD signal type, topology and reference plane

Signal Group	Signal Name	Routing Layer	Length Difference (mil)		Accumulated Trace Length (LT)
			To Clock	In Group	
Data	LCD1DO0-	Top/Bottom	<500	<1000	Route to Minimum (or <6")
	LCD1DO0+				
	LCD1DO1-				
	LCD1DO1+				
	LCD1DO2-				
	LCD1DO2+				
	LCD1DO3-				
	LCD1DO3+				
Clock	LCD1CLK-	Top/Bottom	-	-	-
	LCD1CLK+				

Table 24: LCD layout guidelines

4.5.3 LCD Reference Schematics

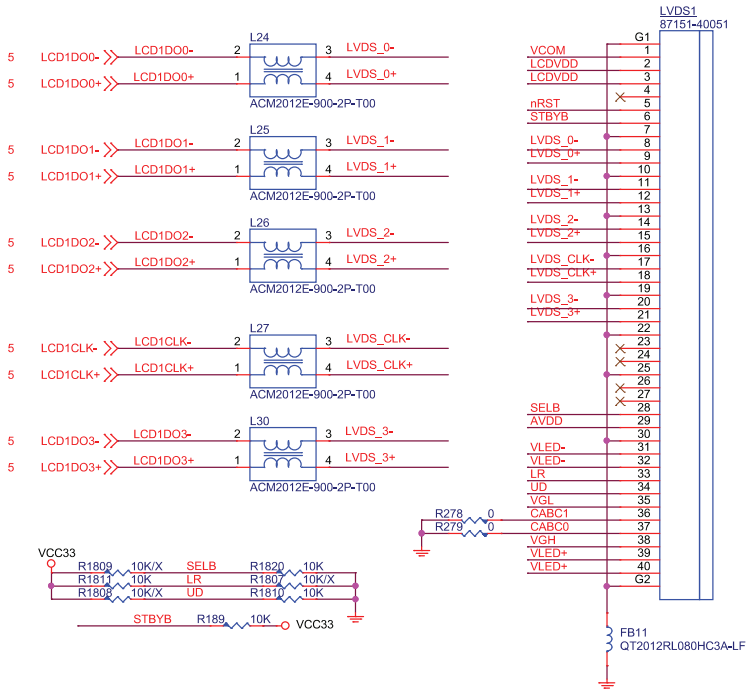


Figure 39: LCD reference circuitry

4.6 Touch Panel Interface

The VIA SOM-6X80 module features a touch panel interface for capacitive touch screens. It allows the integration of the touch screen solution on the carrier board. The touch panel interface is an interface connection between the SOM DDR3 SODIMM slot and touch panel connector. The touch panel interface supports 4-wire and 5-wire capacitive touch screens.

4.6.1 Touch Panel Signal Definition

The following table provides the definition of the touch panel signals.

From SOM DDR3 SODIMM Slot to Capacitive Touch Sensor Controller			
Signal Name	**Pin #**	**I/O**	**Description**
GPIO4	69	O	TP reset signal
GPIO5	43	O	TP interrupt signal
I2C0SDA	25	O	TP I²C Data
I2C0SCL	23	O	TP I²C Clock

Table 25: Touch panel signal definition

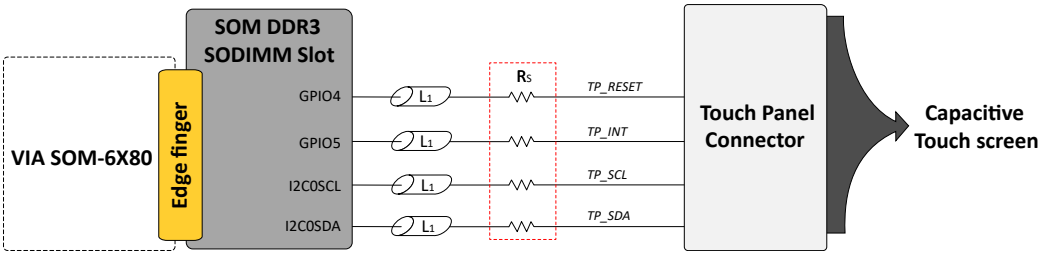


Figure 40: Touch panel routing topology

4.6.2 Touch Panel Layout and Routing Recommendations

- Keep trace lengths as short as possible.
- It is recommended to route the traces on the top layer.
- The amount of vias and corners used for the touch panel signal layout should be minimized.

Interface	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Trace Mismatch	Spacing to Other Signal
SOM DDR3 SODIMM slot to Touch panel connector	GPIO4	55Ω ± 10%	5 : 5	20mil	5mil
	GPIO5				
	I2C0SCL				
	I2C0SDA				

Table 26: Touch panel trace properties

Interface	Signal Name	Signal Type	Topology	Reference Plane
SOM DDR3 SODIMM slot to Touch panel connector	GPIO4	Single-ended	Point-to-Point	Ground/Power
	GPIO5			
	I2C0SCL			
	I2C0SDA			

Table 27: Touch panel signal type, routing topology and reference plane

Interface	Signal Name	Routing Layer	Length Difference (mil)	Accumulated Trace Length ($L_1 + L_2 = L_T$)
SOM DDR3 SODIMM slot to Touch panel connector	GPIO4	Top/Bottom	-	2"
	GPIO5			
	I2C0SCL			
	I2C0SDA			

Table 28: Touch panel layout guidelines

4.6.3 Touch Panel Reference Schematics

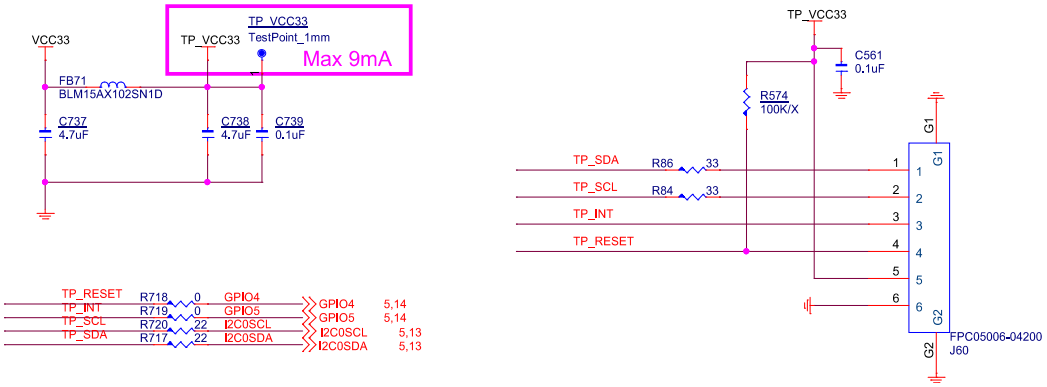


Figure 41: Touch panel reference circuitry

4.7 GPIO Interface

The VIA SOM-6X80 module features a General Purpose Input and Output (GPIO) interface.

4.7.1 GPIO Signal Definition

The following table provides the definition of the GPIO signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
GPIO0	75	IO	General Purpose GPIO
GPIO1	41	IO	
GPIO2	35	IO	
GPIO3	45	IO	
GPIO4	69	IO	
GPIO5	43	IO	
GPIO6	77	IO	
GPIO7	116	IO	
GPIO8	111	IO	
SUS_GPIO0	61	IO	General Purpose GPIO for Suspend Power Domain
SUS_GPIO1	65	IO	

Table 29: GPIO signal definition

4.7.2 GPIO Layout and Routing Recommendation

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	GPIO[7:0]	55Ω	5 : 5	5mil
	GPIO8			
	SUS_GPIO0	55Ω	5 : 5	5mil
	SUS_GPIO1			

Table 30: GPIO trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
Data	GPIO[7:0]	Single-ended	Point-to-Point	Ground/Power	12"
	GPIO8				
	SUS_GPIO0	Single-ended	Point-to-Point	Ground/Power	12"
	SUS_GPIO1				

Table 31: GPIO signal type, topology and layout guidelines

4.8 I²C Interface

The VIA SOM-6X80 module features an I²C interface that can support up to three I²C devices.

4.8.1 I²C Signal Definition

The following table provides the definition of the I²C signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
I2C0SDA	25	IO	I²C0 serial data
I2C0SCL	23	IO	I²C0 serial clock
I2C1SDA	132	IO	I²C1 serial data
I2C1SCL	134	IO	I²C1 serial clock
I2C2SDA	140	IO	I²C2 serial data
I2C2SCL	142	IO	I²C2 serial clock

Table 32: I²C signal definition

4.8.2 I²C Layout and Routing Recommendation

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	I2C[2:0]SDA	55Ω	5 : 5	5mil
Clock	I2C[2:0]SCL	55Ω	5 : 5	5mil

Table 33: I²C trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
Data	I2C[2:0]SDA	Single-ended	Daisy chain	Ground/Power	<12"
Clock	I2C[2:0]SCL	Single-ended	Daisy chain	Ground/Power	<12"

Table 34: I²C signal type, topology and layout guidelines

4.9 SPI Interface

The VIA SOM-6X80 module features two SPI interfaces. Each SPI interface can support one master and one slave.

4.9.1 SPI Signal Definition

The following table provides the definition of the SPI signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
SPI0MISO	56	I	Master Input 0, Slave Output 0
SPI0MOSI	52	O	Master Output 0, Slave Input 0
SPI0CLK	54	O	Serial Clock 0
SPI0SS0-	58	O	Slave Select 0
SPI1MOSI	93	O	Master Output 1, Slave Input 1
SPI1MISO	91	I	Master Input 1, Slave Output 1
SPI1CLK	87	O	Serial Clock 1
SPI1SS0-	89	O	Slave Select 1

Table 35: SPI signal definition

4.9.2 SPI Layout and Routing Recommendation

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	SPI[1:0]MISO	55Ω	5 : 5	5mil
	SPI[1:0]MOSI			
	SPI[1:0]SS0-			
Clock	SPI[1:0]CLK	55Ω	5 : 10	5mil

Table 36: SPI trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
Data	SPI[1:0]MISO	Single-ended	Daisy chain	Ground/Power	<10"
	SPI[1:0]MOSI				
	SPI[1:0]SS0-				
Clock	SPI[1:0]CLK	Single-ended	Rs = 22Ω	Ground/Power	<10"

Table 37: SPI signal type, topology and layout guidelines

4.10 Audio Interface

The VIA SOM-6X80 module features an audio interface for audio connectors such as two line-in, headphone, mono speaker out, right and left channel speaker out, and microphone.

4.10.1 Audio Signal Definition

The following table provides the definition of the audio signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
HPOUTR	11	O	Headphone right channel output
HPOUTL	15	O	Headphone left channel output
OUT3	13	O	Audio mono output
LINPUT1	12	I	Left channel single-ended Mic input/Left channel negative differential Mic input
LINPUT2	8	I	Left channel line input/Left channel positive differential Mic input
LINPUT3	10	I	Left channel line input/Left channel positive differential Mic input/Jack detect input pin
RINPUT1	16	I	Right channel single-ended Mic input/Right channel negative differential Mic input
RINPUT2	14	I	Right channel line input/Right channel positive differential Mic input
SPK_OUT_R+	5	O	Right speaker positive output
SPK_OUT_R-	3	O	Right speaker negative output
SPK_OUT_L+	9	O	Left speaker positive output
SPK_OUT_L-	7	O	Left speaker negative output

Table 38: Audio signal definition

4.10.2 Audio Layout and Routing Recommendations

- Route the analog and digital trace signals as far as possible from each other to prevent noise.
- Route the clock trace away from any analog input and voltage reference pins.
- Isolate the codec or put away from any major current path or ground bounce.
- Fill with copper the regions between the analog traces and attached it to the analog ground.
- Fill with copper the regions between the digital traces and attached it to the digital ground.
- Keep trace lengths as short as possible.

Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
HPOUTR	55Ω ± 10%	8 : 5	5mil
HPOUTL			
OUT3	55Ω ± 10%	8 : 5	5mil
LINPUT[3:1]	55Ω ± 10%	8 : 5	5mil
RINPUT[2:1]			
SPK_OUT_R[+/-]	55Ω ± 10%	8 : 5	5mil
SPK_OUT_L[+/-]			

Table 39: Audio trace properties

Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length
HPOUTR HPOUTL	Single-ended	Point-to-Point	Ground	<10"
OUT3	Single-ended	Point-to-Point	Ground	<10"
LINPUT[3:1] RINPUT[2:1]	Single-ended	Point-to-Point	Ground	<10"
SPK_OUT_R[+/-] SPK_OUT_L[+/-]	Single-ended	Point-to-Point	Ground	<10"

Table 40: Audio signal type, topology and layout guidelines

4.10.3 Audio Interface Reference Schematics

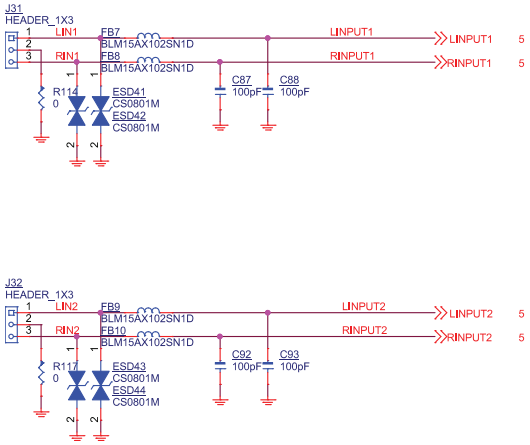


Figure 42: Line-in 1 & 2 reference circuitry

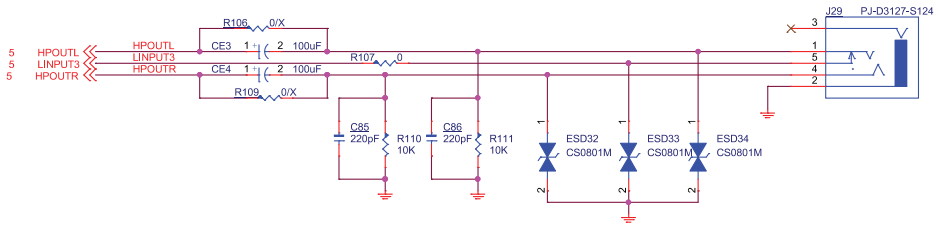


Figure 43: Headphone reference circuitry

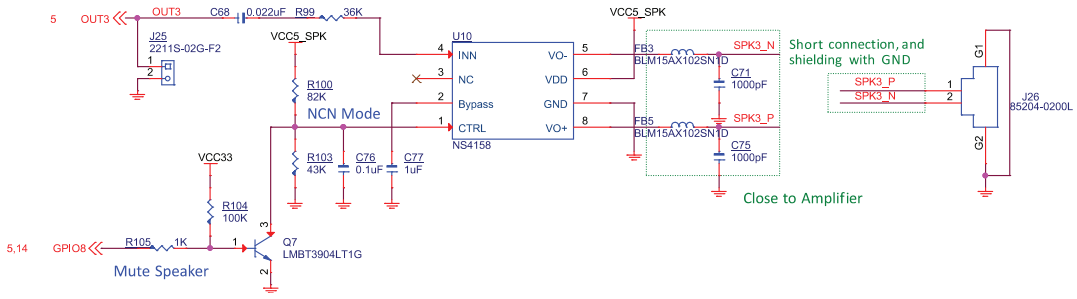


Figure 44: Mono speaker out reference circuitry

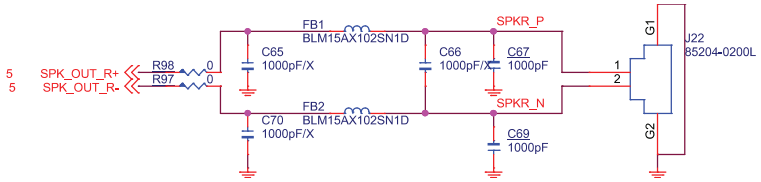


Figure 45: Right channel speaker out reference circuitry

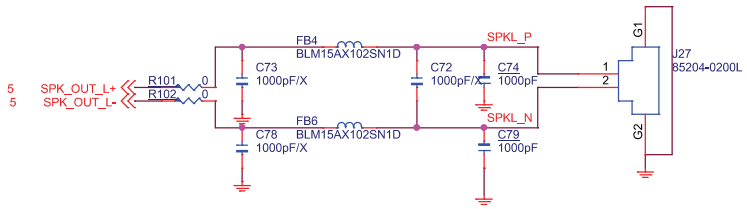


Figure 46: Left channel speaker out reference circuitry

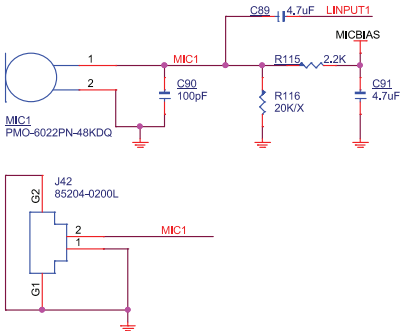


Figure 47: Onboard microphone reference circuitry

4.11 SD Interface

The VIA SOM-6X80 module features an SD interface for SD storage.

4.11.1 SD Signal Definition

The following table provides the definition of the SD signals that are implemented in the SOM DDR3 SODIMM slot.

Signal Name	Pin #	I/O	Description
SD0DATA0	141	IO	Data signal 0, used for SD interface
SD0DATA1	139	IO	Data signal 1, used for SD interface
SD0DATA2	131	IO	Data signal 2, used for SD interface
SD0DATA3	137	IO	Data signal 3, used for SD interface
SD0CMD	143	IO	Command signal, add external pull-up resistor
SD0CLK	135	O	SD0 bus clock
SD0CD	127	I	SD0 Command
SD0PWRSW	129	O	SD0 Power switch
SD0WP	145	I	SD0 write protect

Table 41: SD signal definition

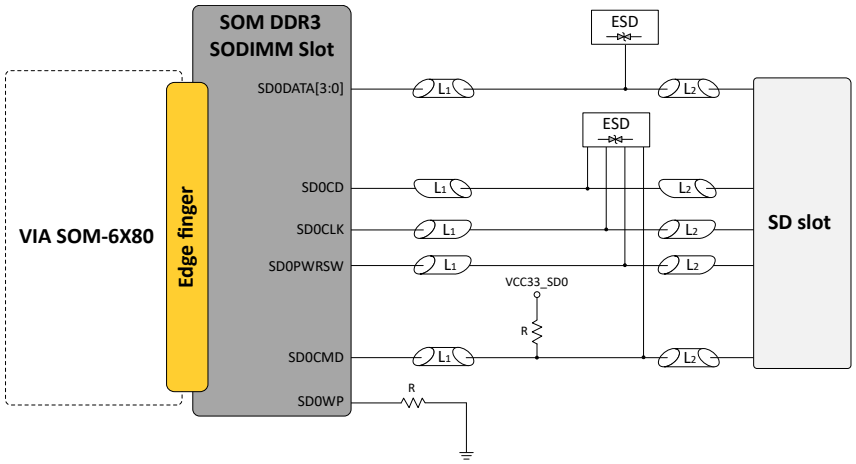


Figure 48: SD routing topology

4.11.2 SD Layout and Routing Recommendations

- Signal traces should be above a solid and continuous ground plane along the path from SOM DDR3 SODIMM slot to SD slot.
- SD0CMD trace signal must have pull-up resistor of 4.7KΩ.
- SD0WP trace signal must have pull-down resistor of 1KΩ to the ground.
- The ESD protection of trace signal SD0PWRSW must be placed near the SD slot.

Signal Group	Signal Name	Trace Impedance	Trace (mil) (Width : Spacing)	Spacing to Other Signal
Data	SD0DATA[3:0]	55Ω ± 15%	5 : 5	5mil
Control	SD0CMD	55Ω ± 15%	5 : 5	5mil
	SD0CD			
	SD0WP			
	SD0PWRSW			
Clock	SD0CLK	55Ω ± 15%	5 : 15	15mil

Table 42: SD trace properties

Signal Group	Signal Name	Signal Type	Topology	Reference Plane	Accumulated Trace Length ($L_1 + L_2 = L_T$)
Data	SD0DATA[3:0]	Single-ended	Point-to-Point	Ground/Power	<8"
Control	SD0CMD	Single-ended	Point-to-Point	Ground/Power	<8"
	SD0CD				
	SD0WP				
	SD0PWRSW				
Clock	SD0CLK	Single-ended	Point-to-Point	Ground/Power	<8"

Table 43: SD signal type, topology and layout guidelines

4.11.3 SD Interface Reference Schematics

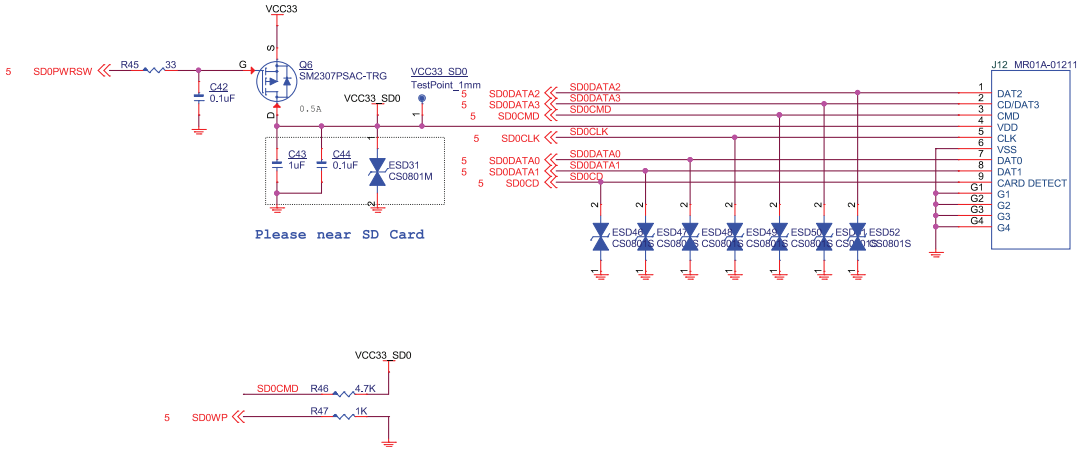


Figure 49: SD reference circuitry

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