DESIGN GUIDE

Carrier Board

for SOM-3000 Module

1.01-21032024

Revision History

Revision	Date	Description
1.01	21/03/2024	Replaced mentions of SOM-9X35 with SOM-3000 in multiple figures.
1.00	06/09/2023	Initial release

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1. Introduction

This document provides design guidelines and rule recommendations for the developers of a carrier board that supports the features of VIA SOM-3000 module. This document includes the layout and routing guidelines for general board designs and major underlying interfaces (ex. MIPI, LVDS, HDMI, USB). In addition, the document includes the placement and mechanical information on the M.2 slot which is used to provide high-speed interfaces between the carrier board and the VIA SOM-3000 module.

Please note that this document is considered to be a reference guide only. This document is not intended to be a specification. All information and examples listed below are considered to be accurate as of the publication date. However, developers must be aware that this document is only a reference guide.

1.1 Document Overview

A brief description of each chapter is given below.

Chapter 1: Introduction

This chapter briefly introduces the structure of the design guide document.

Chapter 2: General Carrier Board Recommendations

The general design schemes and recommended layout rules are shown in this chapter.

Chapter 3: VIA SOM-3000 Module and M.2 Slot Specification Overview

Detailed information about the VIA SOM-3000 module and M.2 slot placement and dimensions are described in this chapter.

Chapter 4: Layout and Routing Recommendations

Detailed layout and routing guidelines for each major interface are described in this chapter.

1.2 Acronyms Used

Term	Description
ADC	Analog to Digital Converter
AMIC	Analog Microphone Jack
ASIC	Application-specific Integrated Circuit
BAM	Bus Access Manager/Module
BLSP	BAM Low Speed Peripheral
BMS	Battery Management System
CMOS	Complementary Metal Oxide Semiconductor
CSI	Camera Serial Interface
CTP	Capacitance Touch Panel
DIO	Digital Input /Output
DMIC	Digital Microphone Jack
DSI	Display Serial Interface
EMI	Electromagnetic Interference
ESD	Electrostatic-discharge
GPIO	General Purpose Input/Output
HDMI	High-Definition Multimedia Interface
I/O	Input/Output
I2C	Inter-IC
IC	Integrated Circuit
LCD	Liquid-Crystal Display
LVDS	Low-Voltage Differential Signaling
M.2	Next Generation Form Factor
MIPI	Mobile Industry Processor Interface
MMC	Multi Media Card
NVMe	Non Volatile Memory Host Controller Interface Specification
P2P	Point-to-Point
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PMIC	Power Management Integrated Circuit
PWM	Pulse Width Modulation
RTC	Real Time Clock
SD	Secure Digital Memory Card
SDC	Secure Digital Controller
SIM	Subscriber Identity Module
SMPS	Switched-mode Power Supply
SOM	System-On-Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Table 01: Acronyms used

1.3 I/O Parameter Definitions

Symbol	Description
Pad attribute	
AI	Analog Input (does not include the pad circuitry)
AO	Analog Output (does not include the pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital Input (CMOS)
DO	Digital Output (CMOS)
H	High-Voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad pull details for digital I/O	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP:pdpukp = default no-pull with programmable options following the colon (:) PD:nppukp = default pull-low (pull-down) with programmable options following the colon (:) PU:nppdkp = default pull-high (pull-up) with programmable options following the colon (:) KP:nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-high device
PD	Contains an internal pull-low device

Table 02: I/O parameter definitions

1.4 Schematic Conventions

The reference schematics depicted in this document show the directional flows of the signals. Directional flow is indicated by the pointed ends of the arrow shapes.

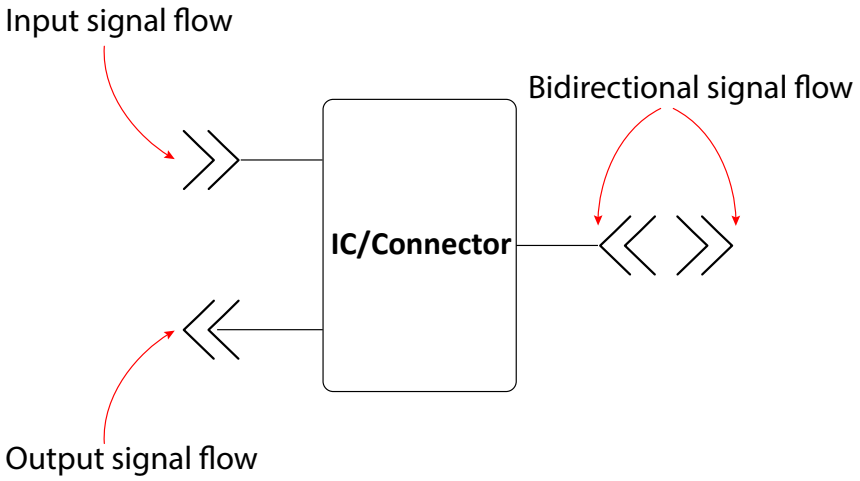


Figure 01: Schematic conventions

2. General Carrier Board Recommendations

This section contains general guidelines for the PCB stack-up and the layout of traces. The general guide lines for routing style, topology, and trace attribute recommendations are also discussed.

2.1 PCB Stack-Up

The PCB stack-up consists of signal layers and reference (power and ground) layers. The signal layers are referred to as the component layer (top), inner layer and solder layer (bottom).

The carrier board designers can choose between two basic categories of PCB stack-up design: micro strip and strip line. Microstrip designs have the outer signal layers exposed while stripline designs have the outermost signal layers shielded by reference layers.

The following figures show examples of microstrip and stripline designs.

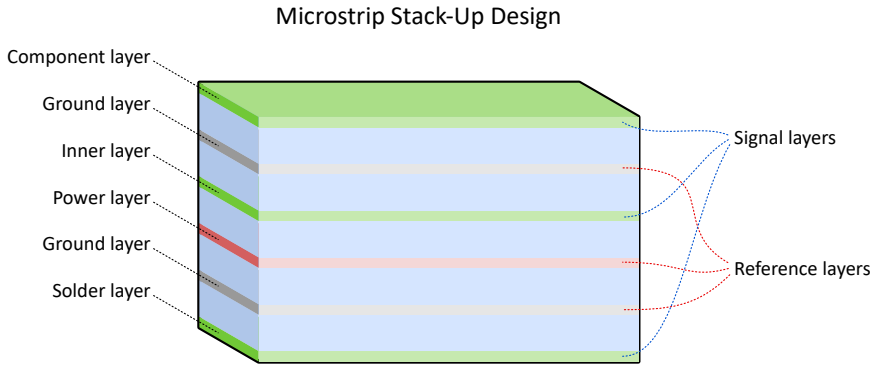


Figure 02: Microstrip PCB stack-up example

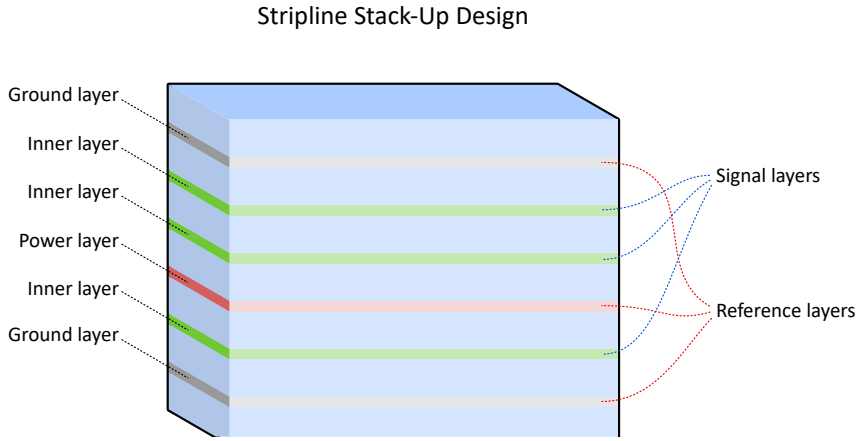


Figure 03: Stripline PCB stack-up example

The choice of microstrip or stripline design depends on the application for which the carrier board is being designed. If the carrier board is being designed for locations where sensitivity to EMI is an issue, a stripline design is recommended for reducing EMI and noise coupling. For applications where the tolerance for EMI levels is greater, a microstrip design is recommended to reduce costs. Due to the inherent nature of stripline PCB stacks, broad-side coupling is possible.

2.1.1 6-Layer PCB Stack-up Example

The following figure shows the recommended 6-layer PCB stack-up design for the carrier board of the VIA SOM-3000 module.

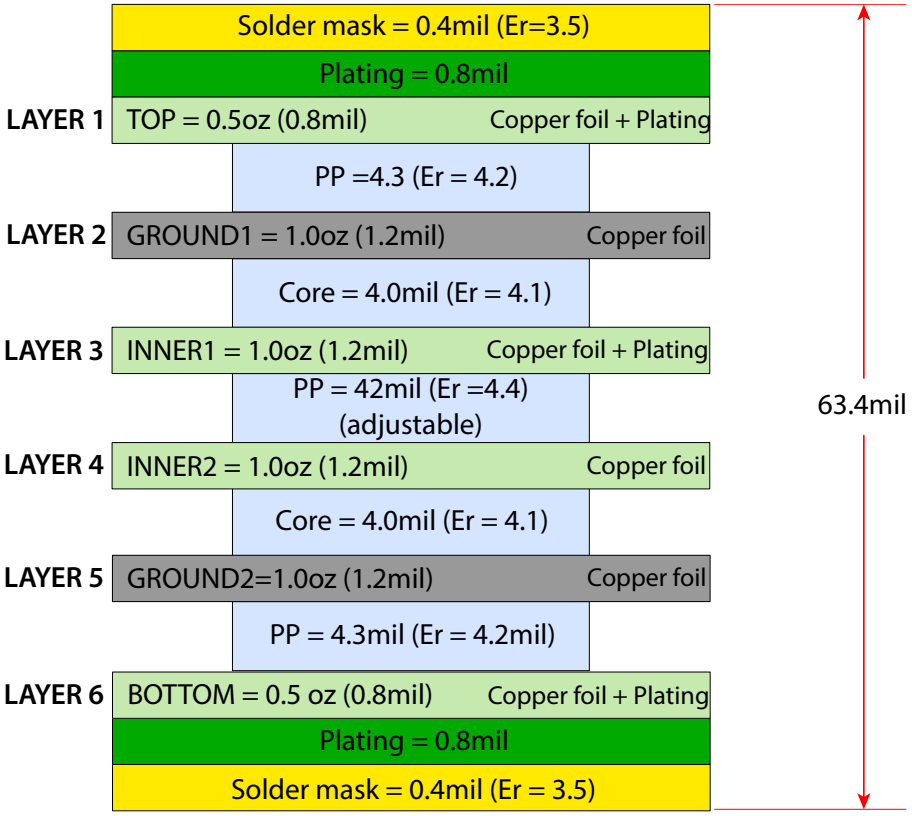


Figure 04: 6-Layer PCB board stack-up detail

2.1.2 Impedance Requirements

Function Type	Other Signal	USB	MIPI DSI	MIPI CSI	HDMI	LVDS	Ethernet
Trace Type	Single-ended	Differential	Differential	Differential	Differential	Differential	Differential
Required value	50Ω	90Ω	100Ω	100Ω	100Ω	100Ω	100Ω
Trace & Spacing (mil) (W:S:W) Micro strip	7	6.1 : 5.6 : 6.1	5.6: 8.3 : 5.6	5.6: 8.3 : 5.6	5.6: 8.3 : 5.6	5.6: 8.3 : 5.6	5.6: 8.3 : 5.6
Trace & Spacing (mil) (W:S:W) Strip line	5	4.4 : 6.4 : 4.4	3.9 : 9.1 : 3.9	3.9 : 9.1 : 3.9	3.9 : 9.1 : 3.9	3.9 : 9.1 : 3.9	3.9 : 9.1 : 3.9

Table 03: Impedance requirements

2.2 General Layout & Routing Guidelines

This section provides general layout rules and routing guidelines for designing carrier boards for the SOM-3000 module.

2.2.1 General Layout & Routing Guidelines

Topology is the physical connectivity of a net or a group of nets. There are two types of topologies for a carrier board layout: point-to-point (P2P) and multi-drop. An example of these topologies is shown in Figure 5.

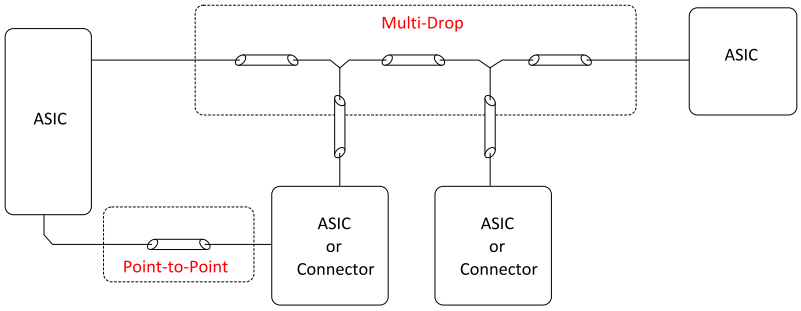


Figure 05: Point-to-point and multi-drop examples

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept as short as possible (less than 1.5”). Therefore, daisy chain style routing is strongly recommended for these signals. Figure 6 below shows an example of daisy chain routing.

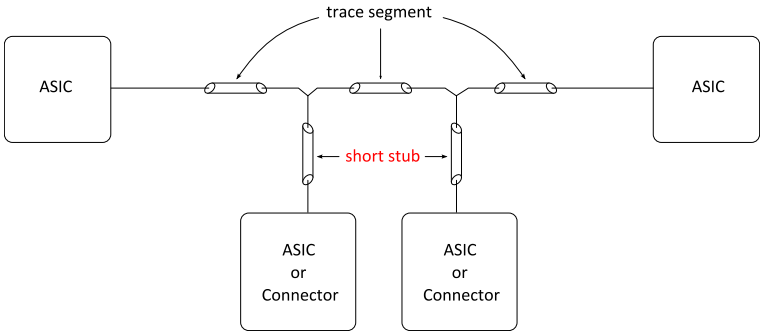


Figure 06: Daisy-chain example

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 7. In this case, the branch point is somewhere between both ends. It may be near the source or the loads, but being close to the load side is preferred. The separated traces should be equal in length.

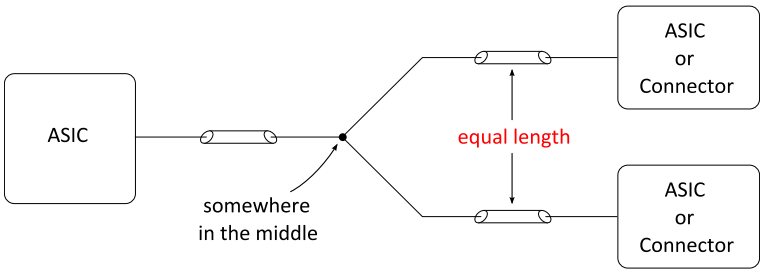


Figure 07: Alternate multi-drop example

2.2.2 General Trace Attribute Recommendation

A 5mil trace width and 15mil spacing are generally advised for most signal traces on a carrier board layout. To reduce trace inductance, the minimum power trace width is recommended to be 30mil.

As a quick reference, the overall recommended trace width and spacing for different trace types are listed in Table 4, and the recommended trace width and spacing for each signal group is shown in Chapter 4.

Trace Type	Trace Width (mil)	Spacing (mil)
Regular Signal	5 or wider	15 or wider
Interface or Bus Reference Voltage Signal	20 or wider	20 or wider
Power	30 or wider	20 or wider

Table 04: Recommended trace width and spacing

General rules for minimizing crosstalk in high-speed bus designs are listed below:

- Maximize the distance between traces. Maintain 15mil minimum spaces between traces wherever possible.
- Maximize the distance (30mil minimum) between two adjacent routing areas of different signal groups wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Select a board stack-up that minimizes coupling between adjacent traces.

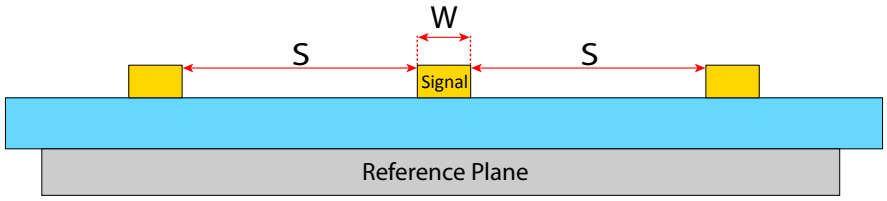


Figure 08: Single-ended trace width and spacing example

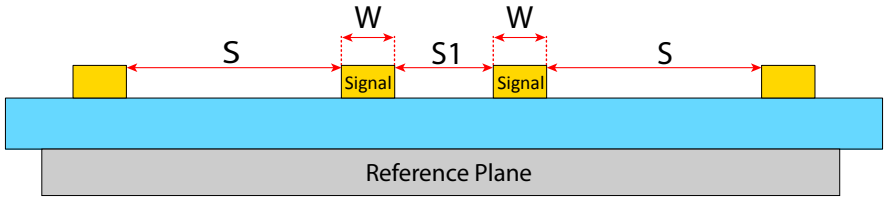


Figure 09: Differential trace width and spacing example

Note:
1. W: Trace width
2. S: The spacing to other traces
3. S1: Differential pair spacing

2.2.3 General Clock Routing Considerations

The clock routing guidelines are listed below:

- The recommended clock trace width is 5mil.
- The minimum space between one clock trace and adjacent clock traces is 20mil. The minimum space from one segment of a clock trace to other segments of the same clock trace is at least two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 10).
- The clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 11).
- The series terminations (damping resistors) are needed for all clock signals (typically 0Ω to 47Ω). When two loads are driven by one clock signal, the series termination layout is shown in Figure 12. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20mil to 50mil wide) is preferred.
- No clock traces on the internal layer if a 6-layer board is used.

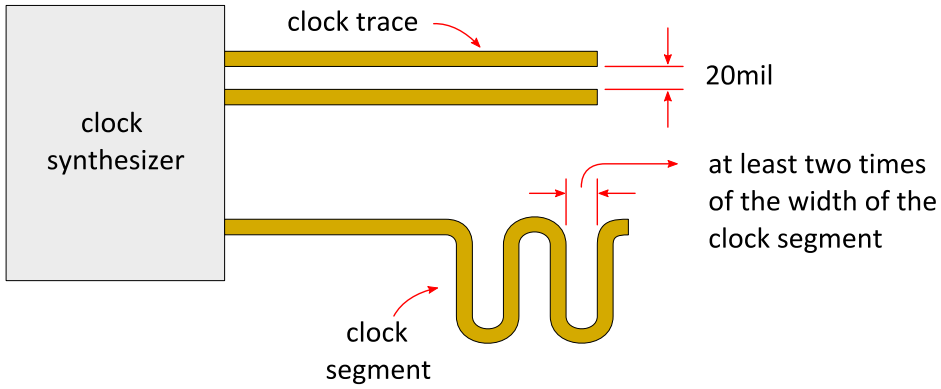


Figure 10: Suggested clock trace spacing

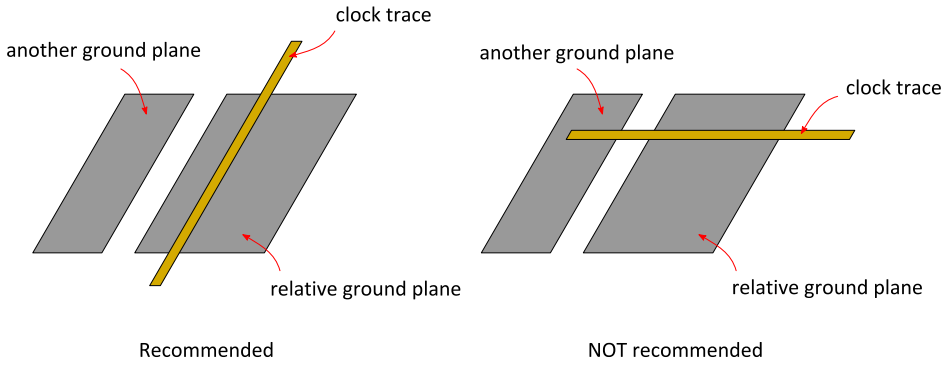


Figure 11: Clock trace layout in relation to the ground plane

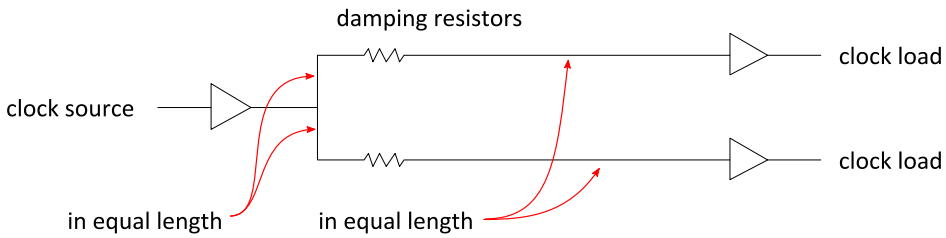


Figure 12: Series termination for multiple clock loads

2.2.4 Trace Bend Geometry

When routing high-speed signals, bends should be minimized. If bends are needed, use 135° bends instead of 90°.

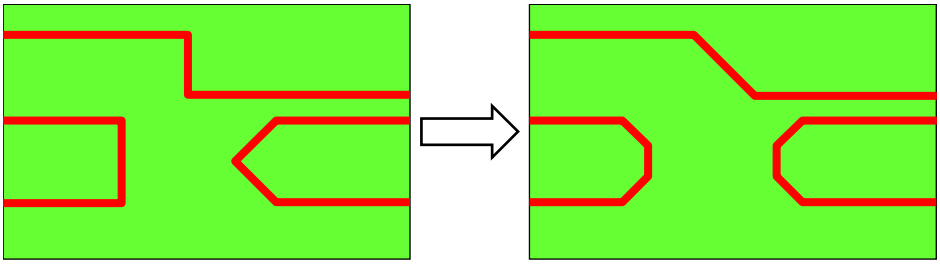


Figure 13: Use 135° bends instead of 90°

Serpentine traces (also called meander) are often needed when a certain trace length needs to be achieved. For high-speed interfaces, if there is space available, it is suggested to keep a minimum distance of four times the trace width between adjacent copper in a single trace. If its space is tight such as LPDDR3 interface, keep a minimum distance of two times the trace width between adjacent copper in a single trace. The individual segments of the bends should be at least 1.5 times the trace width.

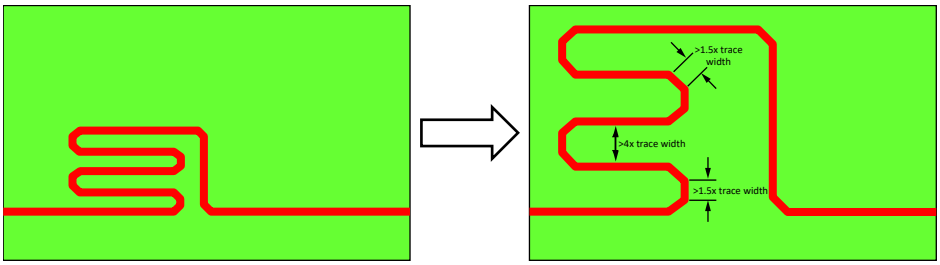


Figure 14: Suggested minimum distance and segment length at bends

2.2.5 Signal Proximity

A minimum distance is required in order to minimize crosstalk between high-speed signals traces. The level of crosstalk depends on the distance between two traces and the length in which they are closely routed. Sometimes, bottlenecks can force the routing of traces closer than to what is normally permitted. Try to minimize such areas and enlarge the distance between the signals outside the bottleneck. If there is space available, try to enlarge the distance between the high speed-signals (and between high-speed and low-speed signals) even if the minimum trace separation requirement has been met.

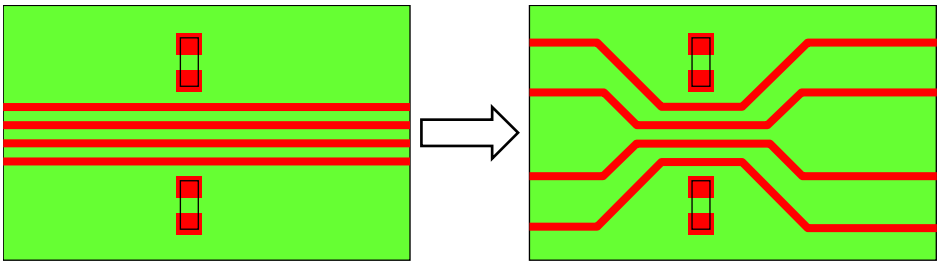


Figure 15: Try to increase spacing between traces whenever it is possible

2.2.6 Trace Stubs

Long stub traces can act as antennas and therefore increase problems complying with EMC standards. Stub traces can also produce reflections which negatively impacts signal integrity. Common sources for stubs are pull-up or pull-down resistors on high-speed signals. If such resistors are required, route the signals as a daisy chain.

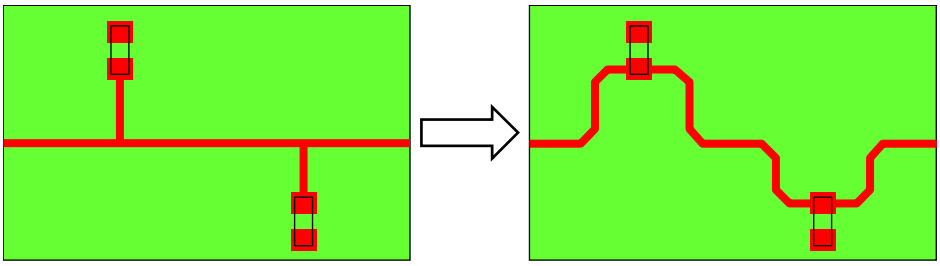


Figure 16: Avoid stub traces by daisy chain routing

Vias can also act as stubs. For example, in a 6-layer board, when a signal changes from layer 1 to 3 by using a via, the via creates a stub which reaches layer 6. Back-drilling the vias in order to avoid such stubs is a quite expensive technology and one which is not supported by most PCB manufacturers. The only practical solution is to reduce the number of vias in high-speed traces.

2.2.7 Ground Planes Under Pads

The impedance of a trace depends on its width and the distance between trace and reference plane. A wide trace has lower impedance than a thin one with the same distance. The same effect also exists for connector and component pads. A large pad has significantly lower impedance than the trace which is connected to the pad. This impedance discontinuity can cause reflections reduces signal integrity. Therefore, under large connector and component pads, a plane obstruct should be placed. The area of the plane should be decided by means of simulation. In this case, an active reference plane should be placed on another layer. This reference plane's net should be same as the normal reference plane. This reference plane needs to be stitched with vias to the normal reference plane.

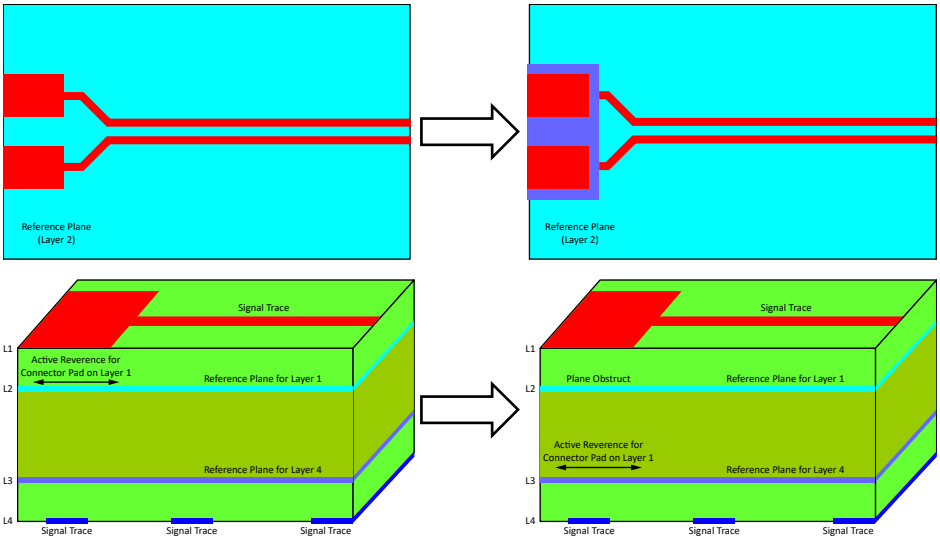


Figure 17: Remove ground plane under large pads

2.2.8 Differential Pair Signals

It is not permitted to place any components or vias between the differential pairs, even if the signals are routed symmetrically. Components and vias between the pairs could lead to EMC compliance problems and create an impedance discontinuity.

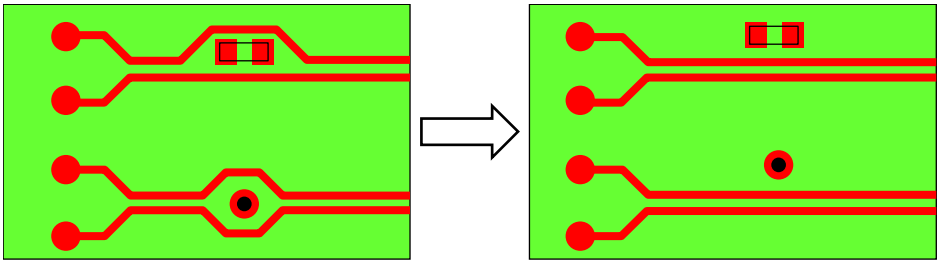


Figure 18: Do not put any components or vias between differential pairs

Vias introduce a huge discontinuity in impedance. Try to reduce the amount of placed vias to a minimum and place the vias symmetrically.

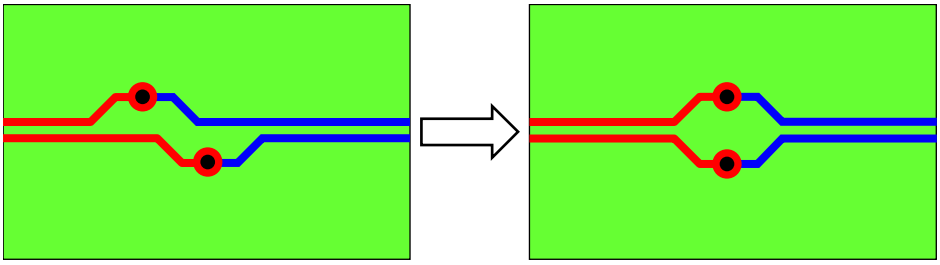


Figure 19: Place vias symmetrical

In order to meet the impedance requirements of a differential pair, both signal traces need to be routed on the same layer. Add the same amount of vias to the traces.

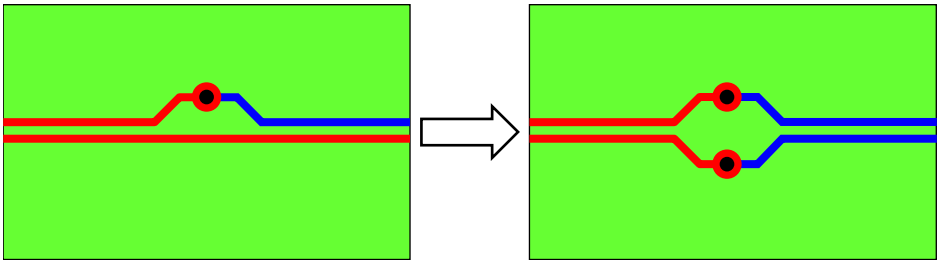


Figure 20: Route pairs on the same layer, place same amount of vias

2.2.9 Length Matching

High-speed interfaces have additional requirements regarding the time of arrival skew between different traces and pairs of signals. For example, in a high-speed parallel bus, all data signals need to arrive within a time period in order to meet the setup and hold time requirements of the receiver. The carrier board designer needs to make sure that the permitted skew is not exceeded. In order to meet this requirement, length matching is required. Often, the requirements are given as a maximum time skew.

Differential pair signals often require a very tight delay skew between the positive and negative signal traces. Therefore, length differences need to be compensated for using serpentines (also called meanders). The geometry of serpentine traces needs to be carefully chosen in order to reduce impedance discontinuity. The following figure shows the requirements for ideal serpentine traces.

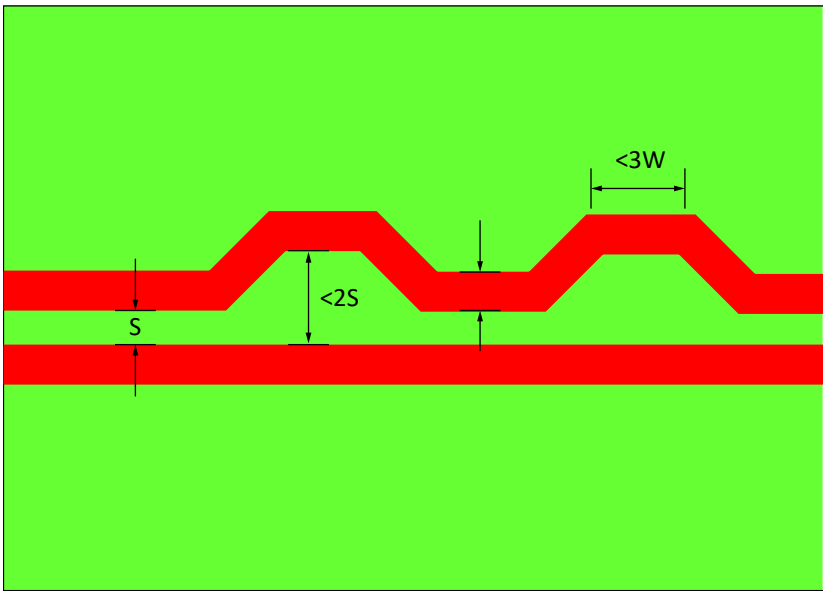


Figure 21: Route pairs on the same layer, place same amount of vias

2.2.9.1 SOM Module Package Breakout Length Matching

As to SOM-3000 module, high speed differential interface such as HDMI, USB ,LVDS, MIPI, and SDIO need to do package breakout length mismatching.

Because package and PCB compensate each other in the location of package breakout.

2.2.9.2 Length Matching Except Package Breakout

The following figure shows the requirements for length matching except package breakout. The serpentine traces should be placed at the origin of the length mismatching. This ensures that the positive and negative signal components are propagated synchronously over the major part of the connection.

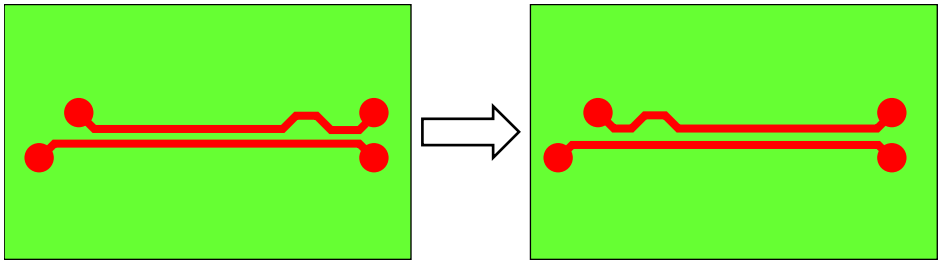


Figure 22: Add length correction to the mismatching point

Bends are a common source of length mismatching. The compensation should be placed close to the bend with a maximum distance of 15mm.

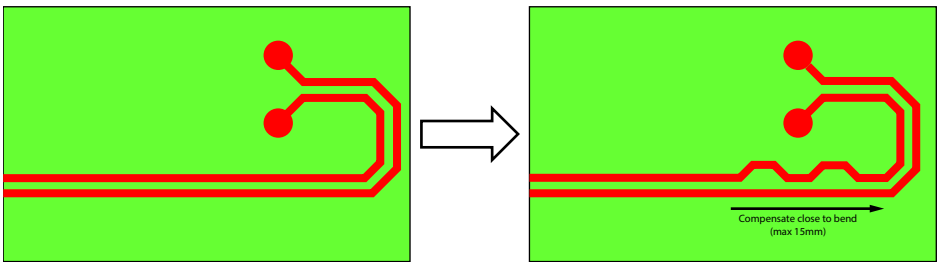


Figure 23: Place length compensation close to a bend

Each segment of a differential pair connection needs to be matched individually. A connection can be segmented by a connector, serial coupling capacitors or vias. The two bends in the following figure would compensate each other. Since the vias divide the differential pair into two segments, the bends need to be compensated individually. This makes sure that the positive and negative signals are propagated synchronously through the vias. The violation of this rule might need to be checked manually as the DRC may only check the length difference over the whole connection.

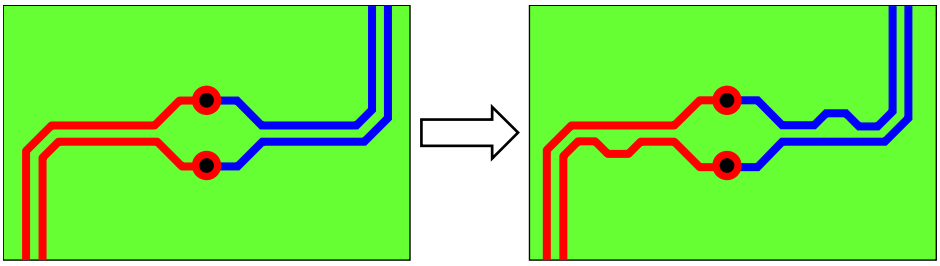


Figure 24: Length differences need to be compensated in each segment

The signal speed is not equal for different layers. Since the difference is hard to estimate, it is preferable to route signals on the same layer if they need to be matched. For example, the MIPI display interface requires tight matching between the signal pairs and the clock pair.

It is preferable to route all data and clock signals of a MIPI DSI channel on the same layer.

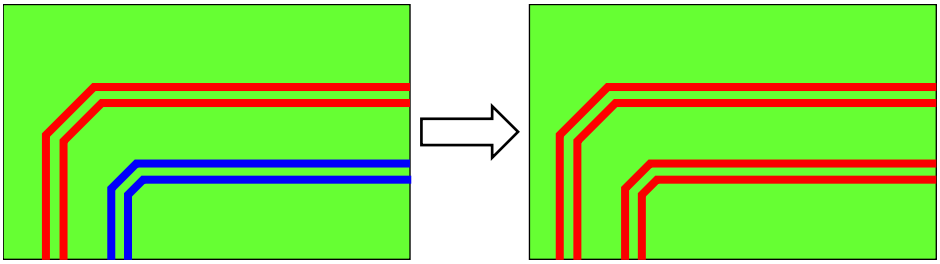


Figure 25: Pairs within same Interface should be routed preferable on same layer

Whenever possible, a symmetric breakout of differential pair signal is preferred in order to avoid the need of serpentine traces.

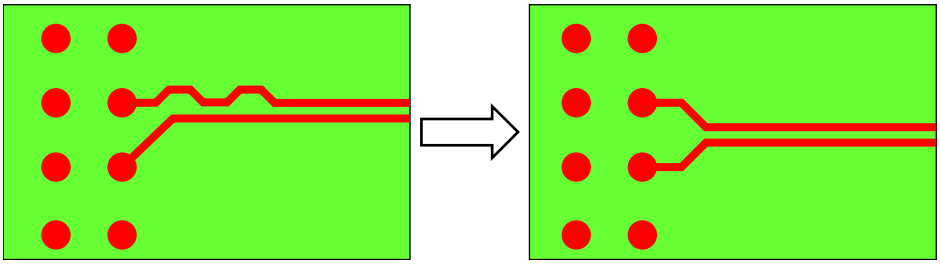


Figure 26: Preferred symmetrical breakout

If the space between the pads permits, try to add a small loop to the shorter trace. This is the preferred solution for matching the length difference as opposed to creating a serpentine trace.

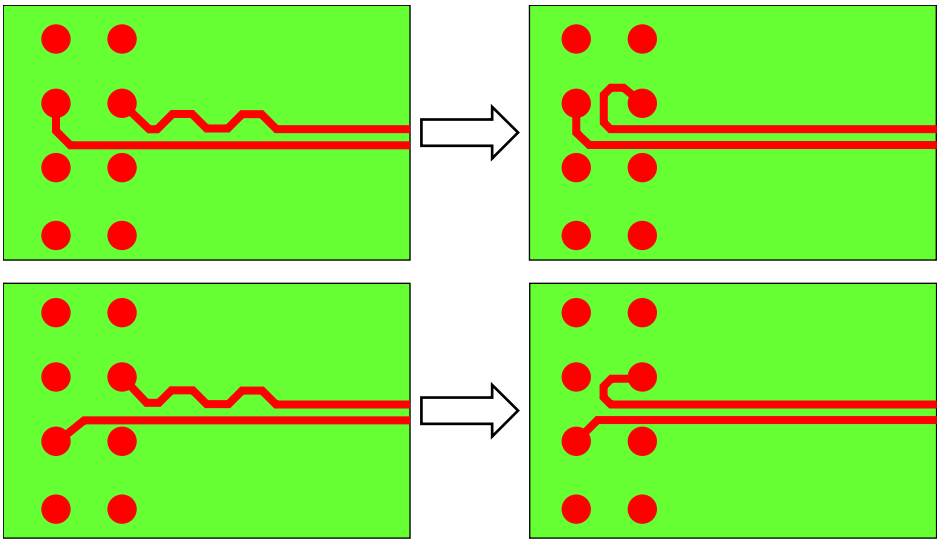


Figure 27: Preferred breakout of differential pairs

3. SOM-3000 Module & M.2 Slot Specification Overview

3.1 SOM-3000 Module Placement

The following figure shows the depiction of the top view of the carrier board PCB with the appropriate amount of space reserved for the SOM-3000 module.

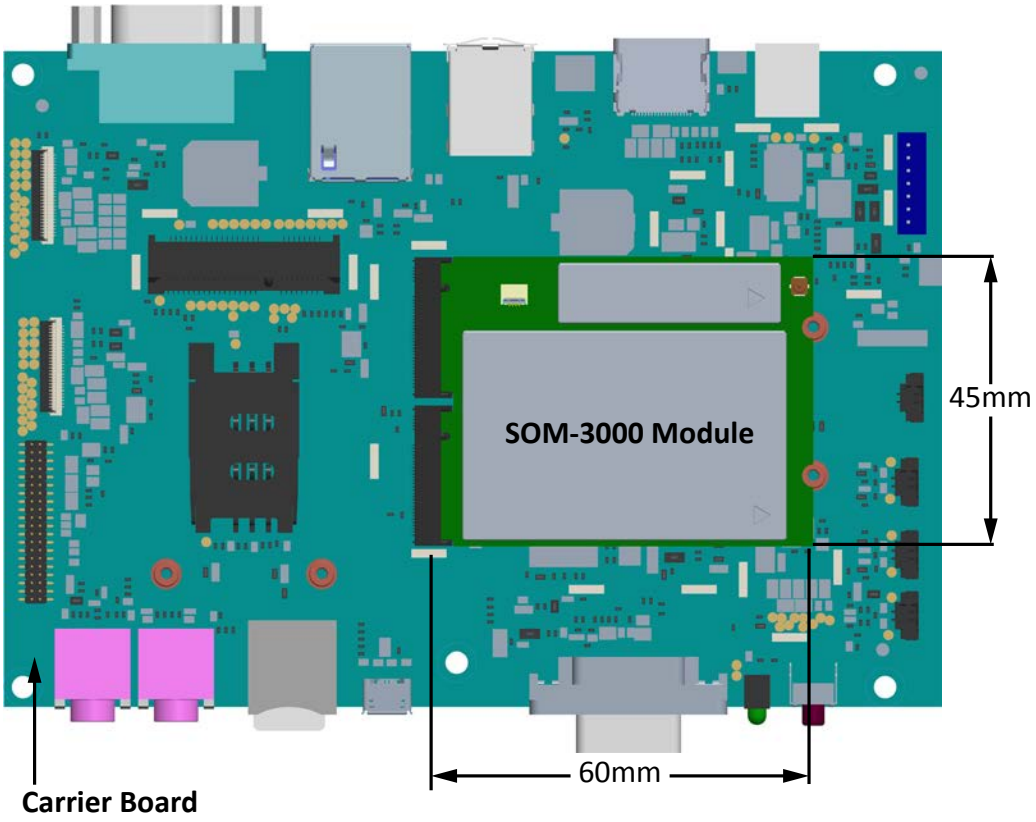


Figure 28: SOM-3000 module placement example on the carrier board

3.2 SOM-3000 Module & Carrier Board Dimensions

The following figures show the mechanical dimensions of the SOM-3000 module and the reference carrier board (VAB-935).

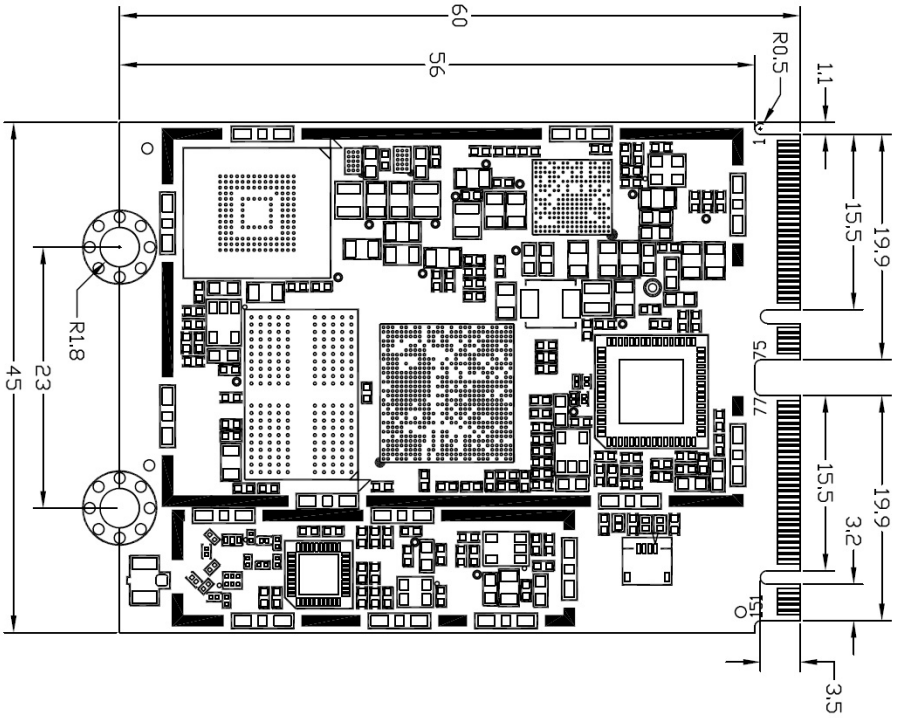


Figure 29: Dimensions of the SOM-3000 module

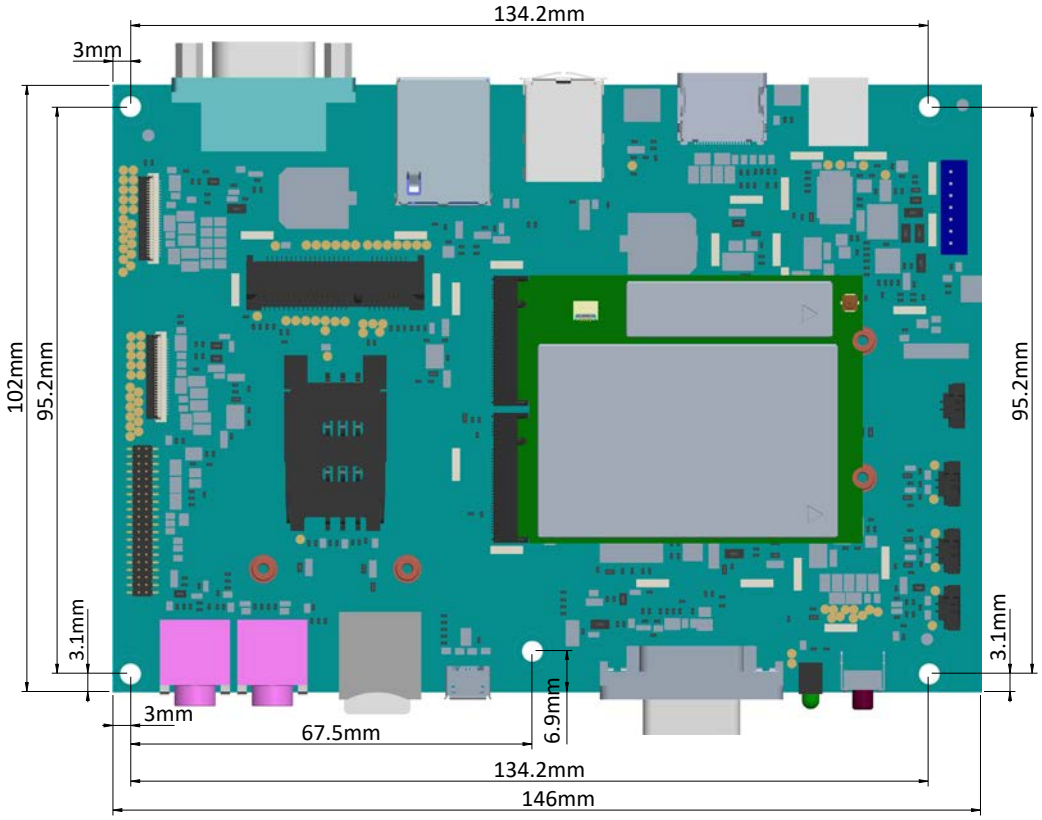


Figure 30: Dimensions of the reference carrier board

3.3 M.2 Slot

The M.2 slot can handle high-speed signals and comprises 132 pins to connect the SOM-3000 module. Table 5 shows the specifications of the sample M.2 slot.

M.2 Slot (VIA Part Number)	Description
99H30-071127	Conn Slot 2E0BC21-S85BM-7H M.2 (NGFF) Connector (KEYM) 75PIN SMD right angle black LCP H=8.5mm Foxconn

Table 05: M.2 slot sample

3.3.1 M.2 Slot Dimensions

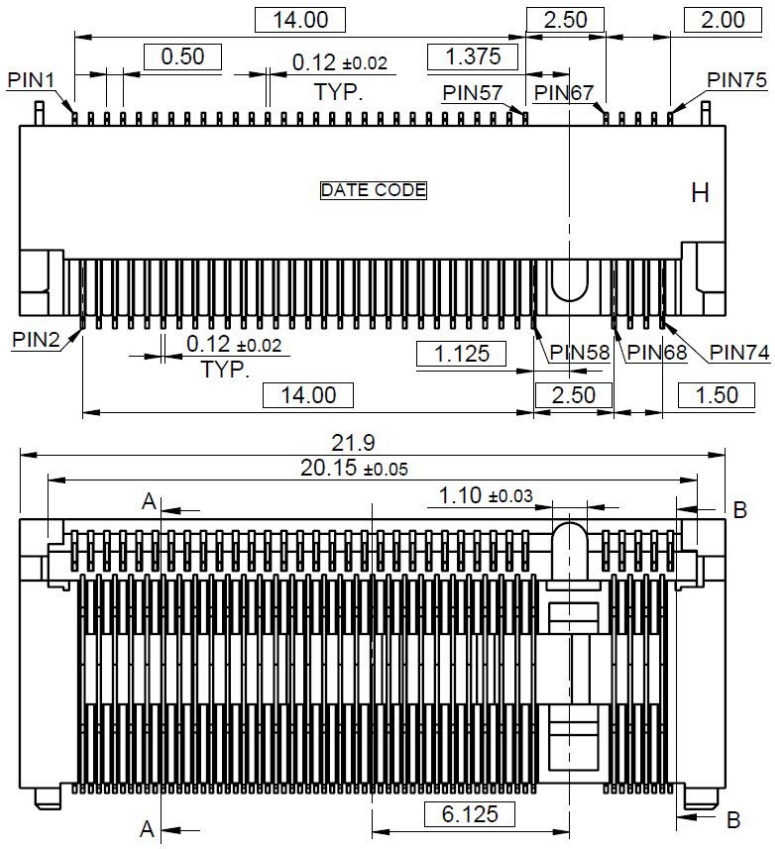


Figure 31: Dimensions of the M.2 slot (top view)

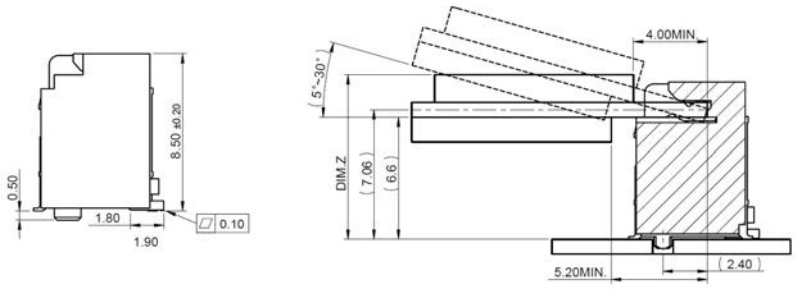


Figure 32: Dimensions of the M.2 slot (side view)

3.3.2 M.2 Slot Height Notes

The M Key M.2 connector height should be calculated carefully to avoid mechanism interference between SOM-3000 module bottom heat sink and carrier board top layer components. For example, if the 0402 components (height less than 0.5mm) are placed on the carrier board top layer (under the SOM-3000 module), then the M Key M.2 connector height should be ≥5mm.

3.3.3 M.2 Slot Placement (unit mm)

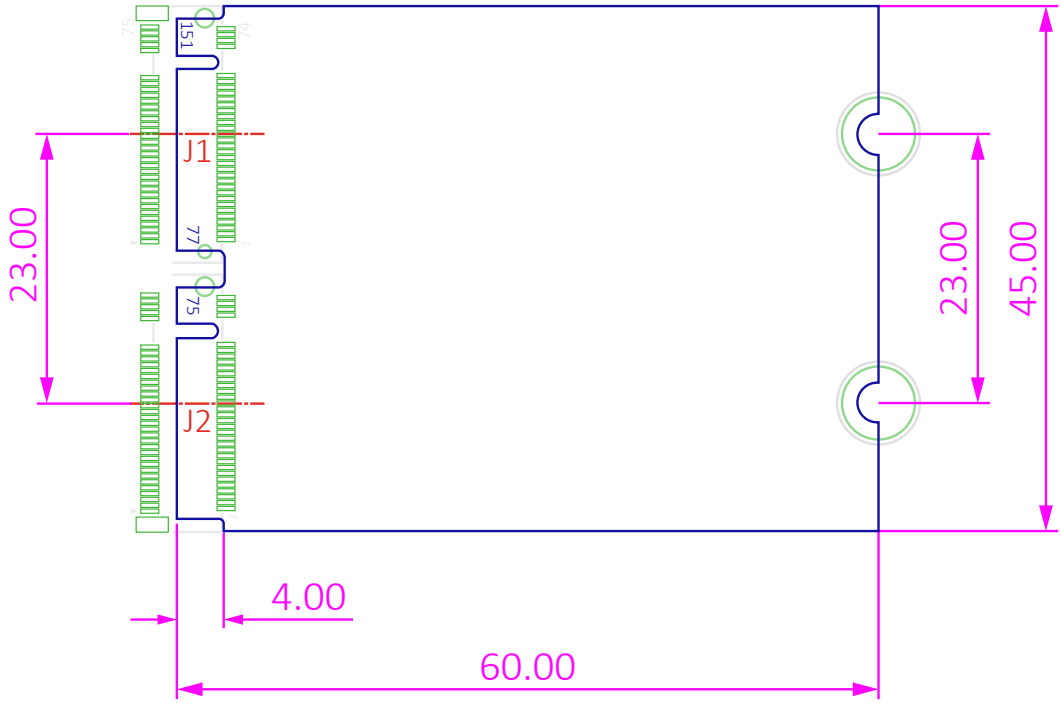


Figure 33: M.2 slot placement

3.4 M.2 Slot Pin Assignments

The M.2 slot consists of 132 pins. The pinouts of the M.2 slot are shown below.

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J2.1	USB_DM_P1	MT8365 USB_DM_P1	3.3V	AVDD33_ USB	AIO	USB_DM_P1	2nd USB2.0 Host D-
J2.2	AU_VIN1_N	MT6390/ MT6357 AU_VIN1_N	2.8V	AVDD28_ MIC	AI	AU_VIN1_N	Earphone MIC, Differential MIC1- input,
J2.3	USB_DP_P1	MT8365 USB_DP_P1	3.3V	AVDD33_ USB	AIO	USB_DP_P1	2nd USB2.0 Host D+
J2.4	AU_VIN1_P	MT6390/ MT6357 AU_VIN1_P	2.8V	AVDD28_ MIC	AI	AU_VIN1_P	Earphone MIC, Differential MIC1+ input, need Vbias on carrier board
J2.5	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J2.6	ACCDET	MT6390/ MT6357 ACCDET	2.8V	AVDD28_ MIC	AI	ACCDET	Earphone MIC, ACCDET
J2.7	USB_DM_P0	MT8365 USB_DM_P0	3.3V	AVDD33_ USB	AIO	USB_DM_P0	1st USB2.0 OTG D-
J2.8	AU_VIN0_N	MT6390/ MT6357 AU_VIN0_N	2.8V	AVDD28_ MIC	AI	AU_VIN0_N	On board MIC, Differential MIC0- input,
J2.9	USB_DP_P0	MT8365 USB_DP_P0	3.3V	AVDD33_ USB	AIO	USB_DP_P0	1st USB2.0 OTG D+
J2.10	AU_VIN0_P	MT6390/ MT6357 AU_VIN0_P	2.8V	AVDD28_ MIC	AI	AU_VIN0_P	On board MIC, differential MIC0+ input, need Vbias on carrier board
J2.11	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.12	AVSS28_AUD	MT6390/ MT6357 AVSS28_AUD			AIO	AVSS28_AUD	Audio analog ground, add a 0 Ohm resistor to ground (Carrier board)
J2.13	USBOTG_ VBUS	USBOTG_ VBUS	5V	USBOTG_ VBUS	Power	USBOTG_ VBUS	1st USB2.0 OTG VBUS power for detect
J2.14	AU_HPR	MT6390/ MT6357 AU_HPR	2.8V	AVDD28_ AUD	AO	AU_HPR	Headphone audio right channel output
J2.15	USBOTG_ID	MT8365 EINT23/ GPIO23/ KPROW1/ I0:IDDIG/ O:WIFI_TXD/ O*CLKM3	1.8V	DVDD18_ IO1	I, PD	IDDIG	1st USB2.0 OTG ID input, High: device, Low: Host
J2.16	AU_HPL	MT6390 AU_HPL			AO	AU_HPL	Headphone audio left channel output
J2.17	USBOTG_ DRVVBUS	MT8365 EINT25/ GPIO25/ B1:KPCOL1/ O:USB_ DRVVBUS	1.8V	VDD18_IO1	I, PD	USBOTG_ DRVVBUS	1st USB2.0 OTG DRVVBUS output, High active
J2.18	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.19	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.20	EXT_GPIO3	MT8365 EINT130/ GPIO130/ O*TDM_ TX_LRCK/ O*I2S3_LRCK	1.8V	DVDD18_ IO1	I, PD	EXT_GPIO3	MT8365 GPIO130, default for SPI_BUSY, input, high active
J2.21	CS_N	MT6390/ MT6357 CS_N	0~4.2V	Vbattery	AI	CS_N	Battery Gas Gauge CS_N

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J2.22	EXT_GPIO2	MT8365 EINT131/ GPIO131/ O*TDM_ TX_MCK/ O*I2S3_MCK	1.8V	DVDD18_ IO1	I, PD	EXT_GPIO2	MT8365 GPIO131,default for NFC_CARD_INT, input, high active
J2.23	CS_P	MT6390/ MT6357 CS_P	0~4.2V	Vbattery	AI	CS_P	Battery Gas Gauge CS_P
J2.24	EXT_GPIO1	MT8365 EINT129/ GPIO129/ O*TDM_TX_ BCK/O*I2S3_ BCK	1.8V	DVDD18_ IO1	I, PD	EXT_GPIO1	MT8365 GPIO129, default for NFC_ CARD_RESET, output, high active
J2.25	BATSNS	MT6390/ MT6357 BATSNS	3.0~4.2V	Vbattery	AI	BATSNS	Battery voltage input
J2.26	SPI_CS	MT8365 EINT26/ GPIO26/ O*SPI_CSB	1.8V	DVDD18_ IO3	I, PD	SPI_CS	SPI_CS,SPI Bus chip select output, default for motor driver
J2.27	SDA0	MT8365 EINT57/ GPIO57/ B1:SDA0_0	1.8V	DVDD18_ IO1	I, PU	SDA0	I2C0 SDA, default connect to G-sensor and DC/DC
J2.28	SPI_MO	MT8365 EINT29/ GPIO29/ O*SPI_MO/ I0*SPI_MI/ I0:DVFSRC_ EXT_REQ	1.8V	DVDD18_ IO3	I, PD	SPI_MO	SPI_MO,SPI Bus master data output, default for motor driver
J2.29	SCL0	MT8365 EINT58/ GPIO58/ B1:SCL0_0	1.8V	DVDD18_ IO1	I, PU	SCL0	I2C0 SCL, default connect to G-sensor and DC/DC
J2.30	SPI_MI	MT8365 EINT28/ GPIO28/ I0*SPI_MI/ O*SPI_MO	1.8V	DVDD18_ IO3	I, PD	SPI_MI	SPI_MI,SPI Bus master data input, default for motor driver
J2.31	EXT_INT3	MT8365 EINT105/ GPIO105/ O*NCLE/ O*TDM_RX_ MCK	1.8V	DVDD18_ MSDC0	O, PD	EXT_INT3	MT8365 EINT105,IO Extender interrupt input, Low active

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J2.32	SPI_CK	MT8365 EINT27/ GPIO27/ O*SPI_CLK	1.8V	DVDD18_ IO3	I, PD	SPI_CK	SPI_CK,SPI Bus clock output, default for motor driver
J2.33	EXT_INT2	MT8365 EINT115/ GPIO115/ B0*I2S0_ LRCK/ O*I2S1_ LRCK/ O*I2S2_ LRCK/ O*I2S3_ LRCK/ O:PWM_B/ O*SPDIF_ OUT	1.8V	DVDD18_ IO1	I, PD	EXT_INT2	MT8365 EINT115, G-sensor interrupt input, High active
J2.34	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.35	EXT_INT1	EINT67/ GPIO67/ I0*CMPCLK/ O*TDM_ RX_BCK/ B0*I2S0_BCK	1.8V	DVDD18_ IO3	I, PD	EXT_INT1	MT8365 EINT67, Reserved
J2.36	URXD2	MT8365 EINT39/ GPIO39/ I1:URXD2/ O:UTXD2/ I1:UCTS1/ I0:IDDIG/ O*I2S2_ MCK/I1: DSP_URXD0	1.8V	DVDD18_ IO1	I, PD	URXD2	UART2 RXD, default for NFC
J2.37	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.38	UTXD2	MT8365 EINT40/ GPIO40/ O:UTXD2/ I1:URXD2/ O:URTS1/ O:USB_ DRVVBUS/ O*I2S3_ MCK/O: DSP_UTXD0	1.8V	DVDD18_ IO1	I, PD	UTXD2	UART2 TXD, default for NFC
J2.39	TX_CH2_P	LT8618SXB TX_D2+	3.3V	HDMI_ VCC33	AO	TX_CH2_P	HDMI1.4 output, TX_D2+

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J2.40	UTXD1	MT8365 EINT38/ GPIO38/ O:UTXD1/ I1:URXD1/ O:URTS2/ O*I2S1_ MCK/O: DSP_UTXD0	1.8V	DVDD18_ IO1	I, PD	UTXD1	UART1 TXD output, default connect to RS232 transceiver
J2.41	TX_CH2_M	LT8618SXB TX_D2-	3.3V	HDMI_ VCC33	AO	TX_CH2_M	HDMI1.4 output,TX_ D2-
J2.42	URXD1	MT8365 EINT37/ GPIO37/ I1:URXD1/ O:UTXD1/ I1:UCTS2/ I0:DVFSRC_ EXT_REQ/ O*I2S0_ MCK/I1: DSP_URXD0	1.8V	DVDD18_ IO1	I, PD	URXD1	UART1 RXD input, default connect to RS232 transceiver
J2.43	TX_CH1_P	LT8618SXB TX_D1+	3.3V	HDMI_ VCC33	AO	TX_CH1_P	HDMI1.4 output,TX_ D1+
J2.44	MCU_INT	MT8365 EINT132/ GPIO132/ O*TDM_ TX_DATA0/ O*I2S3_DO	1.8V	DVDD18_ IO1	I, PD	EINT132	MCU_INT, interrupt input, high active, connect to MCU
J2.45	TX_CH1_M	LT8618SXB TX_D1-	3.3V	HDMI_ VCC33	AO	TX_CH1_M	HDMI1.4 output, TX_D1-
J2.46	MCU_WDI	MT8365 EINT133/ GPIO133/ O*TDM_TX_ DATA1	1.8V	DVDD18_ IO1	I, PD	GPIO133	Watch dog feed output, High pulse active, connect to MCU
J2.47	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.48	SYSRSTB	MT8365 System Reset	1.8V	DVDD18_ IO0	I, PU	SYSRSTB	System Reset input, Low active
J2.49	TX_CH0_P	LT8618SXB TX_D0+	3.3V	HDMI_ VCC33	AO	TX_CH0_P	HDMI1.4 output, TX_D0+
J2.50	MCU_STATUS	MT8365 EINT64/ GPIO64/ B1:SCL3_0 (default) MT6390 PWRKEY (Optional)	1.8V	DVDD18_ IO0	I, PU	GPIO64	MCU_STATUS, Low: MCU upgrading; High: MCU work

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J2.51	TX_CH0_M	LT8618SXB TX_D0-	3.3V	HDMI_ VCC33	AO	TX_CH0_M	HDMI1.4 output,TX_ D0-
J2.52	KPCOL0	MT8365 EINT24/ GPIO24/ B1:KPCOL0	1.8V	DVDD18_ IO1	I, PU	KPCOL0	Connect to firmware download key, input, Low active
J2.53	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.54	EXT_3V3_ ENABLE	MT8365 EINT70/ GPIO70/ CMDAT2/I0* TDM_RX_DI/ I0*I2S0_DI	1.8V	DVDD18_ IO3	I, PD	GPIO70	Carrier board Power enable, output, High active, suspend off
J2.55	TX_CLK_P	LT8618SXB TX_CLK+	3.3V	HDMI_ VCC33	AO	TX_CLK_P	HDMI1.4 output, TX_CLK+
J2.56	EXT_PMIC_ EN1	MT6390/ MT6357 EXT_PMIC_ EN1	1.8V	DVDD18_ IO0	O, PD	EXT_PMIC_ EN1	Carrier board power enable, output, High active, suspend on
J2.57	TX_CLK_M	LT8618SXB TX_CLK-	3.3V	HDMI_ VCC33	AO	TX_CLK_M	HDMI1.4 output, TX_CLK-
J2.58	PWM_A	MT8365 EINT114/ GPIO114/ I0*I2S0_DI/ O*I2S1_DO/ I0*I2S2_DI/ O*I2S3_DO/ O:PWM_A/ I0*SPDIF_IN	1.8V	DVDD18_ IO1	I, PD	PWM_A	PWM_A output, connect to 1st motor PWM
J2.67	ADC_VIN0	MT8365 AUXIN2	0~1.45V	AVDD18_AP	AI	AUXIN2	ADC0 input , default for Key buttons
J2.68	PWM_C	MT8365 EINT21/ GPIO21/ DSI_TE/ O:PWM_C/ I0:DVFSRC_ EXT_REQ	1.8V	DVDD18_ IO3	I, PD	PWM_C	PWM_C output, connect to 2nd motor PWM
J2.69	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.70	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.71	VSYS	VSYS	3.4~4.2V	VSYS	Power	VSYS	System Power supply
J2.72	VSYS	VSYS	3.4~4.2V	VSYS	Power	VSYS	System Power supply
J2.73	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.74	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J2.75	VSYS	VSYS	3.4~4.2V	VSYS	Power	VSYS	System Power supply
J1.1	TX_CEC	LT8618SXB TX_CEC	3.3/5V	HDMI_ VCC33	I, PU	TX_CEC	HDMI1.4 TX CEC Input

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J1.2	VIN_DC	MT6390/ MT6357 VIN_DC	3.4~4.2V	VIN_DC	Power	VIN_DC	DC input voltage input, Adapter or Battery plug in detect
J1.3	TX_DDCSCL	LT8618SXB TX_DDCSCL	3.3/5V	HDMI_ VCC33	I, PU	TX_DDCSCL	HDMI1.4 TX DDC SCL
J1.4	TX_HPD	LT8618SXB TX_HPD	3.3/5V	HDMI_ VCC33	I, PD	TX_HPD	HDMI1.4 TX HPD, HDMI plug in detect, high active
J1.5	TX_DDCSDA	LT8618SXB TX_DDCSDA	3.3/5V	HDMI_ VCC33	I, PU	TX_DDCSDA	HDMI1.4 TX DDC SDA
J1.6	SD_WP	MT8365 EINT109/ GPIO109/ I0:TSF_IN	1.8V	DVDD18_ MSDC0	I, PU	GPIO109	SD Card write protect input, Low active
J1.7	SDA2	MT8365 EINT61/ GPIO61/ B1:SDA2_0	1.8V	DVDD18_ IO3	I, PU	SDA2	I2C2 SDA, default connect to front camera and MCU/IO extender
J1.8	MSDC1_INSI	MT8365 EINT63/ GPIO63/ B1:SDA3_0	1.8V	DVDD18_ IO3	I, PU	GPIO63	SD Card detect input, Low active
J1.9	SCL2	MT8365 EINT62/ GPIO62/ B1:SCL2_0	1.8V	DVDD18_ IO3	I, PU	SCL2	I2C2 SCL, default connect to front camera and MCU/IO extender
J1.10	MSDC1_ DAT1	MT8365 EINT90/ GPIO90/ B0*MSDC1_ DAT1/ I0*SPDIF_IN	3.0V	DVDD28_ MSDC1	I, PU	MSDC1_DAT1	SDIO3.0 Bus DAT1, connect to SD Card
J1.11	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.12	MSDC1_ DAT0	MT8365 EINT89/ GPIO89/ B0*MSDC1_ DAT0/ O:PWM_C	3.0V	DVDD28_ MSDC1	I, PU	MSDC1_DAT0	SDIO3.0 Bus DAT0, connect to SD Card
J1.13	CSI1B_L1N	MT8365 CSI1B_L1N	1.2V	AVDD12_ CSI0	AI	CSI1B_L1N	Camera2 MIPI CSI1 4-lane D3-
J1.14	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.15	CSI1B_L1P	MT8365 CSI1B_L1P	1.2V	AVDD12_ CSI0	AI	CSI1B_L1P	Camera2 MIPI CSI1 4-lane D3+
J1.16	MC1CK	MT8365 EINT88/ GPIO88/ O*MSDC1_ CLK	3.0V	DVDD28_ MSDC1	O, PD	MSDC1_CLK	SDIO3.0 Bus CLK, connect to SD Card

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J1.17	CSI1B_L0N	MT8365 CSI1B_L0N	1.2V	AVDD12_ CSI0	AI	CSI1B_L0N	Camera2 MIPI CSI1 4-lane D1-
J1.18	MSDC1_CMD	MT8365 EINT87/ GPIO87/ B0*MSDC1_ CMD	3.0V	DVDD28_ MSDC1	I, PU	MSDC1_CMD	SDIO3.0 Bus CMD, connect to SD Card
J1.19	CSI1B_L0P	MT8365 CSI1B_L0P	1.2V	AVDD12_ CSI0	AI	CSI1B_L0P	Camera2 MIPI CSI1 4-lane D1+
J1.20	MSDC1_ DAT3	MT8365 EINT92/ GPIO92/ B0*MSDC1_ DAT3/ I1*IRRX/ O:PWM_A	3.0V	DVDD28_ MSDC1	I, PU	MSDC1_DAT3	SDIO3.0 Bus DAT3, connect to SD Card
J1.21	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.22	MSDC1_ DAT2	MT8365 EINT91/ GPIO91/ B0*MSDC1_ DAT2/ O*SPDIF_ OUT	3.0V	DVDD28_ MSDC1	I, PU	MSDC1_DAT2	SDIO3.0 Bus DAT2, connect to SD Card
J1.23	CSI1A_L2N	MT8365 CSI1A_L2N	1.2V	AVDD12_ CSI0	AI	CSI1A_L2N	Camera2 MIPI CSI1 4-lane CLK-
J1.24	SCL1	MT8365 EINT60/ GPIO60/ B1:SCL1_0/ B1*USB_SCL/ B1:DBG_SCL	1.8V	DVDD18_ IO1	I, PU	SCL1	I2C1 SCL ,default connect to capacitive touch panel and rear camera
J1.25	CSI1A_L2P	MT8365 CSI1A_L2P	1.2V	AVDD12_ CSI0	AI	CSI1A_L2P	Camera2 MIPI CSI1 4-lane CLK+
J1.26	SDA1	MT8365 EINT59/ GPIO59/ B1:SDA1_0/ B1*USB_ SDA/ B1:DBG_SDA	1.8V	DVDD18_ IO1	I, PU	SDA1	I2C1 SDA, default connect to capacitive touch panel and rear camera
J1.27	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.28	GPIO_CTP_ RST	MT8365 EINT79/ GPIO79/I0 *CMVSYNC/ O*PCM_TX	1.8V	DVDD18_ IO3	I, PD	GPIO79	CTP Reset output, High active, default connect to capacitive touch panel
J1.29	CSI1A_L1N	MT8365 CSI1A_L1N	1.2V	AVDD12_ CSI0	AI	CSI1A_L1N	Camera2 MIPI CSI1 4-lane D0-

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J1.30	ENIT_CTP_INT	MT8365 EINT78/ GPIO78/ CMHSYNC/ I0*PCM_RX	1.8V	DVDD18_IO3	I, PD	EINT78	CTP interrupt input, High active, default connect to capacitive touch panel
J1.31	CSI1A_L1P	MT8365 CSI1A_L1P	1.2V	AVDD12_CSI0	AI	CSI1A_L1P	Camera2 MIPI CSI1 4-lane D0+
J1.32	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.33	CSI1A_L0N	MT8365 CSI1A_L0N	1.2V	AVDD12_CSI0	AI	CSI1A_L0N	Camera2 MIPI CSI1 4-lane D2-
J1.34	DSI_D3P	MT8365 DSI_D3P/LVDS_TX_D3P	1.8V	AVDD18_DSI	AO	DSI_D3P	LCM MIPI DSI 4-lane D3+ /LVDS TX 4-lane D3+
J1.35	CSI1A_L0P	MT8365 CSI1A_L0P	1.2V	AVDD12_CSI0	AI	CSI1A_L0P	Camera2 MIPI CSI1 4-lane D2+
J1.36	DSI_D3N	MT8365 DSI_D3N/LVDS_TX_D3N	1.8V	AVDD18_DSI	AO	DSI_D3N	LCM MIPI DSI 4-lane D3- /LVDS TX 4-lane D3-
J1.37	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.38	DSI_D1P	MT8365 DSI_D1P/LVDS_TX_CKP	1.8V	AVDD18_DSI	AO	DSI_D1P	LCM MIPI DSI 4-lane D1+ /LVDS TX 4-lane CK+
J1.39	CSI0B_L2N	MT8365 CSI0_RDN1_B	1.2V	AVDD12_CSI0	AI	CSI0B_L2N	Camera1 MIPI CSI0 B 2-lane D1-
J1.40	DSI_D1N	MT8365 DSI_D1N/LVDS_TX_CKN	1.8V	AVDD18_DSI	AO	DSI_D1N	LCM MIPI DSI 4-lane D1- /LVDS TX 4-lane CK-
J1.41	CSI0B_L2P	MT8365 CSI0_RDP1_B	1.2V	AVDD12_CSI0	AI	CSI0B_L2P	Camera1 MIPI CSI0 B 2-lane D1+
J1.42	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.43	CSI0B_L0N	MT8365 CSI0_RDN1/ CSI0_RDN0_B	1.2V	AVDD12_CSI0	AI	CSI0B_L0N	Camera1 MIPI CSI0 4-lane D1-/CSI0B 2-lane D0-
J1.44	DSI_CKP	MT8365 DSI_CKP/LVDS_TX_D2P	1.8V	AVDD18_DSI	AO	DSI_CKP	LCM MIPI DSI 4-lane CK+ /LVDS TX 4-lane D2+
J1.45	CSI0B_L0P	MT8365 CSI0_RDP1/ CSI0_RDP0_B	1.2V	AVDD12_CSI0	AI	CSI0B_L0P	Camera1 MIPI0 CSI0 4-lane D1+/CSI0B 2-lane D0+
J1.46	DSI_CKN	MT8365 DSI_CKN/LVDS_TX_D2N	1.8V	AVDD18_DSI	AO	DSI_CKN	LCM MIPI DSI 4-lane CK- /LVDS TX 4-lane D2-
J1.47	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.48	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.49	CSI0B_L1N	MT8365 CSI0_RDN3/ CSI0_RCN_B	1.2V	AVDD12_CSI0	AI	CSI0B_L1N	Camera1 MIPI CSI0 4-lane D3-/CSI0B 2-lane CLK-

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J1.50	DSI_D2N	MT8365 DSI_D2N/LVDS_TX_D0N	1.8V	AVDD18_DSI	AO	DSI_D2N	LCM MIPI DSI 4-lane D2- /LVDS TX 4-lane D0-
J1.51	CSI0B_L1P	MT8365 CSI0_RDP3/ CSI0_RCP_B	1.2V	AVDD12_CSI0	AI	CSI0B_L1P	Camera1 MIPI CSI0 4-lane D3+/CSI0B 2-lane CLK+
J1.52	DSI_D2P	MT8365 DSI_D2P/LVDS_TX_D0P	1.8V	AVDD18_DSI	AO	DSI_D2P	LCM MIPI DSI 4-lane D2+ /LVDS TX 4-lane D0+
J1.53	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.54	DSI_D0N	MT8365 DSI_D0N/LVDS_TX_D1N	1.8V	AVDD18_DSI	AO	DSI_D0N	LCM MIPI DSI 4-lane D0- /LVDS TX 4-lane D1-
J1.55	CSI0A_L0N	MT8365 CSI0_RDN2/ CSI0_RDN0_A	1.2V	AVDD12_CSI0	AI	CSI0A_L0N	Camera1 MIPI CSI0 4-lane D2-/CSI0A 2-lane D0-
J1.56	DSI_D0P	MT8365 DSI_D0P/LVDS_TX_D1P	1.8V	AVDD18_DSI	AO	DSI_D0P	LCM MIPI DSI 4-lane D0+ /LVDS TX 4-lane D1+
J1.57	CSI0A_L0P	MT8365 CSI0_RDP2/ CSI0_RDP0_A	1.2V	AVDD12_CSI0	AI	CSI0A_L0P	Camera1 MIPI CSI0 4-lane D2+/CSI0A 2-lane D0+
J1.58	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground
J1.67	CSI0A_L1N	MT8365 CSI0_RDN0/ CSI0_RCN_A	1.2V	AVDD12_CSI0	AI	CSI0A_L1N	Camera1 MIPI CSI0 4-lane D0-/CSI0A 2-lane CLK-
J1.68	LCM_ENN	MT8365 EINT127/ GPIO127/ I0*DMIC3_DAT0/I0* TDM_RX_DI	1.8V	DVDD18_IO1	I, PD	GPIO127	LCM_ENN,LCM VBIAS/VIO enable Output, High active
J1.69	CSI0A_L1P	MT8365 CSI0_RDP0/ CSI0_RCP0_A	1.2V	AVDD12_CSI0	AI	CSI0A_L1P	Camera MIPI CSI0 4-lane D0+/CSI0A 2-lane CLK+
J1.70	LCM_ENP	MT8365 EINT116/ GPIO116/ B0*I2S0_BCK/O*I2S1_BCK/O*I2S2_BCK/O*I2S3_BCK/ O:PWM_C/ I1*IRRX	1.8V	DVDD18_IO1	I, PD	GPIO116	LCM_ENP,LCM Backlight enable output, High active,
J1.71	GND_SIGNAL	Ground			Power	Ground	SIGNAL Ground

PIN#	PIN Name	GPIO#	Voltage Level	Power Domain	I/O Reset	Assignment	Function
J1.72	LCM_RST	MT8365 EINT20/ GPIO20/ LCM_RST/ O:PWM_B	1.8V	DVDD18_ IO3	I, PD	LCM_RST	LCM_RST,LCD Reset output, High pulse active
J1.73	CSI0A_L2N	MT8365 CSI0_RCN/ CSI0_ RDN1_A	1.2V	AVDD12_ CSI0	AI	CSI0A_L2N	Camera MIPI CSI0 4-lane CLK-/CSI0A 2-lane D1-
J1.74	DISP_PWM	MT8365 EINT19/ GPIO19/ DISP_PWM/ O:PWM_A	1.8V	DVDD18_ IO3	I, PD	DISP_PWM	DISP_PWM,LCM Brightness PWM output
J1.75	CSI0A_L2P	MT8365 CSI0_RCP/ CSI0_RDP1_A	1.2V	AVDD12_ CSI0	AI	CSI0A_L2P	Camera MIPI CSI0 4-lane CLK+/CSI0A 2-lane D1+

Table 06: M.2 slot pinouts

3.4.1 M.2 Slot Reference Schematics

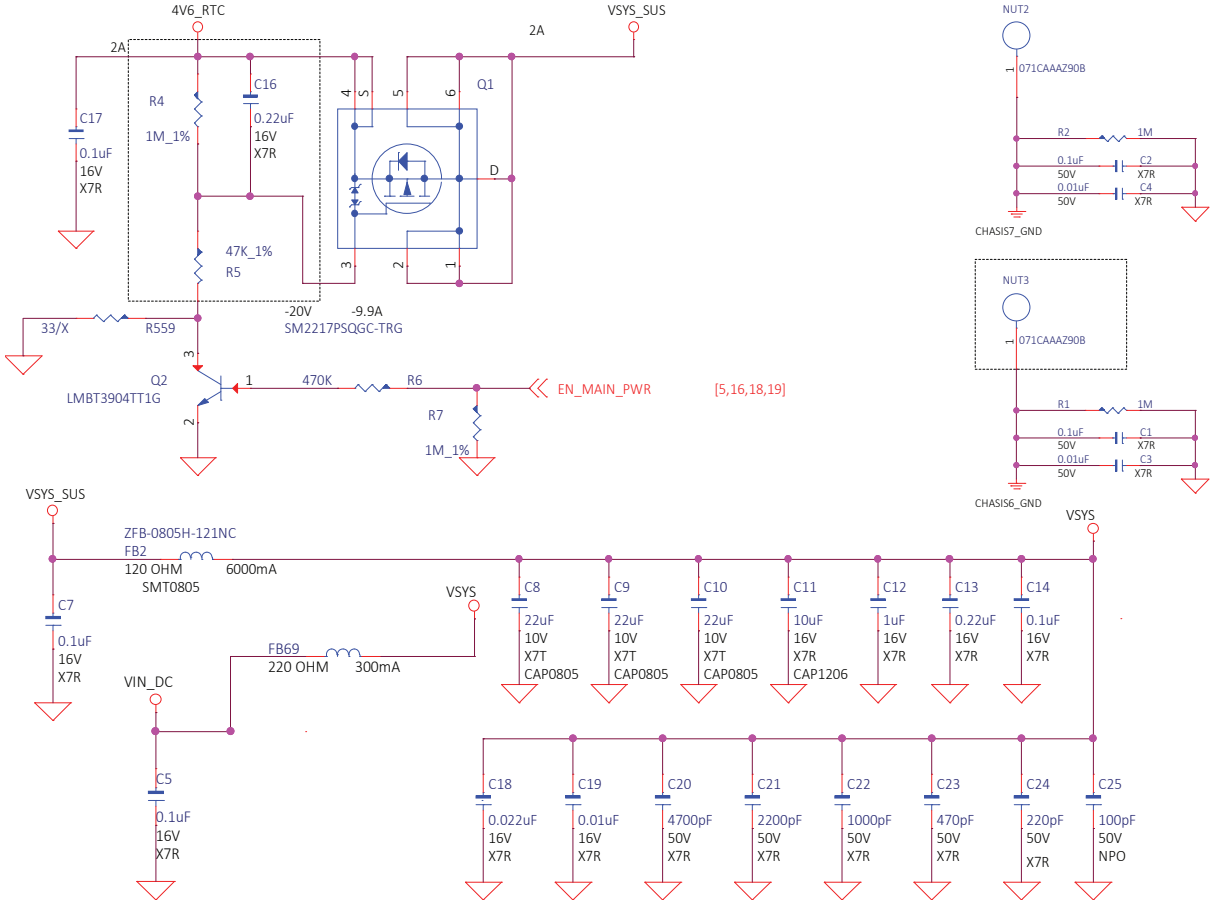


Figure 34: M.2 slot reference circuitry (part 1)

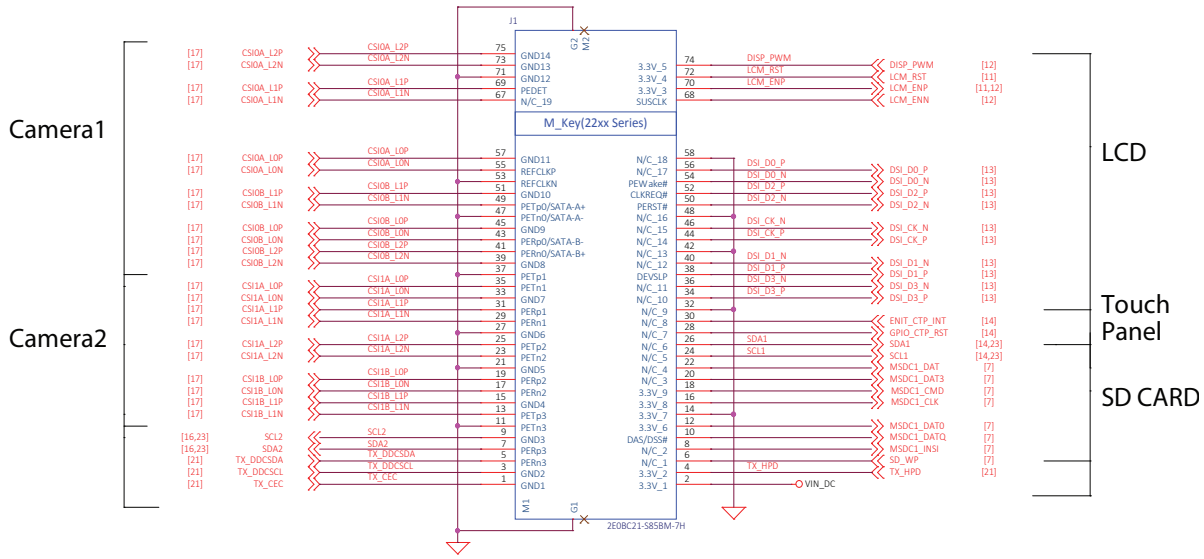


Figure 35: M.2 slot reference circuitry (part 2)

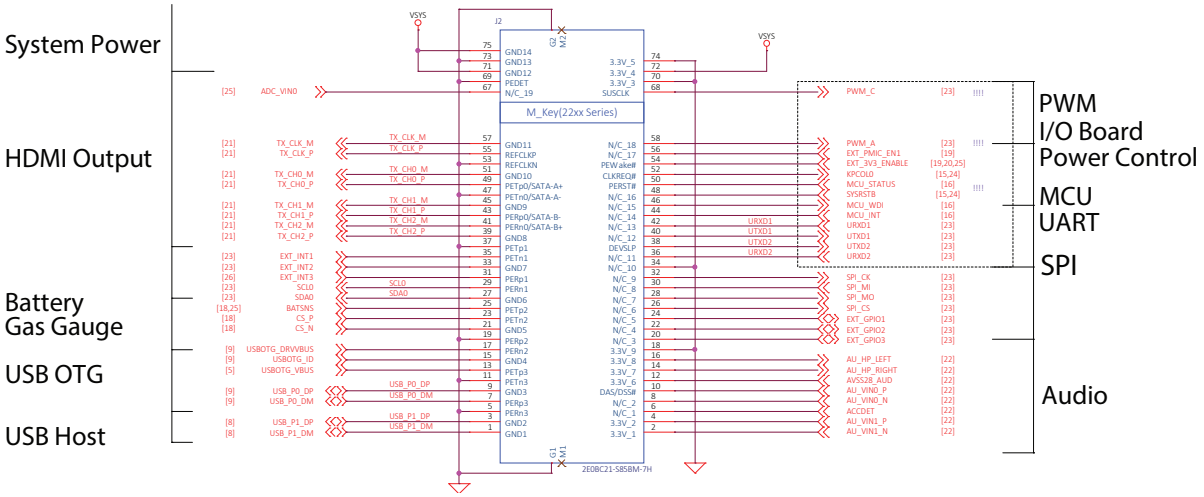


Figure 36: M.2 slot reference circuitry (part 3)

4. Layout & Routing Recommendation

The information presented in this chapter includes the signal definition, topology, layout and routing guidelines for each bus interface, and reference schematics example. The information provided is intended for designing carrier boards that are compliant with the SOM-3000 module.

4.1 HDMI Interface

The SOM-3000 module features one HDMI interface. The HDMI interface uses four control signals, one differential clock, and three differential data pair signals that carry video and audio signals.

4.1.1 HDMI Signal Definition

Signal Name	Pin #	Pad Characteristics		Description
		Voltage	Type	
TX _CLK_M	J2.57		AO	HDMI differential clock – minus
TX _CLK_P	J2.55		AO	HDMI differential clock –plus
TX _CH0_M	J2.51		AO	HDMI differential transmit 0 – minus
TX _CH0_P	J2.49		AO	HDMI differential transmit 0–plus
TX _CH1_M	J2.45		AO	HDMI differential transmit 1 – minus
TX _CH1_P	J2.43		AO	HDMI differential transmit 1–plus
TX_CH2_M	J2.41		AO	HDMI differential transmit 2 – minus
TX_CH2_P	J2.39		AO	HDMI differential transmit 2–plus
TX_CEC	J1.1	3.3V	B-PU	HDMI consumer electronics control configurable I/O
TX_DDCSCL	J1.3	5V	B-PU	HDMI display data channel – clock configurable I/O
TX_DDCSDA	J1.5	5V	B-PU	HDMI display data channel – data configurable I/O
TX_HPD	J1.4	5V	B-PD	HDMI hot plug detect configurable I/O

Table 07: HDMI signal definition

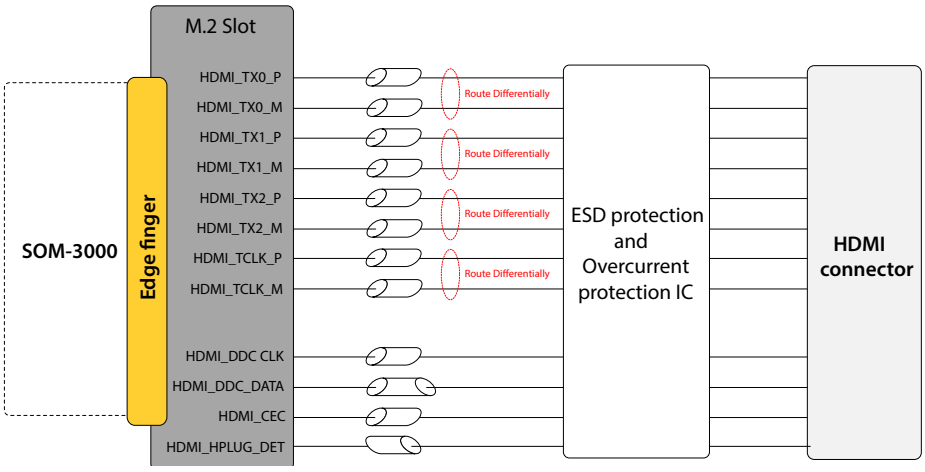


Figure 37: HDMI routing topology

4.1.2 HDMI Layout & Routing Recommendations

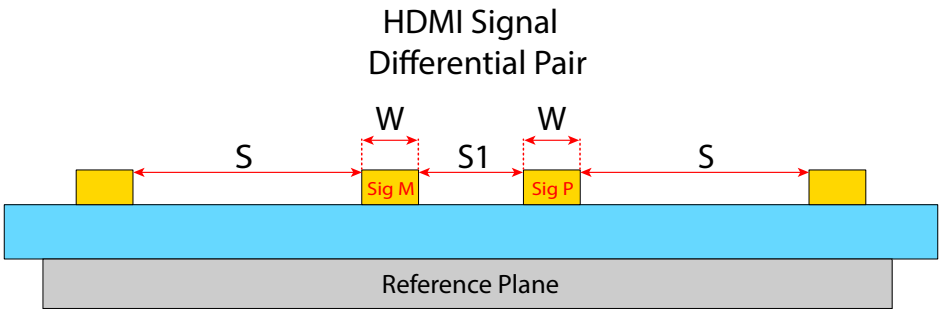


Figure 38: HDMI differential trace width and spacing example

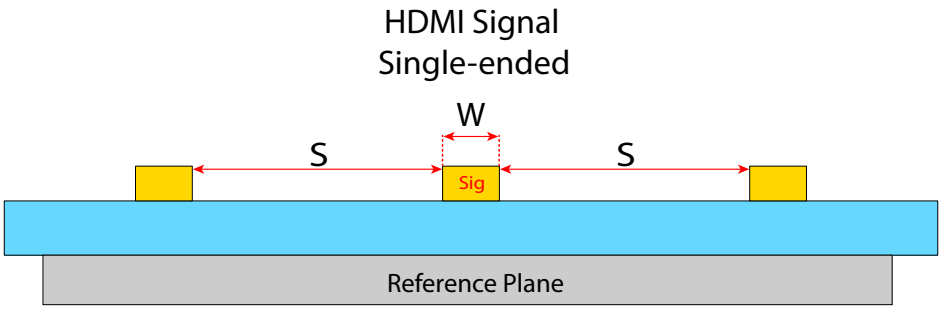


Figure 39: HDMI single-ended trace width and spacing example

Metrics			
General Information	Clock frequency		25MHz - 600MHz
	Data rate		6.0 Gbit/s per lane
Impedance	Differential	Main route	100Ω ± 3%
		Connector	100Ω ± 10%
	Single-ended	Main route	50Ω ± 20%
		Connector	50Ω ± 30%
Length match	Differential pair trace mismatch		<5mil
	Pair to pair trace mismatch		<27mil
Spacing	Spacing to all other signals		4 x line width
	Spacing data lane-to-lane		3 x line width

Table 08: HDMI layout guidelines

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
TX_CH2_P	578.393	6000	-0.25	6.75	83.52	-0.04	1	Inter-pair
TX_CH2_M	578.641				83.56			
TX_CH2_P			-8.53	29.74		-1.23	5	Pair-to-Pair
TX_CH2_M			-9.45			-1.36		
TX_CH0_P	584.078	6000	-0.71	6.75	84.34	-0.10	1	Inter-pair
TX_CH0_M	584.786				84.44			
TX_CH0_P			-2.85	29.74		-0.41	5	Pair-to-Pair
TX_CH0_M			-3.31			-0.48		

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
TX_CLK_P	586.923	6000	-1.17	6.75	84.75	-0.17	1	Inter-pair
TX_CLK_M	588.091				84.92			
TX_CH1_P	578.331	6000	0.96	6.75	83.51	0.14	1	Inter-pair
TX_CH1_M	577.373				83.37			
TX_CH1_P			-8.59	29.74		-1.24	5	Pair-to-Pair
TX_CH1_M			-10.72			-1.55		

Table 09: SOM-3000 HDMI trace & via delay

4.1.3 HDMI Reference Schematics

HDMI Output Port

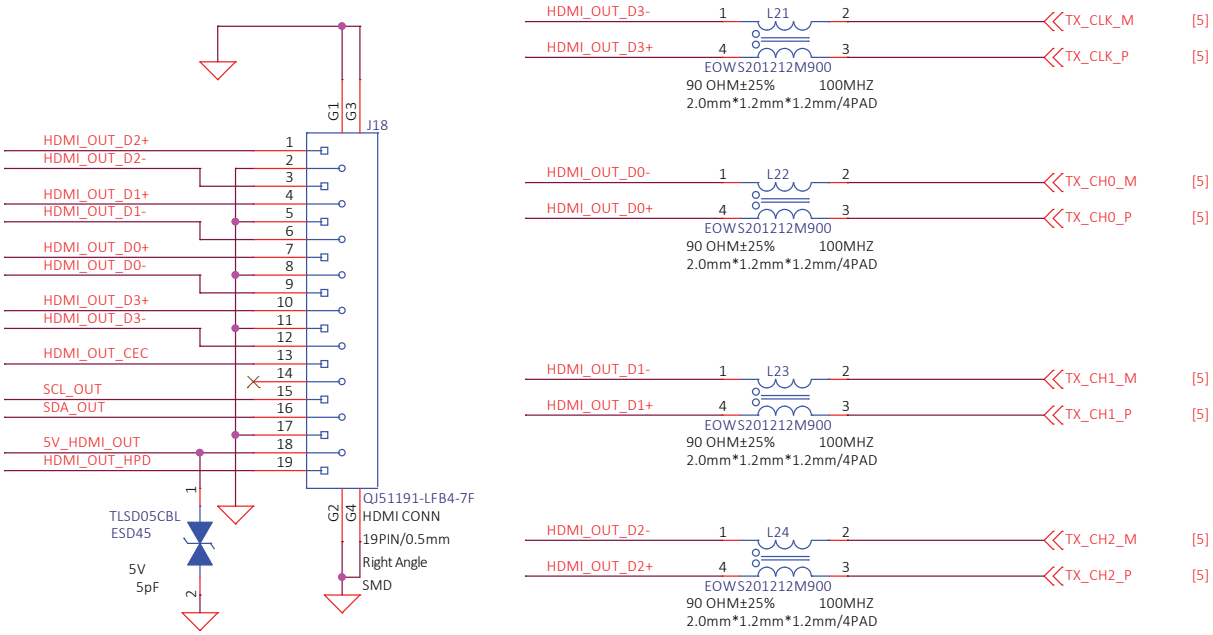


Figure 40: HDMI reference circuitry (Part 1)

To avoid HDMI 5V leakage from the HDMI monitor to carrier board, it is highly recommended to use a P Channel MOS FET as leakage protection on the HDMI 5V circuit.

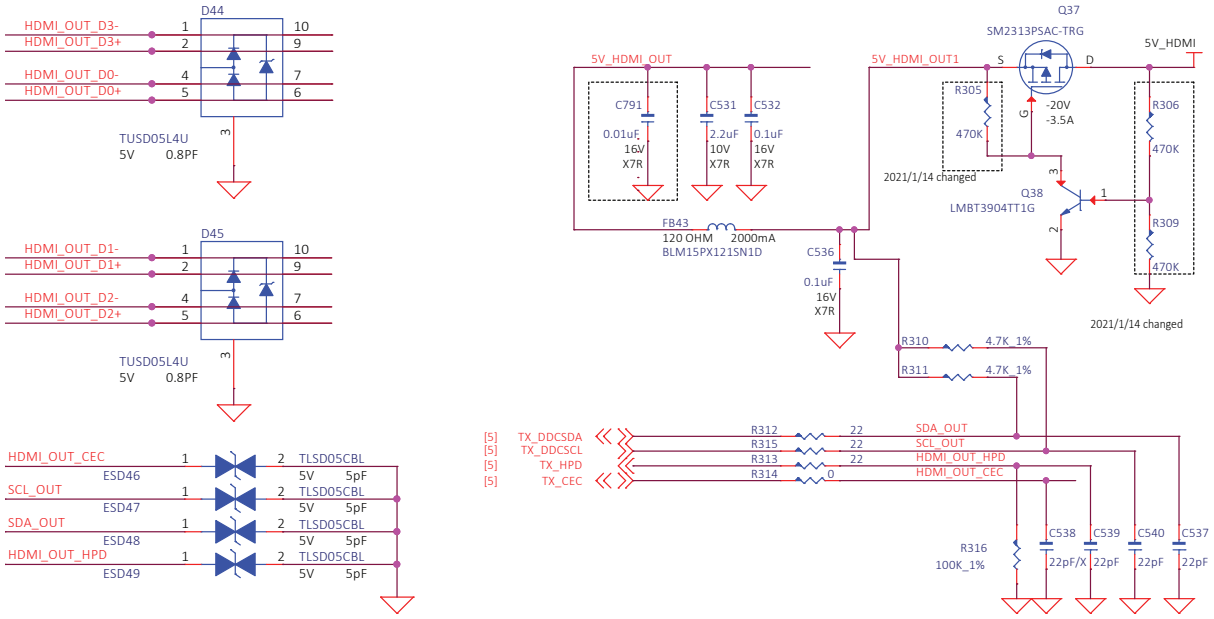


Figure 41: HDMI reference circuitry (Part 2)

For the HDMI compliance test, 5V_HDMI should be less than 5.3V @0mA, and more than 4.8V @55mA. It is highly recommended to use an independent DC/DC converter or charge pump to supply the 5V_HDMI.

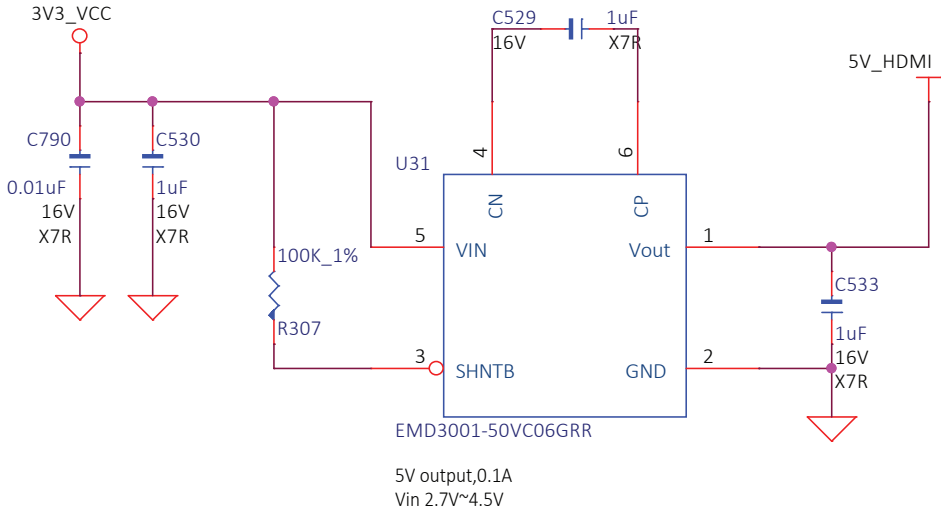


Figure 42: HDMI reference circuitry (Part 3)

For the HDMI compliance test:

- HDMI DDC SDA capacitance loading≤50pF
- HDMI DDC SCL capacitance loading ≤50pF
- HDMI CEC capacitance loading ≤150pF

HDMI CEC should not be pulled High on the carrier board. (It is already pulled High on the VIA SOM-3000 module.)

- High level: 2.5V≤V-CEC ≤3.6V.

HDMI DDC SDA/ DDC SCL must be pulled High to 5V_HDMI on the carrier board.

- High level: 4.5V≤V-SDA ≤5.5V; 4.5V≤V-SCL ≤5.5V.

EMI filter/Common mode choke for HDMI cap loading needs to be under 3pF.

4.2 MIPI DSI Interface

The SOM-3000 module features a MIPI DSI interface. The MIPI DSI interface has four differential pair signals that carry video display signals.

4.2.1 MIPI DSI Signal Definition

The following table provides the definition of the MIPI DSI signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
DSI_D3P	J1.34			AO	MIPI display serial interface lane 3 –positive
DSI_D3N	J1.36			AO	MIPI display serial interface lane 3 –negative
DSI_D1P	J1.38			AO	MIPI display serial interface lane 1 –positive
DSI_D1N	J1.40			AO	MIPI display serial interface lane 1 –negative
DSI_CKP	J1.44			AO	MIPI display serial interface clock – positive
DSI_CKN	J1.46			AO	MIPI display serial interface clock – negative
DSI_D2N	J1.50			AO	MIPI display serial interface lane 2 – negative
DSI_D2P	J1.52			AO	MIPI display serial interface lane 2 – positive
DSI_D0N	J1.54			AO	MIPI display serial interface lane 0 – negative
DSI_D0P	J1.56			AO	MIPI display serial interface lane 0 – positive
DISP_PWM	J1.74	DISP_PWM	1.8V	I, PD	DISP_PWM,LCM Brightness PWM output
LCM_RST	J1.72	LCM_RST	1.8V	I, PD	LCD Reset output, High active
LCM_ENP	J1.70	GPIO116	1.8V	I, PD	LCM power enable output, High active
LCM_ENN	J1.68	GPIO127	1.8V	I, PD	LCM AVDD enable Output, High active

Table 10: MIPI DSI signal definition

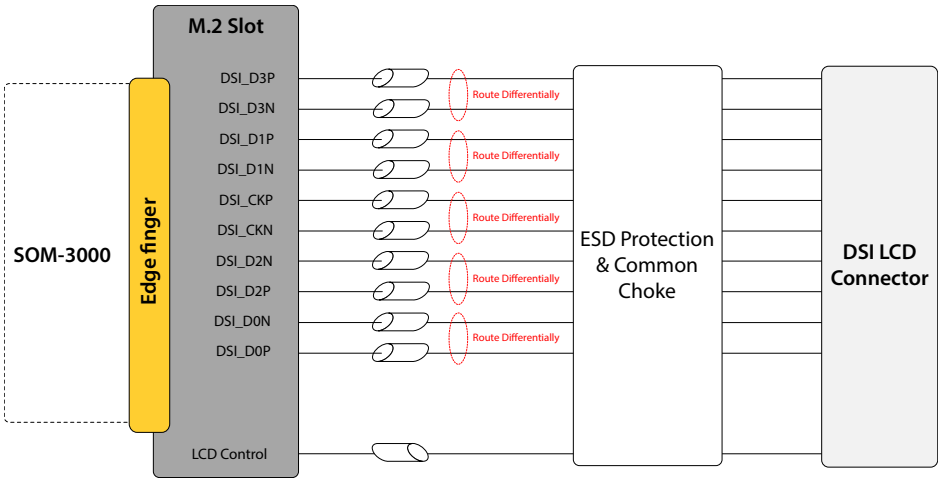


Figure 43: MIPI DSI routing topology

4.2.2 MIPI DSI Layout & Routing Recommendations

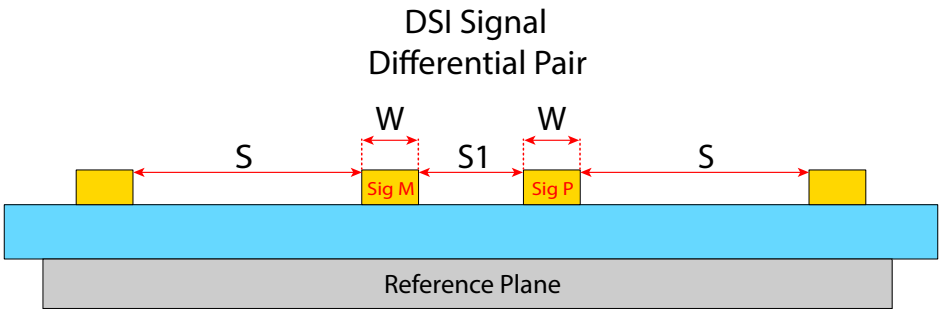


Figure 44: MIPI DSI differential trace width and spacing example

Metrics			Information/Design Guidance
General Information	Data rate		DSI – 2.1Gbit/s per lane
Impedance	Differential	Main route	100Ω ± 3%
		Connector	100Ω ± 10%
	Single-ended	Main route	50Ω ± 20%
		Connector	50Ω ± 30%
Length match (including SOM-3000)	Differential pair trace mismatch		<5mil
	Pair to pair trace mismatch		<27mil
	Data-to-clock slew		<55mil
	Maximum trace length		6000 mil
Spacing	Spacing to all other signals		4 x line width
	Spacing data lane-to-lane		3 x line width

Table 11: MIPI DSI layout guidelines

The carrier board MIPI DSI trace length and mismatch calculations should take into account the MIPI DSI Bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
DSI_D2P	1504.27	6000	-0.55	6.75	252.61	0.14	1	Inter-pair
DSI_D2N	1504.82				252.47			
DSI_D2P			-9.52	23.8		0.35	5	Pair-to-Pair
DSI_D2N			-10.53			-0.07		
DSI_D0P	1536.50	6000	4.44	6.75	253.71	0.20	1	Inter-pair
DSI_D0N	1532.06							
DSI_D0P			22.70	23.8		1.45	5	Pair-to-Pair
DSI_D0N			16.71			0.97		
DSI_CKP	1513.79	6000	-1.55	6.75	252.26	-0.28	1	Inter-pair
DSI_CKN	1515.35				252.54			
DSI_D1P	1530.18	6000	-2.59	6.75	253.24	-0.23	1	Inter-pair
DSI_D1N	1532.77				253.47			
DSI_D1P			16.38	23.8		0.97	5	Pair-to-Pair
DSI_D1N			17.42			0.92		

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
DSI_D3P	1530.94	6000	5.46	6.75	253.08	0.46	1	Inter-pair
DSI_D3N	1525.48				252.62			
DSI_D3P			17.15	23.8		0.82	5	Pair-to-Pair
DSI_D3N			-10.72	29.74		-1.55		

Table 12: SOM-3000 MIPI DSI trace & via delay

4.2.3 MIPI DSI Reference Schematics

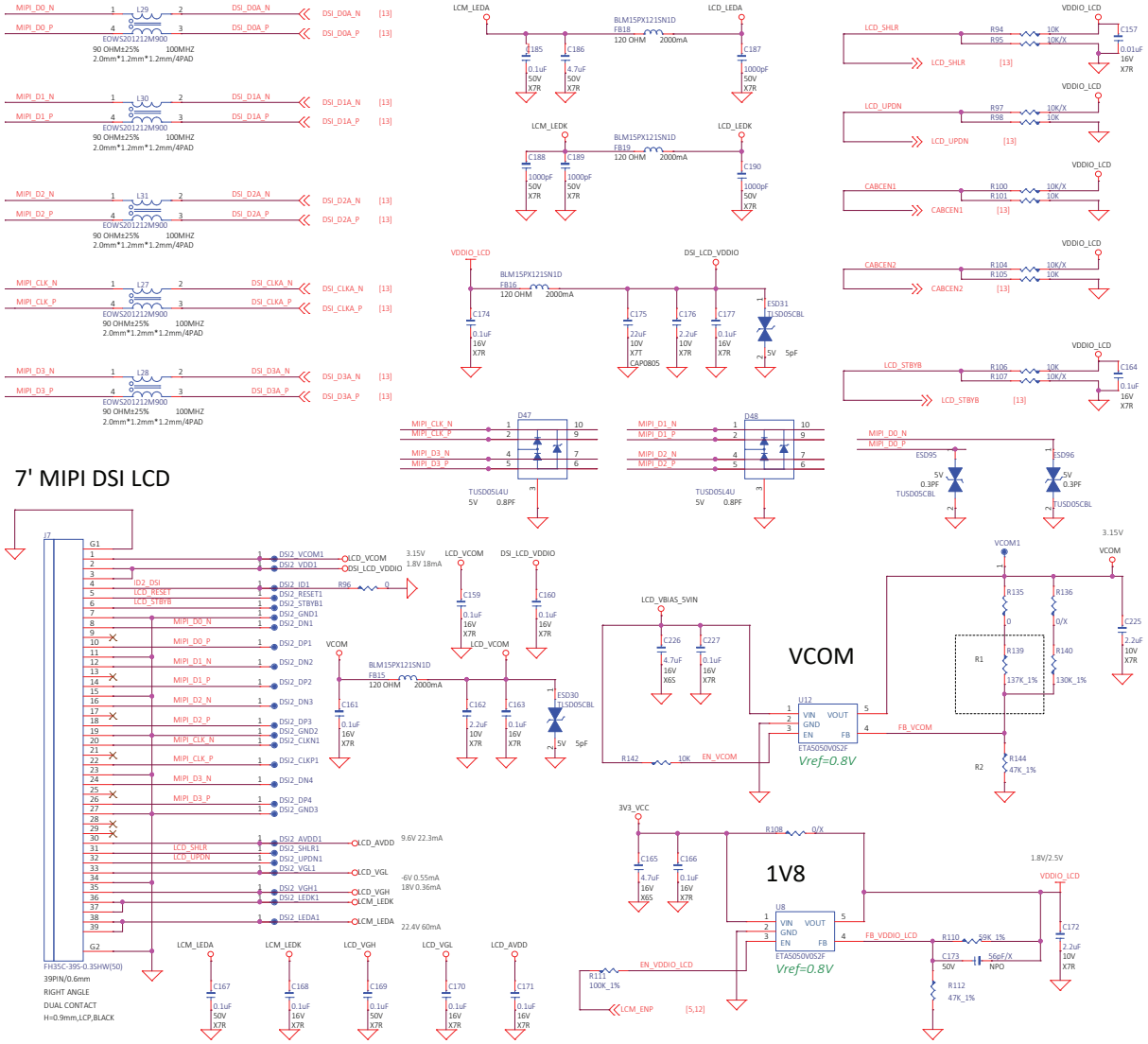


Figure 45: MIPI DSI reference circuitry

4.2.4 LCD Backlight & Bias Voltage Reference Schematics

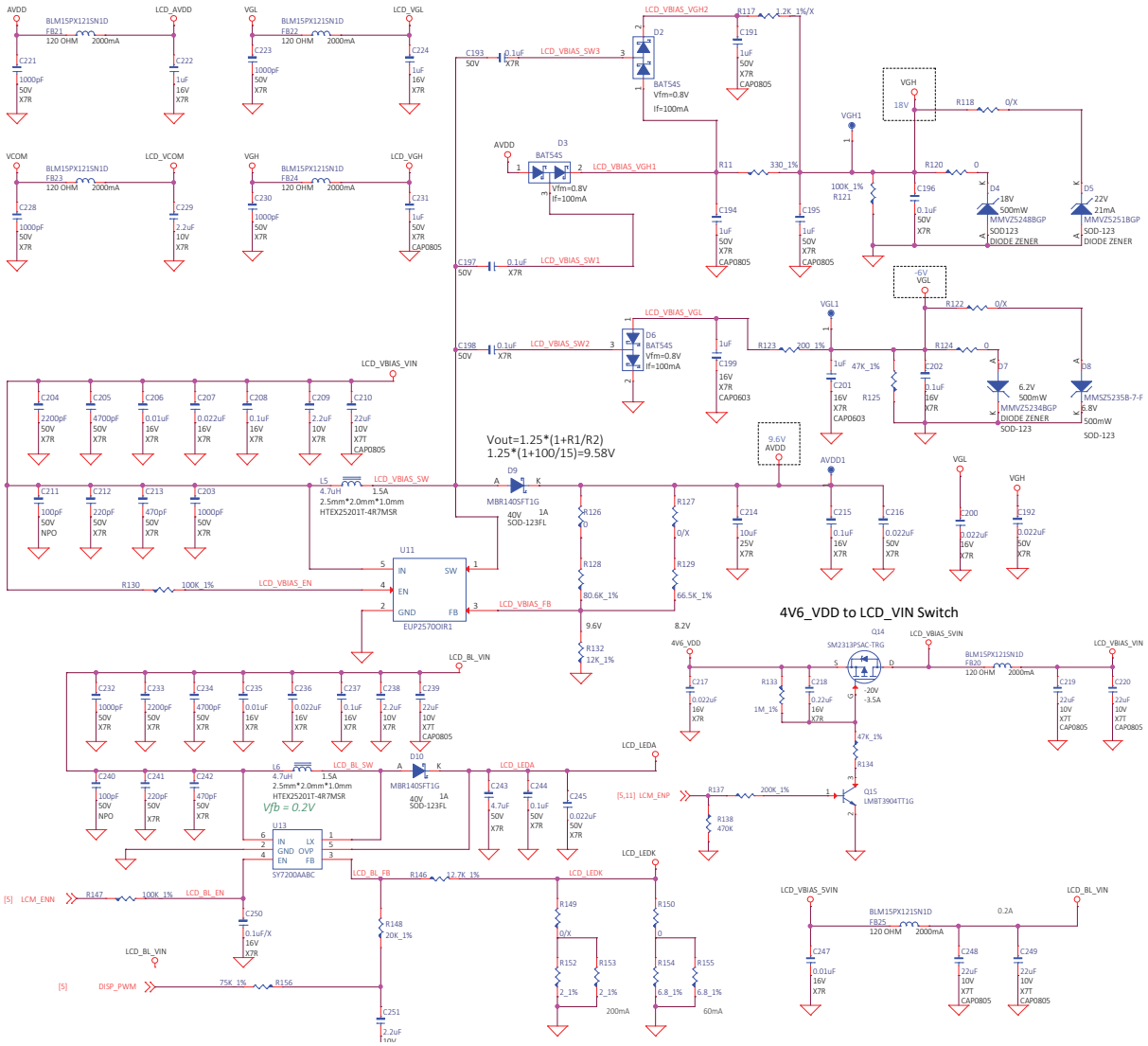


Figure 46: LCD backlight & bias voltage reference circuitry

4.3 LVDS Interface

The SOM-3000 module features an LVDS interface. The LVDS interface has four differential pair signals that carry video display signals.

4.3.1 LVDS Signal Definition

The following table provides the definition of the LVDS signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
LVDS_TX_D3P	J1.34			AO	LVDS display serial interface lane 3 –positive
LVDS_TX_D3N	J1.36			AO	LVDS display serial interface lane 3 –negative
LVDS_TX_CKP	J1.38			AO	LVDS display serial interface clock – positive
LVDS_TX_CKN	J1.40			AO	LVDS display serial interface clock – negative

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
LVDS_TX_D2P	J1.44			AO	LVDS display serial interface lane 2 – positive
LVDS_TX_D2N	J1.46			AO	LVDS display serial interface lane 2 – negative
LVDS_TX_D0N	J1.50			AO	LVDS display serial interface lane 0 – negative
LVDS_TX_D0P	J1.52			AO	LVDS display serial interface lane 0 – positive
LVDS_TX_D1N	J1.54			AO	LVDS display serial interface lane 1 – negative
LVDS_TX_D1P	J1.56			AO	LVDS display serial interface lane 1 – positive
DISP_PWM	J1.74	DISP_PWM	1.8V	I, PD	DISP_PWM,LCM Brightness PWM output
LCM_RST	J1.72	LCM_RST	1.8V	I, PD	LCD Reset output, High active
LCM_ENP	J1.70	GPIO116	1.8V	I, PD	LCM power enable output, High active
LCM_ENN	J1.68	GPIO127	1.8V	I, PD	LCM AVDD enable Output, High active

Table 13: LVDS signal definition

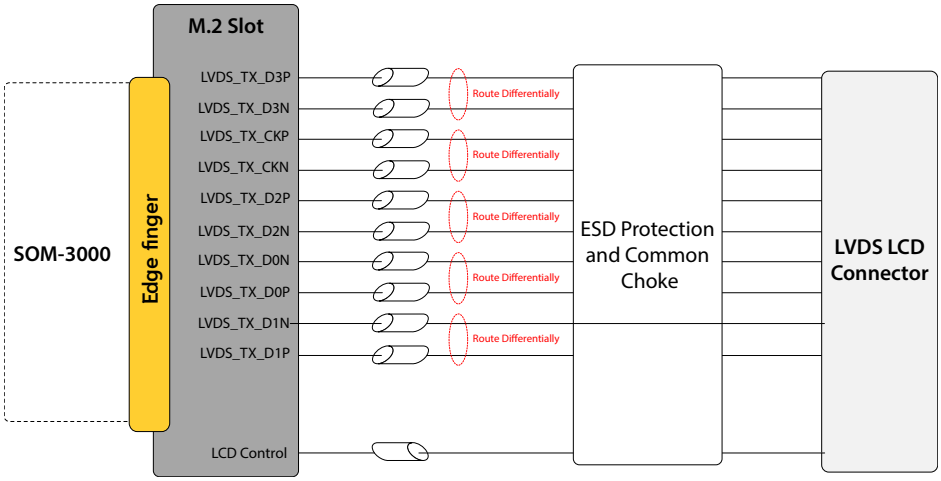


Figure 47: LVDS routing topology

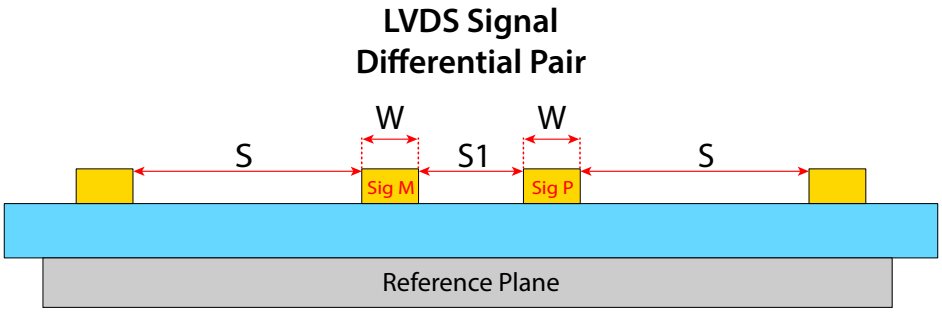


Figure 48: LVDS differential trace width and spacing example

Metrics			Information/Design Guidance
General Information	Data rate		LVDS – 2.1Gbit/s per lane
Impedance	Differential	Main route	100Ω ± 3%
		Connector	100Ω ± 10%
	Single-ended	Main route	50Ω ± 20%
		Connector	50Ω ± 30%

Metrics		Information/Design Guidance
Length match	Differential pair trace mismatch	<5mil
	Pair to pair trace mismatch	<27mil
	Data-to-clock slew	<55mil
	Maximum trace length	4000 mil
Spacing	Spacing to all other signals	4 x line width
	Spacing data lane-to-lane	3 x line width

Table 14: LVDS layout guidelines

The carrier board LVDS trace length and mismatch calculations should take into account the SOM-3000 module LVDS bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
LVDS_TX_D0P	1504.27	4000	-0.55	6.75	252.61	0.14	1	Inter-pair
LVDS_TX_D0N	1504.82				252.47			
LVDS_TX_D0P			-25.91	29.74		-0.63	5	Pair-to-Pair
LVDS_TX_D0N			-27.95			-1.00		
LVDS_TX_D1P	1536.50	4000	4.44	6.75	253.71	0.20	1	Inter-pair
LVDS_TX_D1N	1532.06				253.51			
LVDS_TX_D1P			6.32	29.74		0.47	5	Pair-to-Pair
LVDS_TX_D1N			-0.71			0.04		
LVDS_TX_CKP	1530.18	4000	-2.59	6.75	253.24	-0.23	1	Inter-pair
LVDS_TX_CKN	1532.77				253.47			
LVDS_TX_D2P	1513.79	4000	-1.55	6.75	252.26	-0.28	1	Inter-pair
LVDS_TX_D2N	1515.35				252.54			
LVDS_TX_D2P			-16.38	29.74		-0.97	5	Pair-to-Pair
LVDS_TX_D2N			-17.42			-0.92		
LVDS_TX_D3P	1530.94	4000	5.46	6.75	253.08	0.46	1	Inter-pair
LVDS_TX_D3N	1525.48				252.62			
LVDS_TX_D3P			0.76	29.74		-0.15	5	Pair-to-Pair
LVDS_TX_D3N			-7.29			-0.85		

Table 15: SOM-3000 LVDS trace & via delay

4.3.2 LVDS Reference Schematics

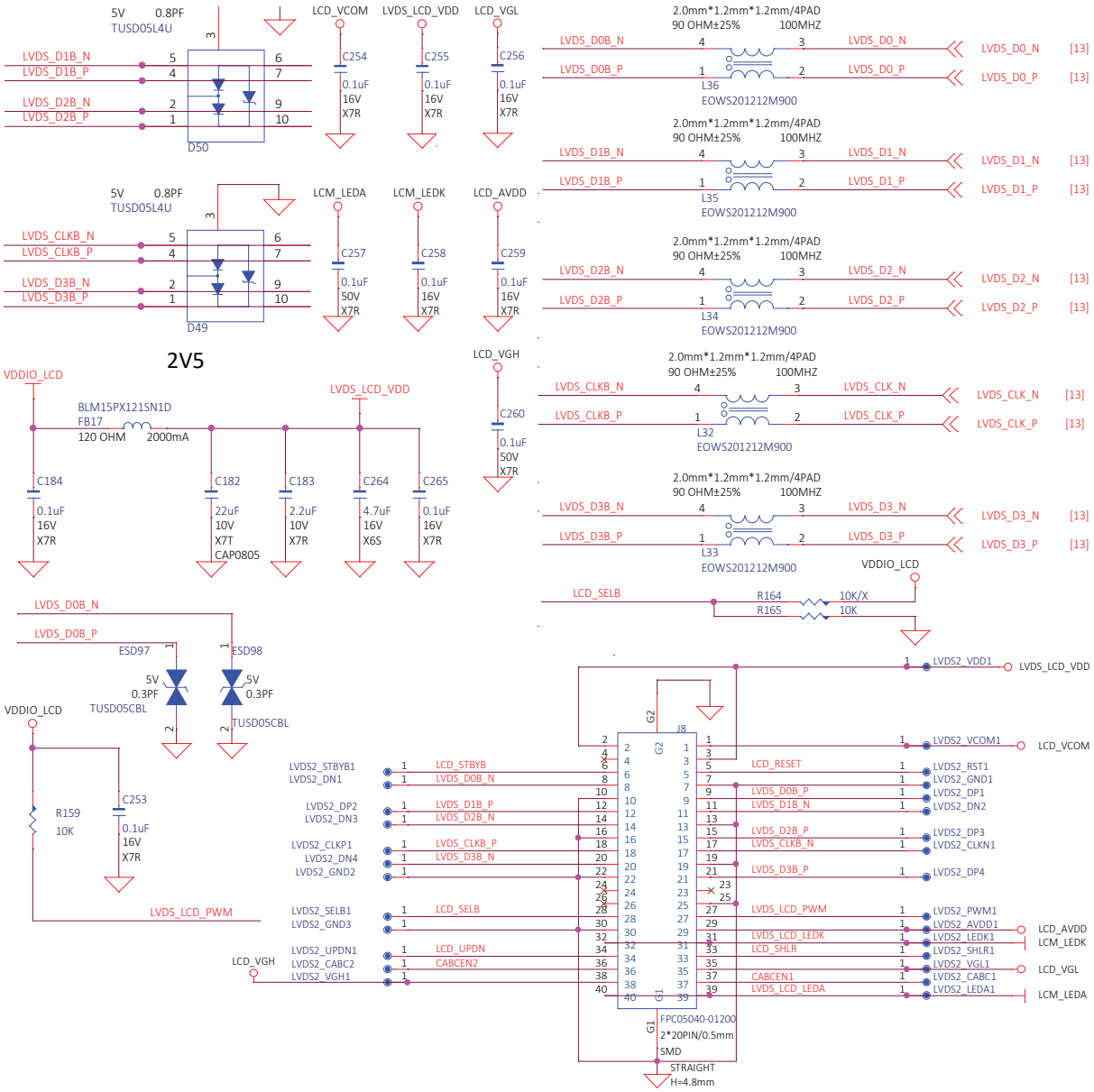


Figure 49: LVDS reference circuitry

4.4 MIPI CSI Interface

The SOM-3000 module features two MIPI CSI interfaces. Each MIPI CSI has four differential pair signals that carry data signals.

4.4.1 MIPI CSI Signal Definition

The following table provides the definition of the MIPI CSI signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
CSI0B_L2N	J1.39			AI	MIPI CSI0B serial interface lane 2 – negative CSI0_RDN1_B
CSI0B_L2P	J1.41			AI	MIPI CSI0B serial interface lane 2 – positive CSI0_RDP1_B
CSI0B_L0N	J1.43			AI	MIPI CSI0B serial interface lane 0 – negative CSI0_RDN0_B CSI0_RDN1
CSI0B_L0P	J1.45			AI	MIPI CSI0B serial interface lane 0 – positive CSI0_RDP0_B CSI0_RDP1
CSI0B_L1N	J1.49			AI	MIPI CSI0B serial interface lane 1 – negative CSI0_RCN_B CSI0_RDN3
CSI0B_L1P	J1.51			AI	MIPI CSI0B serial interface lane 1 – positive CSI0_RCP_B CSI0_RDP3
CSI0A_L0N	J1.55			AI	MIPI CSI0A serial interface lane 0 – negative CSI0_RDN0_A CSI0_RDN2
CSI0A_L0P	J1.57			AI	MIPI CSI0A serial interface lane 0 – positive CSI0_RDP0_A CSI0_RDP2
CSI0A_L1N	J1.67			AI	MIPI CSI0A serial interface lane 1 – negative CSI0_RCN0_A CSI0_RDN0
CSI0A_L1P	J1.69			AI	MIPI CSI0A serial interface lane 1 – positive CSI0_RCP0_A CSI0_RDP0
CSI0A_L2N	J1.73			AI	MIPI CSI0A serial interface lane 2 – negative CSI0_RDN1_A CSI0_RCN
CSI0A_L2P	J1.75			AI	MIPI CSI0A serial interface lane 2 – positive CSI0_RDP1_A CSI0_RCP
I2C2_SCL	J1.9	I2C2_SCL	1.8V	I, PU	I2C bus2 clock
I2C2_SDA	J1.7	I2C2_SDA	1.8V	I, PU	I2C bus2 data

Table 16: MIPI CSI0 signal definition

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
CSI1B_L1N	J1.13			AI	MIPI CSI1B serial interface lane 1 – negative MIPI CSI1 4-lane D3-
CSI1B_L1P	J1.15			AI	MIPI CSI1B serial interface lane 1 – positive MIPI CSI1 4-lane D3+
CSI1B_L0N	J1.17			AI	MIPI CSI1B serial interface lane 0 – negative MIPI CSI1 4-lane D1-
CSI1B_L0P	J1.19			AI	MIPI CSI1B serial interface lane 0 – positive MIPI CSI1 4-lane D1+

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
CSI1A_L2N	J1.23			AI	MIPI CSI1A serial interface lane 2 – negative MIPI CSI1 4-lane CLK-
CSI1A_L2P	J1.25			AI	MIPI CSI1A serial interface lane 2 – positive MIPI CSI1 4-lane CLK+
CSI1A_L1N	J1.29			AI	MIPI CSI1A serial interface lane 1 – negative MIPI CSI1 4-lane D0-
CSI1A_L1P	J1.31			AI	MIPI CSI1A serial interface lane 1 – positive MIPI CSI1 4-lane D0+
CSI1A_L0N	J1.33			AI	MIPI CSI1A serial interface lane 0 – negative MIPI CSI1 4-lane D2-
CSI1A_L0P	J1.35			AI	MIPI CSI1A serial interface lane 0 – positive MIPI CSI1 4-lane D2+
I2C1_SCL	J1.24	I2C1_SCL	1.8V	I, PU	I2C bus1 clock
I2C1_SDA	J1.26	I2C1_SDA	1.8V	I, PU	I2C bus1 data

Table 17: MIPI CSI1 signal definition

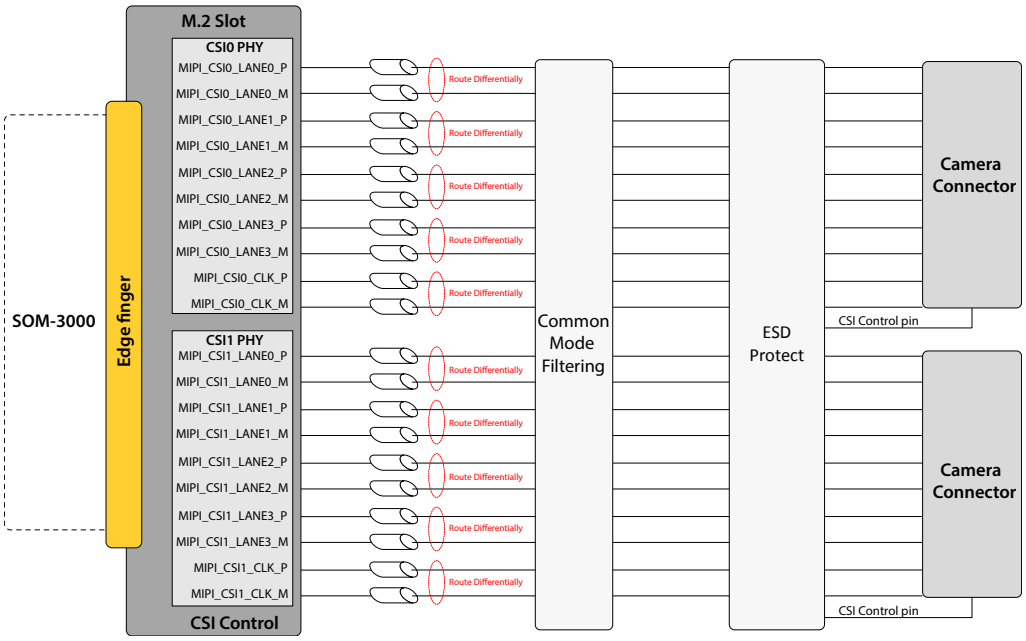


Figure 50: MIPI CSI routing topology

4.4.2 MIPI CSI Layout & Routing Recommendations

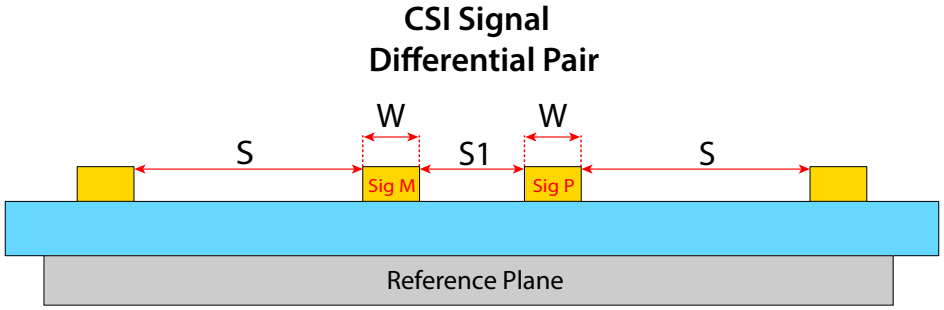


Figure 51: MIPI CSI differential trace width and spacing example

Metrics			Information/Design Guidance
General Information	Data rate		CSI – 2.1Gbit/s per lane
Impedance	Differential	Main route	100Ω ± 3%
		Connector	100Ω ± 10%
	Single-ended	Main route	50Ω ± 20%
		Connector	50Ω ± 30%
Length match (including SOM-3000)	Differential pair trace mismatch		<5mil
	Pair to pair trace mismatch		<27mil
	Data-to-clock slew		<55mil
	Maximum trace length		6000 mil
Spacing	Spacing to all other signals		4 x line width
	Spacing data lane-to-lane		3 x line width

Table 18: MIPI CSI layout guidelines

The carrier board MIPI CSI0 4-lane trace length and mismatch calculations should take into account the SOM-3000 module MIPI CSI0 4-lane bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
CSI0A_L0P	1905.844	6000	1.39	6.75	329.72	0.16	1	Inter-pair
CSI0A_L0N	1904.454				329.56			
CSI0A_L0P			9.41	29.74		-0.09	5	Pair-to-Pair
CSI0A_L0N			7.39			-0.57		
CSI0A_L1P	1905.455	6000	-0.28	6.75	330.07	-0.07	1	Inter-pair
CSI0A_L1N	1905.739				330.15			
CSI0A_L1P			9.02	29.74		0.26	5	Pair-to-Pair
CSI0A_L1N			8.68			0.02		
CSI0A_L2P	1896.432	6000	-0.63	6.75	329.81	-0.31	1	Inter-pair
CSI0A_L2N	1897.062				330.12			
CSI0B_L0P	1917.102	6000	-0.67	6.75	329.48	0.25	1	Inter-pair
CSI0B_L0N	1917.770				329.23			
CSI0B_L0P			20.67	29.74		-0.34	5	Pair-to-Pair
CSI0B_L0N			20.71			-0.89		
CSI0B_L1P	1917.858	6000	-0.24	6.75	329.59	0.30	1	Inter-pair
CSI0B_L1N	1918.094				329.28			
CSI0B_L1P			21.43	29.74		-0.22	5	Pair-to-Pair
CSI0B_L1N			21.03					

Table 19: SOM-3000 MIPI CSI0 4-lane trace & via delay

The carrier board MIPI CSI0A 2-lane trace length and mismatch calculations should take into account the SOM-3000 module MIPI CSI0A 2-lane bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
CSI0A_L0P	1905.844	6000	1.39	6.75	329.72	0.16	1	Inter-pair
CSI0A_L0N	1904.454				329.56			
CSI0A_L0P			0.39	29.74		-0.35	5	Pair-to-Pair
CSI0A_L0N			-1.28			-0.59		
CSI0A_L1P	1905.455	6000	-0.28	6.75	330.07	-0.07	1	Inter-pair
CSI0A_L1N	1905.739				330.15			
CSI0A_L2P	1896.432	6000	-0.63	6.75	329.81	-0.31	1	Inter-pair
CSI0A_L2N	1897.062				330.12			
CSI0A_L2P			-9.02	29.74		-0.26	5	Pair-to-Pair
CSI0A_L2N			-8.68			-0.02		

Table 20: SOM-3000 MIPI CSI0A 2-lane trace & via delay

The carrier board MIPI CSI0B 2-lane trace length and mismatch calculations should take into account the SOM-3000 module MIPI CSI0B 2-lane bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
CSI0B_L0P	1917.102	6000	-0.67	6.75	329.48	0.25	1	Inter-pair
CSI0B_L0N	1917.770				329.23			
CSI0B_L0P			-0.76	29.74		-0.11	5	Pair-to-Pair
CSI0B_L0N			-0.32			-0.05		
CSI0B_L1P	1917.858	6000	-0.24	6.75	329.59	0.30	1	Inter-pair
CSI0B_L1N	1918.094				329.28			
CSI0B_L2P	1927.066	6000	-0.94	6.75	329.97	-0.15	1	Inter-pair
CSI0B_L2N	1928.004				330.12			
CSI0B_L2P			9.21	29.74		0.38	5	Pair-to-Pair
CSI0B_L2N			9.91			0.83		

Table 21: SOM-3000 MIPI CSI0B 2-lane trace & via delay

The carrier board MIPI CSI1 4-lane trace length and mismatch calculations should take into account the SOM-3000 module MIPI CSI1 4-lane bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
CSI1A_L0P	2027.858	6000	-0.63	6.75	349.22	-0.56	1	Inter-pair
CSI1A_L0N	2028.492				349.78			
CSI1A_L0P			6.07	29.74		-0.21	5	Pair-to-Pair
CSI1A_L0N			8.17			0.14		

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
CSI1A_L1P	2035.249	6000	-0.89	6.75	350.27	-0.66	1	Inter-pair
CSI1A_L1N	2036.144				350.93			
CSI1A_L1P			13.46	29.74		0.84	5	Pair-to-Pair
CSI1A_L1N			15.82			1.29		
CSI1A_L2P	2021.790	6000	1.46	6.75	349.43	-0.21	1	Inter-pair
CSI1A_L2N	2020.327				349.64			
CSI1B_L0P	2051.357	6000	10.09	6.75	350.14	0.82	1	Inter-pair
CSI1B_L0N	2041.270				349.31			
CSI1B_L0P			29.57	29.74		0.71	5	Pair-to-Pair
CSI1B_L0N			20.94			-0.32		
CSI1B_L1P	2041.354	6000	4.19	6.75	349.42	0.25	1	Inter-pair
CSI1B_L1N	2037.164				349.17			
CSI1B_L1P			19.56	29.74		-0.01	5	Pair-to-Pair
CSI1B_L1N			16.84			-0.47		

Table 22: SOM-3000 MIPI CSI1 4-lane trace & via delay

4.4.3 MIPI CSI Reference Schematics

The carrier board must use a 24MHz Oscillator to generate the main clock to the camera module. The oscillator's power should be supplied by the VDDIO of the camera.

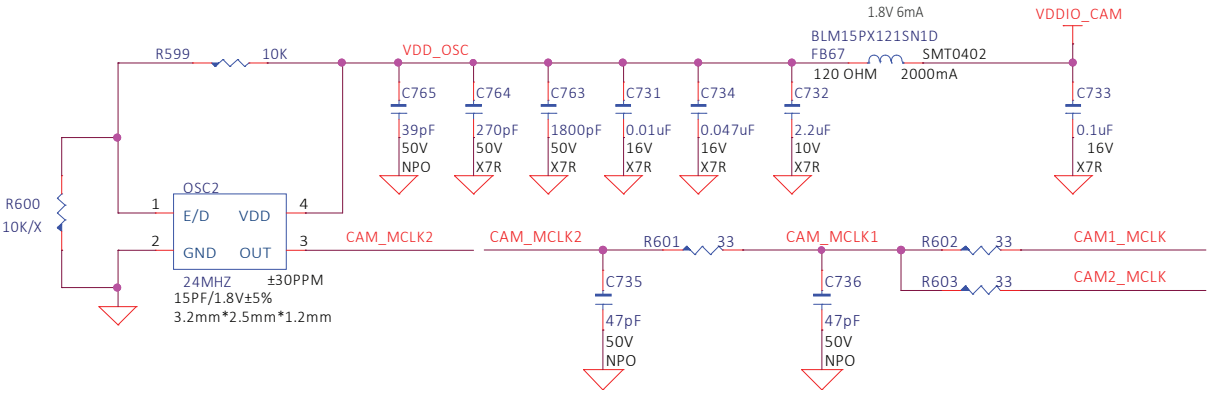


Figure 52: Camera main clock oscillator reference circuitry

In order to prevent power leakage while the system is in suspend, a level shift circuit should be added to the I2C bus of the camera.

Note:
The N Channel MOS FET should be a fast-switching type, the Vgs (th) gate-source threshold voltage should be less than 1.65V.

I2C2 Bus Level Shift

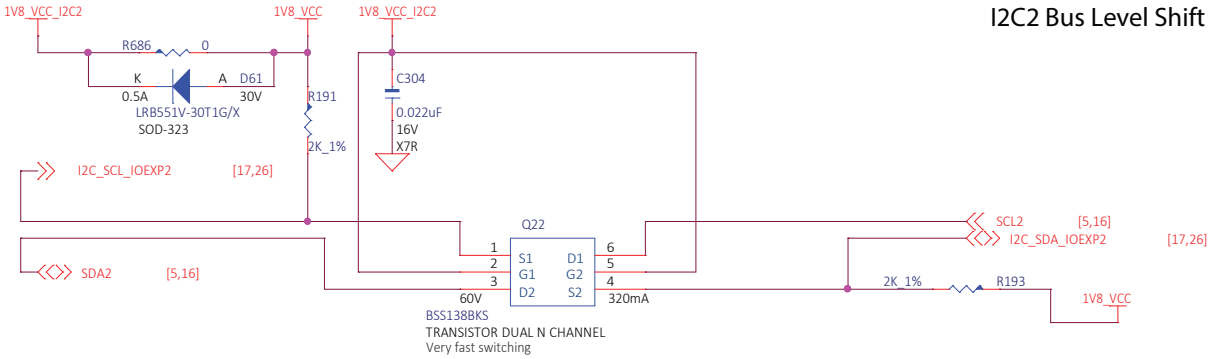


Figure 53: Camera I2C Bus level shift reference circuitry

The front and rear cameras must use independent reset and power down pins. It is recommended to use an I/O on the expander to control the cameras as there are only 6 GPIOs assigned on the SOM-3000 module's golden finger. Ensure that the I/O on the expander is the same as the cameras' I/O level.

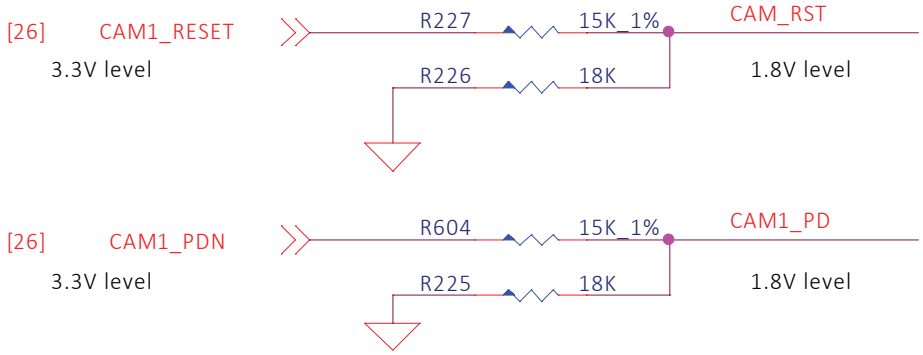


Figure 54: Camera control pin level shift reference circuitry

Use a GPIO to control the cameras' power supply to reduce the power consumption if the cameras are turned on/off by a user. It is recommended to use I/O on the expander to control the cameras' because there are only 6 GPIOs assigned on the SOM-3000 module's golden finger.

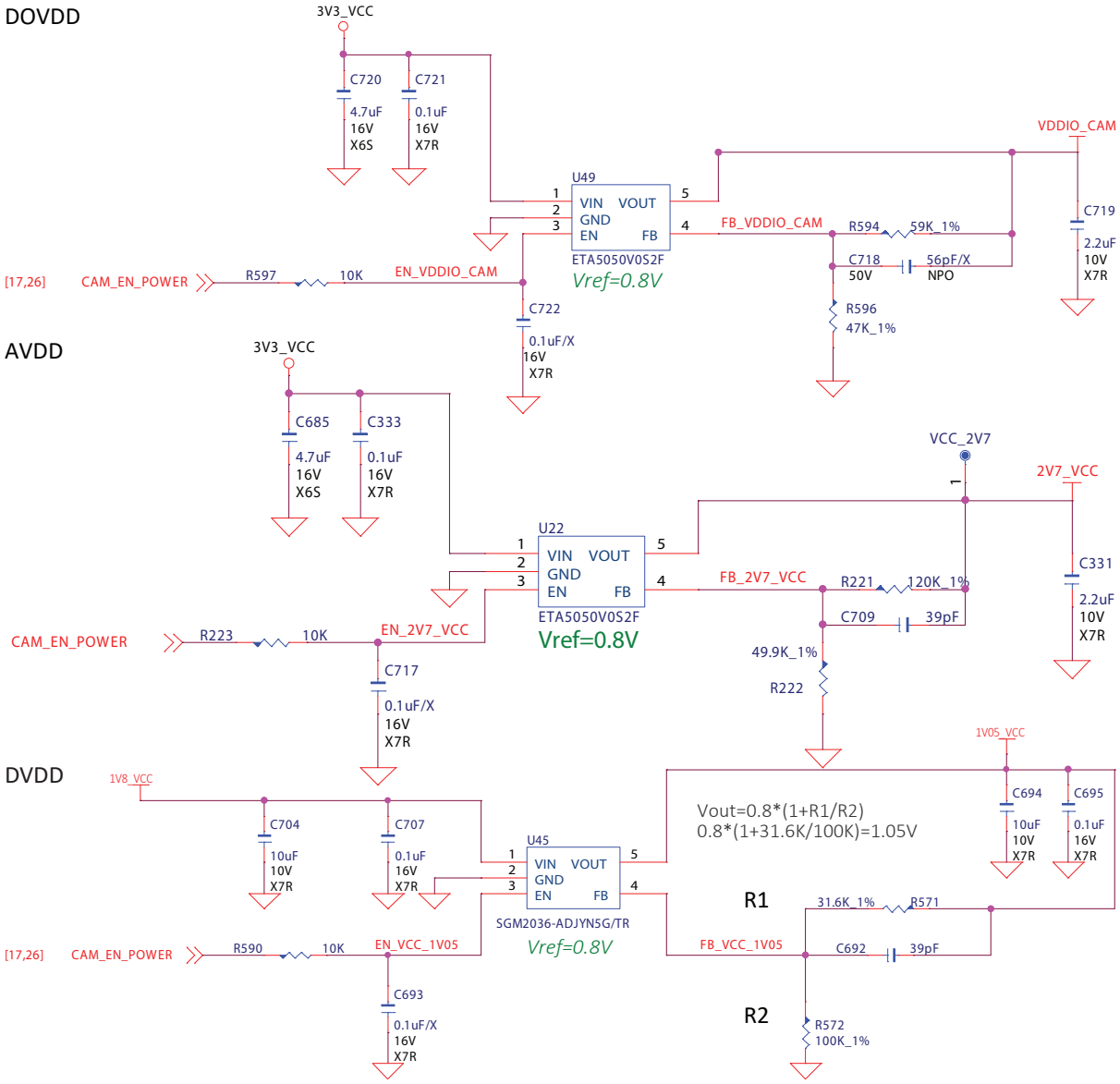


Figure 55: Camera power control reference circuitry

To 1st IMX135 Camera Module

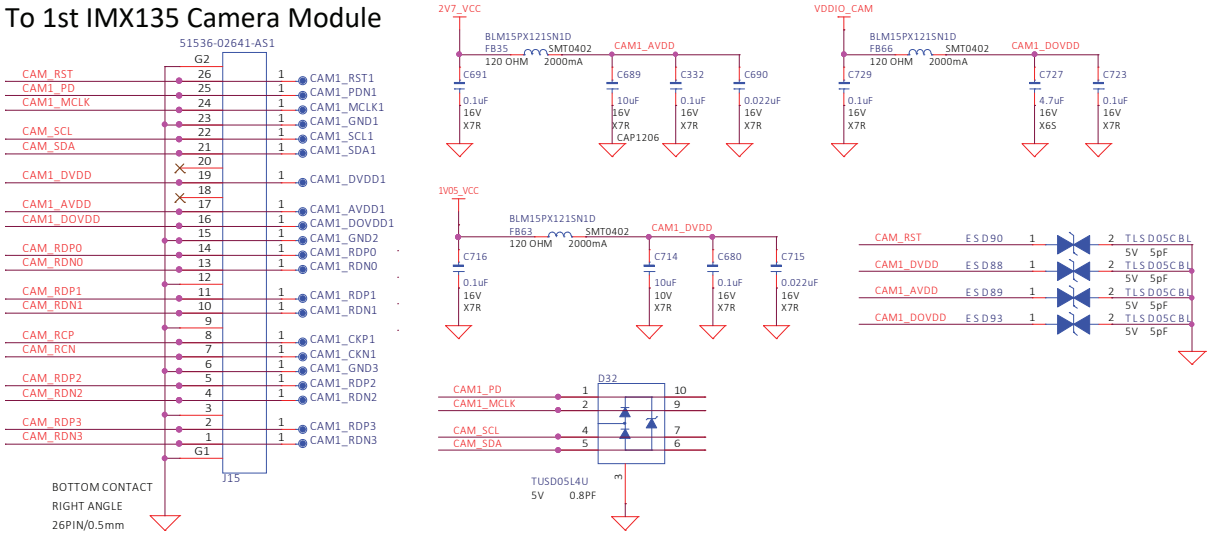


Figure 56: MIPI 4-lane camera reference circuitry (Part 1)

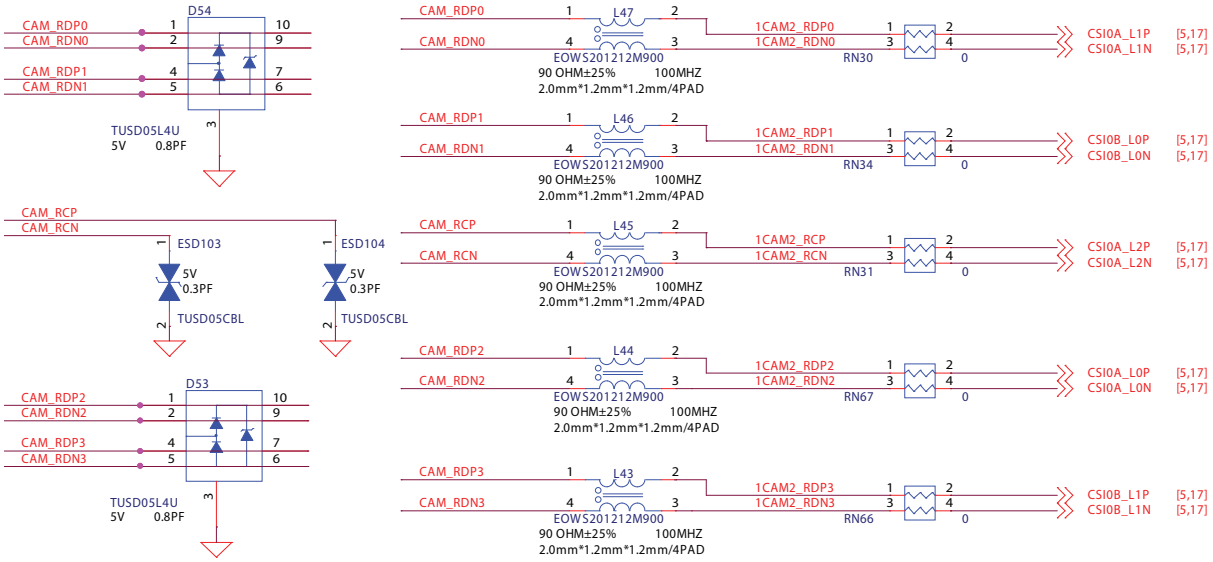


Figure 57: MIPI 4-lane camera reference circuitry (Part 2)

4.5 USB Interface

The SOM-3000 module features two USB interfaces (USB 2.0 Host and USB 2.0 OTG). The USB Port1 interface can only be used as a host while the USB Port0 interface can be configured as either a host or client.

4.5.1 USB Signal Definition

The following table provides the definition of the USB signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
USB_P1_DM	J2.1			AI, AO	USB1 Host high-speed data –minus
USB_P1_DP	J2.3			AI, AO	USB1 Host high-speed data - plus
USB_P0_DM	J2.7			AI, AO	USB0 OTG high-speed data –minus
USB_P0_DP	J2.9			AI, AO	USB0 OTG high-speed data - plus
USBOTG_VBUS	J2.13		5V	Power	USB0 OTG VBUS Power for detect
USBOTG_ID	J2.15	IDDIG	1.8V	I, PD	USB0 OTG ID input, High: device, Low: Host
USBOTG_ DRVVBUS	J2.17	USBOTG_ DRVVBUS	1.8V	I, PD	USB0 OTG DRVVBUS output, High active

Table 23: USB signal definition

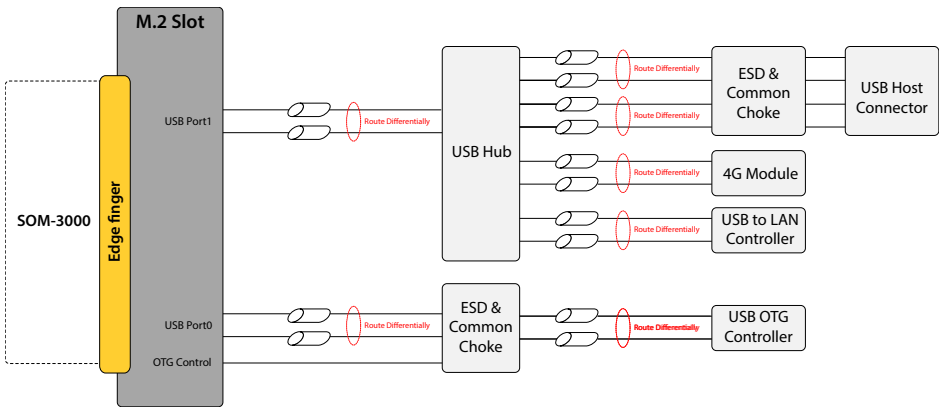


Figure 58: USB routing topology

4.5.2 USB Layout & Routing Recommendations

TVS components need to be placed as close to the USB connector and the stub on trace routing should be minimized.

It is recommended to keep a safe distance between the USB connector and high frequency EMI parts (ex. RF antenna, camera sensor) in order to minimize the side effect of interference.

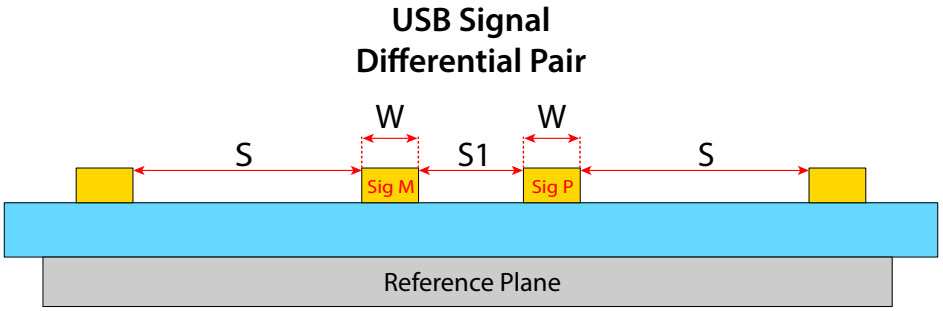


Figure 59: USB differential trace width and spacing example

Metrics			Information/Design Guidance
General Information	Data rate		USB2.0 – 480Mbit/s
Impedance	Differential	Main route	90Ω ± 3%
		Connector	90Ω ± 10%
Length match (including SOM-3000)	Differential pair trace mismatch		<5mil
	Maximum trace length		10000 mil
Spacing	Spacing to all other signals		4 x line width
	Spacing data lane-to-lane		3 x line width

Table 24: USB layout guidelines

If the USB port0 OTG function is required, connect USBOTG_VBUS pin (2.13) to VBUS.

If it is not required, connect USBOTG_VBUS to GND.

Pin#	Net Name	OTG	No OTG
J2.13	USBOTG_VBUS	VBUS	GND

Table 25: USB port0 OTG

If the USB port0 Host function is required, connect USBOTG_ID pin (J2.15) to GND.

If the USB port0 Device function is required, connect USBOTG_ID pin (J2.15) NC or floating.

Note:
System firmware download from PC by USB port0, USB port0 must be configured as Device as default. Do not pull High {USBOTG_ID pin (J2.15)} on the carrier board as it is pulled High to 1.8V on the SOM-3000 module already.

Pin#	net Name	Device (default)	Host
J2.15	USBOTG_ID	NC	GND

Table 26: USB port0 Host/Device

The carrier board USB Port0 trace length and mismatch calculations should take into account the USB Port0 from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
USB_DP_P0	1942.178	10000	0.72	6.75	335.14	-0.09	1	Inter-pair
USB_DM_P0	1941.456				335.23			

Table 27: USB Port0 trace & via delay

The carrier board USB Port1 trace length and mismatch calculations should take into account the USB Port1 from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
USB_DP_P1	2075.870	10000	2.68	6.75	358.79	-0.13	1	Inter-pair
USB_DM_P1	2073.186				358.92			

Table 28: USB Port1 trace & via delay

4.5.3 USB Reference Schematics

Micro USB

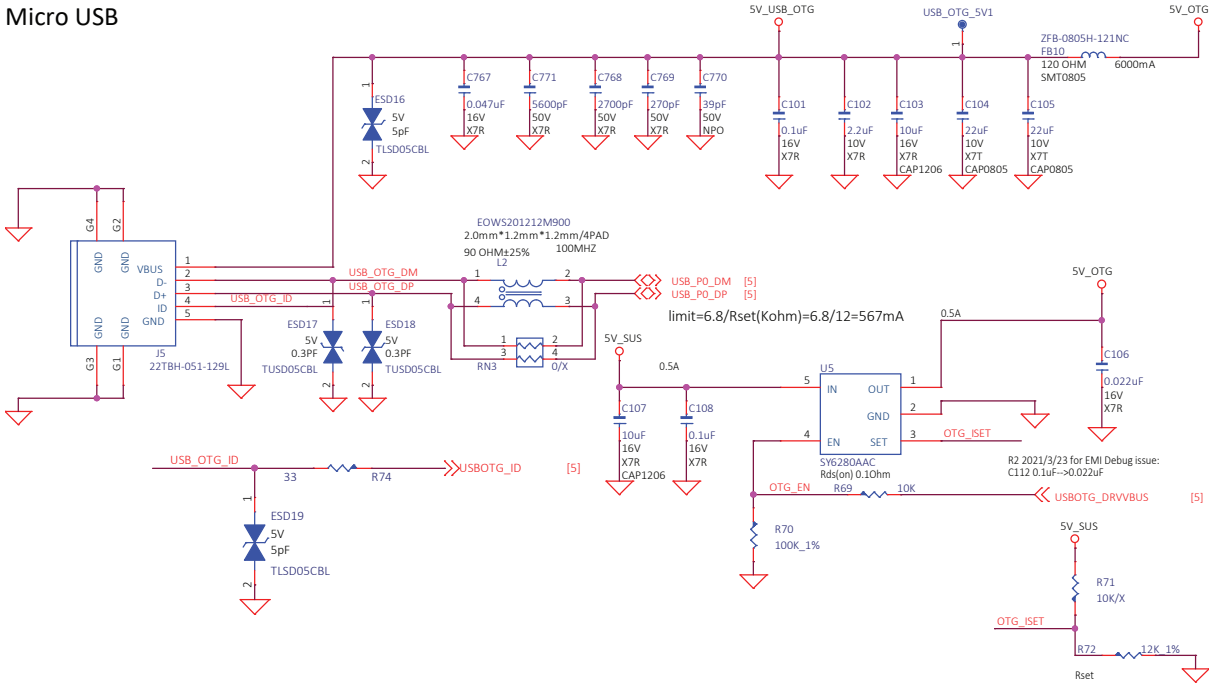


Figure 60: USB Port0 reference circuitry

USB HUB

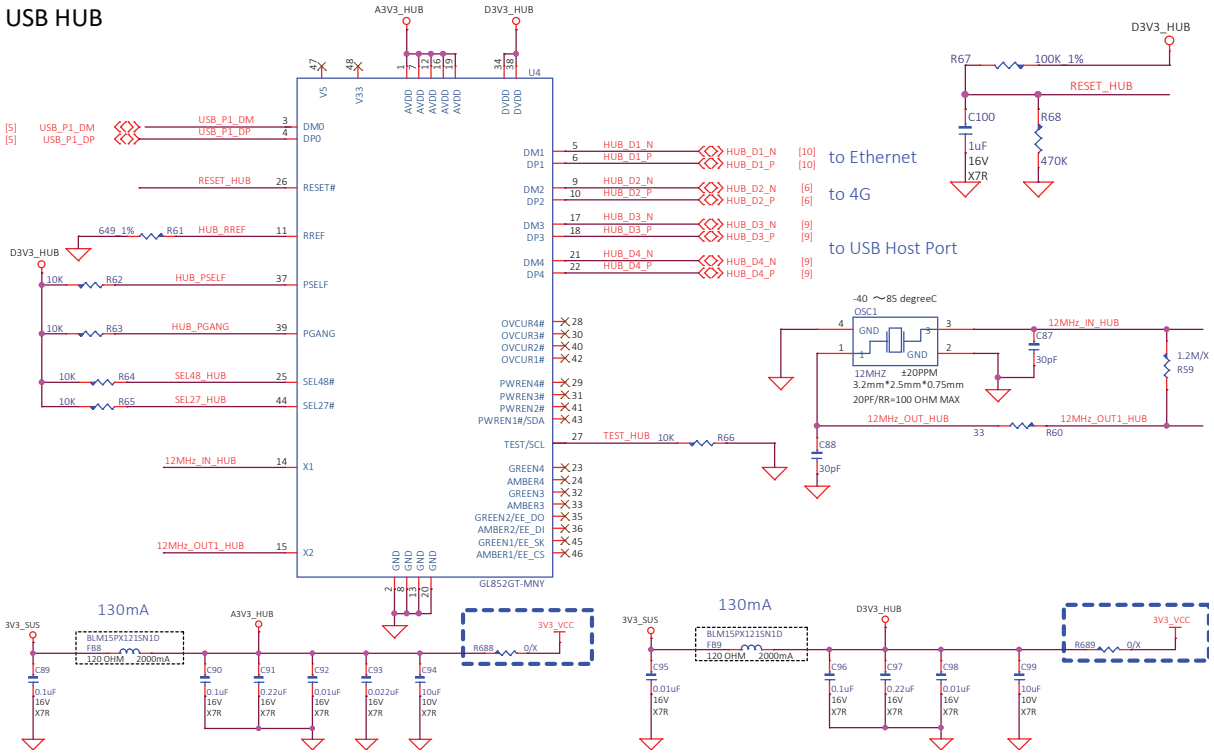


Figure 61: USB Port1 reference circuitry (Part1)

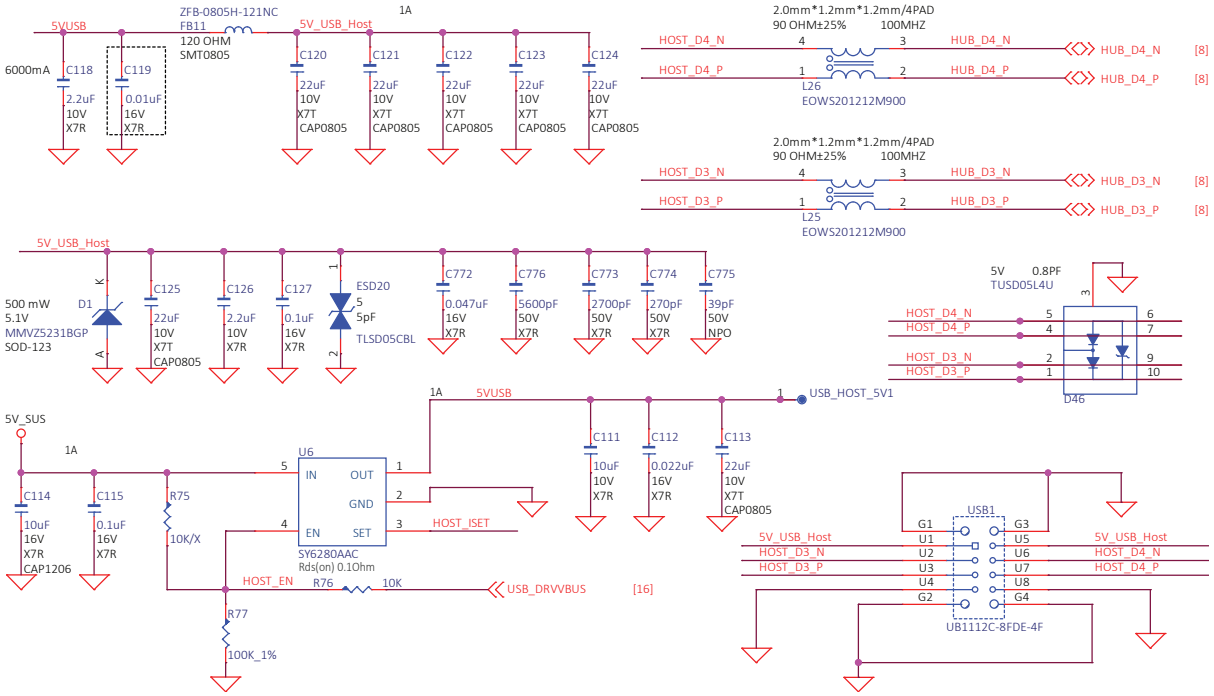


Figure 62: USB Port1 reference circuitry (Part2)

4.6 SDC Interface

The SOM-3000 module features a Secure Digital Controller (SDC) interface.

4.6.1 SDC Signal Definition

The following table provides the definition of the SDC signals that are implemented in the M.2 slot

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
MSDC1_DAT2	J1.22		3.0V	I, PU	SDIO3.0 Bus DAT2
MSDC1_DAT3	J1.20		3.0V	I, PU	SDIO3.0 Bus DAT3
MSDC1_CMD	J1.18		3.0V	I, PU	SDIO3.0 Bus Command
MSDC1_CLK	J1.16		3.0V	O, PD	SDIO3.0 Bus Clock
MSDC1_DAT0	J1.12		3.0V	I, PU	SDIO3.0 Bus DAT0
MSDC1_DAT1	J1.10		3.0V	I, PU	SDIO3.0 Bus DAT1
MSDC1_INSI	J1.8	GPIO63	1.8V	I, PU	SD Card detect input, Low active
SD_WP	J1.6	GPIO109	1.8V	I, PU	SD Card write protect input, Low active

Table 29: SDC signal definition

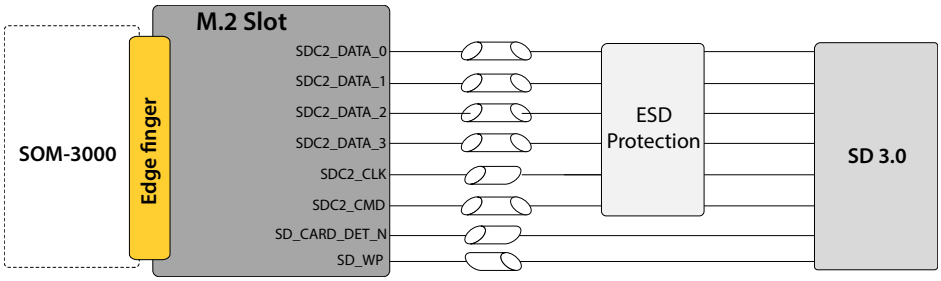


Figure 63: SDC routing topology

4.6.2 SDC Layout & Routing Recommendations

- ESD protection diode on SDIO DATA/CMD/CLK with cap value <5 pF;
- The carrier board should supply 3.0V power to the MicroSD card slot by LDO.
  - Power required for SD 2.0 SD card: 200mA
  - Power required for SD 3.0 SDR50 and DDR50 card: 400mA
  - Power required for SD 3.0 SDR104 card: 800mA and a 4.7uF cap for the power is necessary
- For EMI debugging, a second order RC filter is recommended on the SDC2_CLK (R53,R54,C82,C83)
- Do not pull the SD_WP pin (J1.6) High on the carrier board as it is already pulled High to 1.8V on the SOM-3000 module.
- The MicroSD card slot should not be occupied by default. The card detect MSDC1_INSI (J1.8) pin is pulled High when a MicroSD card is inserted, and pulled Low when a MicroSD card is removed.

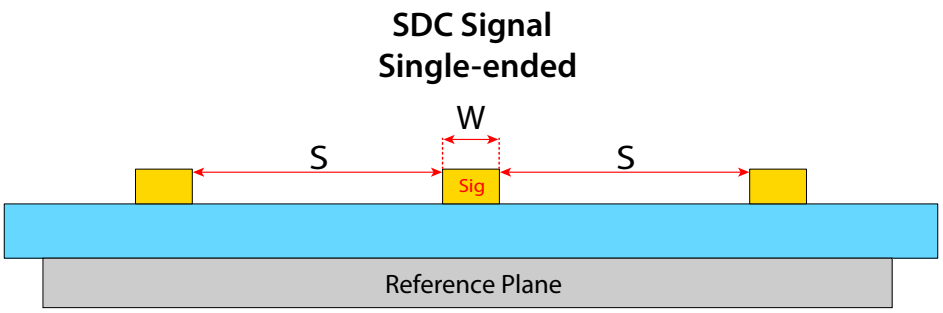


Figure 64: SDC single-ended trace width and spacing example

Metrics			Information/Design Guidance
General Information	Data rate		208MHz
Impedance	Single-end	Main route	50Ω ± 5%
		Connector	50Ω ± 20%
Length match (including SOM-3000)	Between clock and data		<27mil
	Maximum trace length		6000 mil
Spacing	Spacing to all other signals		2 x line width
	Spacing data lane-to-lane		2 x line width

Table 30: SDC layout guidelines

The carrier board SDC trace length and mismatch calculations should take into account consider the SDIO bus from the SOM-3000 module.

Net Name	Trace Length (mil)	Length Spec (mil)	Length Mismatch (mil)	Length Mismatch Spec (mil)	Total Delay (Trace + Via) (ps)	Delay Mismatch (ps)	Delay Mismatch Spec (ps)	Notes
MSDC1_CLK	2418.60	6000			404.16			
MSDC1_CMD	2363.90		-54.70	67.50	404.38	0.22	10	Refer to MSDC1_CLK
MSDC1_DAT0	2393.46		-25.14		404.08	-0.08	10	
MSDC1_DAT1	2393.93		-24.67		404.28	0.12	10	
MSDC1_DAT2	2366.33		-52.28		404.06	-0.10	10	
MSDC1_DAT3	2367.25		-51.35		404.36	0.20	10	

Table 31: SOM-3000 SDC trace & via delay

4.6.3 SDC Reference Schematics

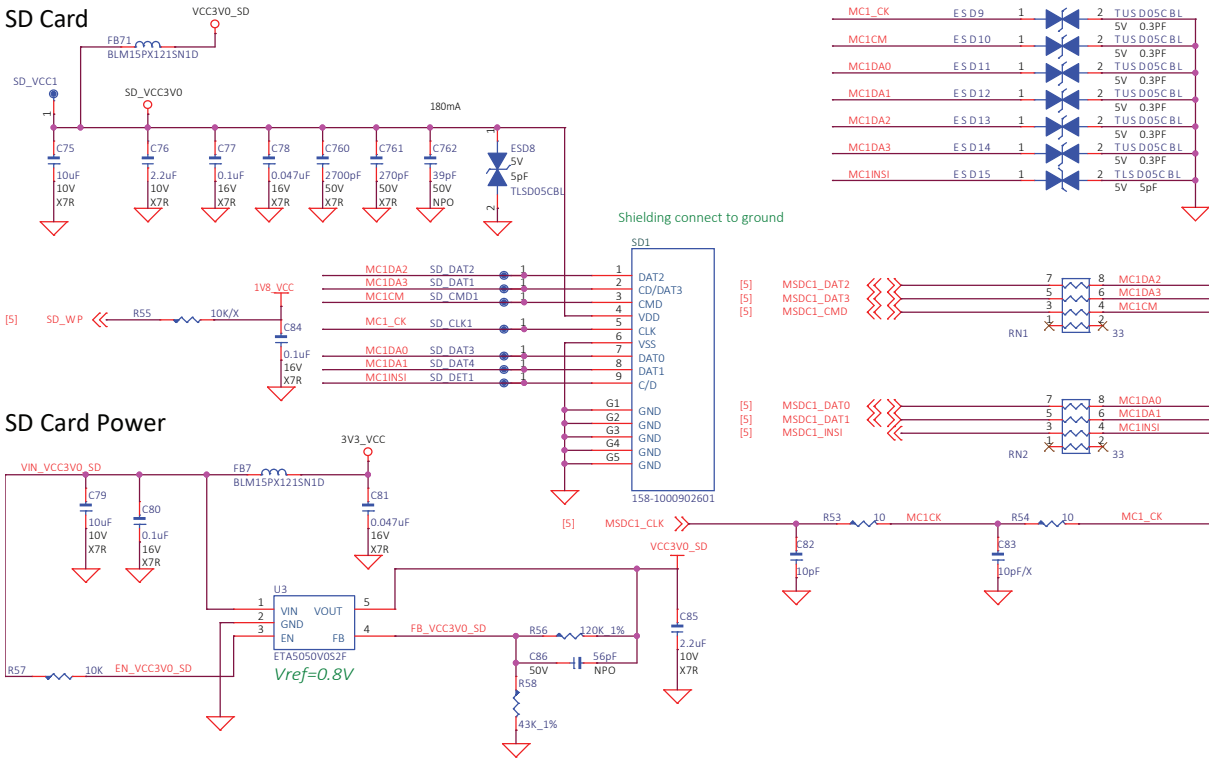


Figure 65: SDC reference circuitry

4.7 Analog Audio Interface

The SOM-3000 module features an Analog Audio interface.

4.7.1 Analog Audio Signal Definition

The following table provides the definition of the Analog Audio signals that are implemented in the M.2 slot.

Signal Name	Pin #	Pad Characteristics		Description
		Voltage	Type	
AU_VIN1_N	J2.2	2.8V	AI	Earphone MIC, Differential MIC1- input,
AU_VIN1_P	J2.4	2.8V	AI	Earphone MIC, Differential MIC1+ input, need Vbias on the carrier board
ACCDET	J2.6	2.8V	AI	Earphone MIC, ACCDET
AU_VIN0_N	J2.8	2.8V	AI	On board MIC, Differential MIC0- input,
AU_VIN0_P	J2.10	2.8V	AI	On board MIC, Differential MIC0+ input, need Vbias on the carrier board
AVSS28_AUD	J2.12		Power	Audio Analog Ground, add a 0 Ohm resistor to Ground on the carrier board
AU_HP_RIGHT	J2.14	2.8V	AO	Headphone audio right channel output
AU_HP_LEFT	J2.16	2.8V	AO	Headphone audio left channel output

Table 32: Analog audio signal definition

4.7.2 PCB Layout Requirement

- Place the Headset AU_VIN1_P/N DC block capacitor near the M.2 slot and keep the ACCDET as short as possible.
- The AU_MICBIAS should be guarded by the GND on all sides and should be kept away from high power/ RF signals.
- The AU_VIN0_P/N, AU_VIN1_P/N, SPK_LP/N, and SPK_RP/N signals should be routed in parallel and be guarded by GND on all sides and should be kept away from high power/ RF signals.
- The AU_HP_LEFT and AU_HP_RIGHT channel signals should also be guarded by GND on all sides

4.7.3 Schematics Requirement

- The ESD component should be bi-directional.
- The Serial Beads should be placed close to the Line out jack. RDC <0.3ohm and a rated current >30mA is recommended.
- An independent 3.0V LDO is required to supply MIC Vbias.

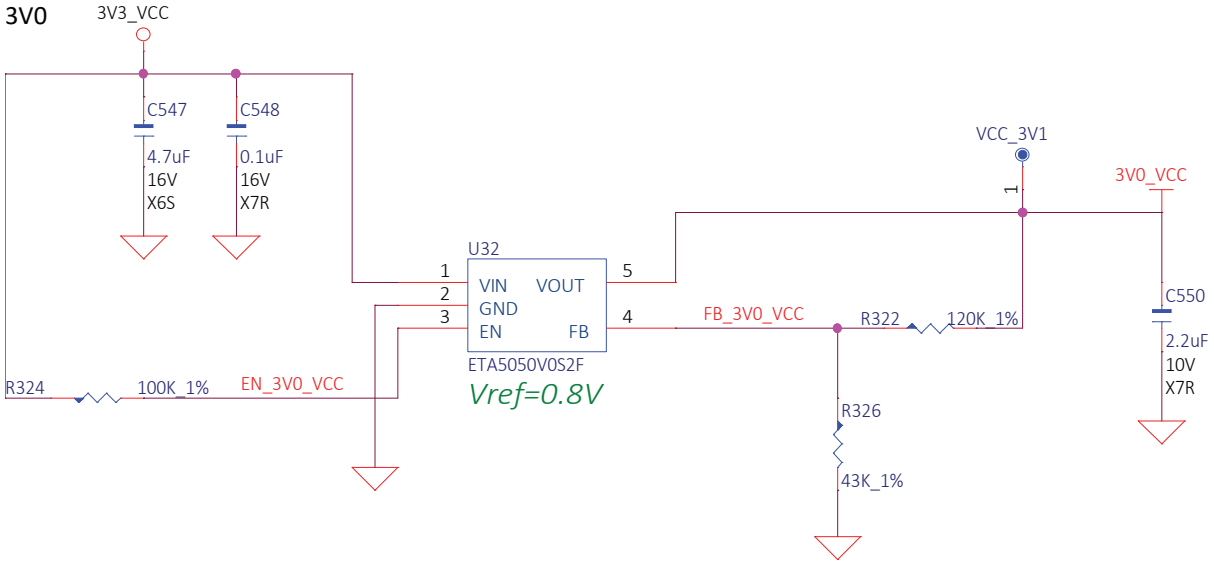


Figure 66: Audio bias voltage LDO reference circuitry

- A 3.5mm or 2.5mm Line-out jack with a switch pin should be used and empty by default. The HP_DET pin is pulled High when a headset is inserted and pulled Low when a headset is removed.
- The HP_DET pin should be pulled High. The pulled High voltage should be the same as the GPIO VDD on the I/O expander.
- A Class-D amplifier should be controlled by the I/O expander, and the enable pin should be pulled Low by default.
- A 0.1uF DC couple cap between the GND and AVSS28_AUD pins should be placed close to the Class-D amplifier and the on-board MIC.

4.7.4 Audio Analog Reference Schematics

On-Board MIC

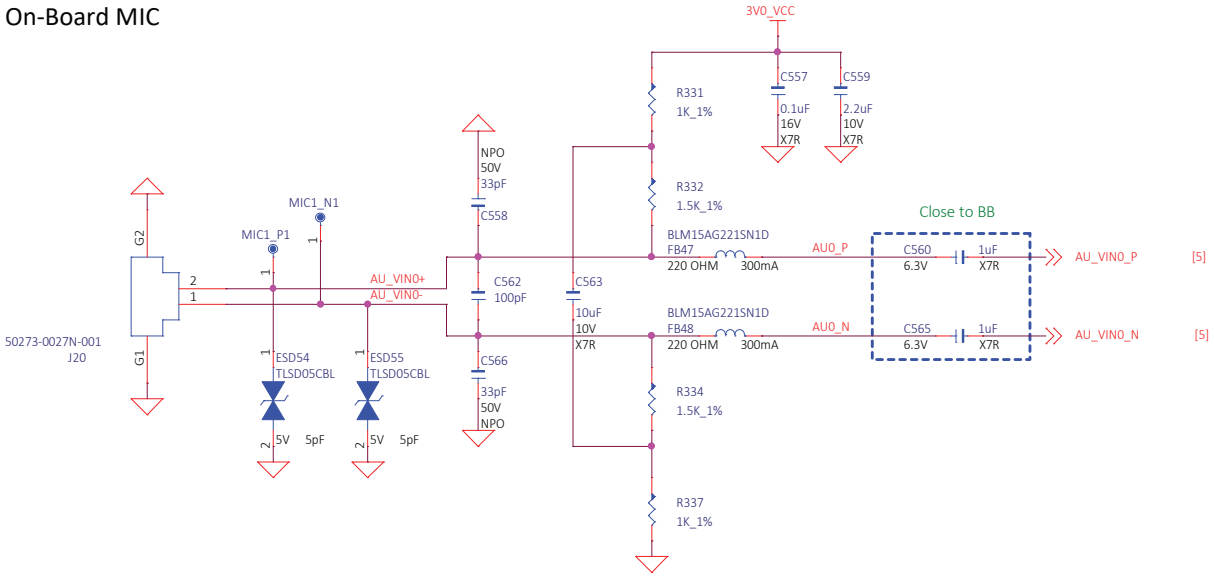
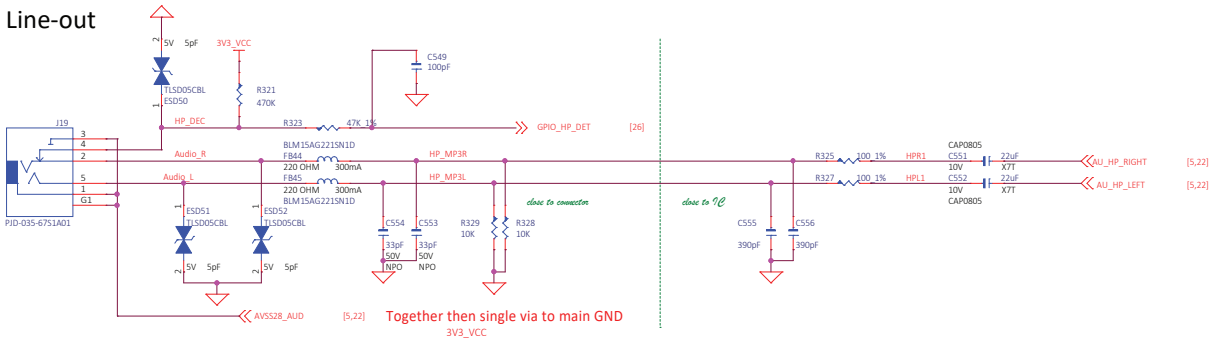


Figure 67: On-board MIC reference circuitry

Line-out



Microphone

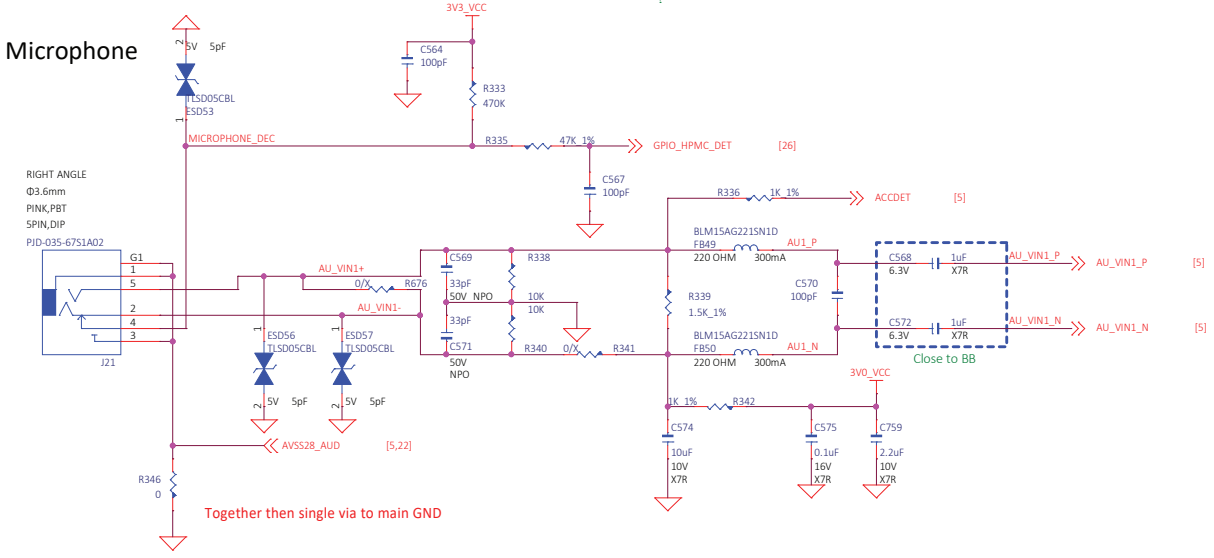


Figure 68: Line-out & MIC-in jack reference circuitry

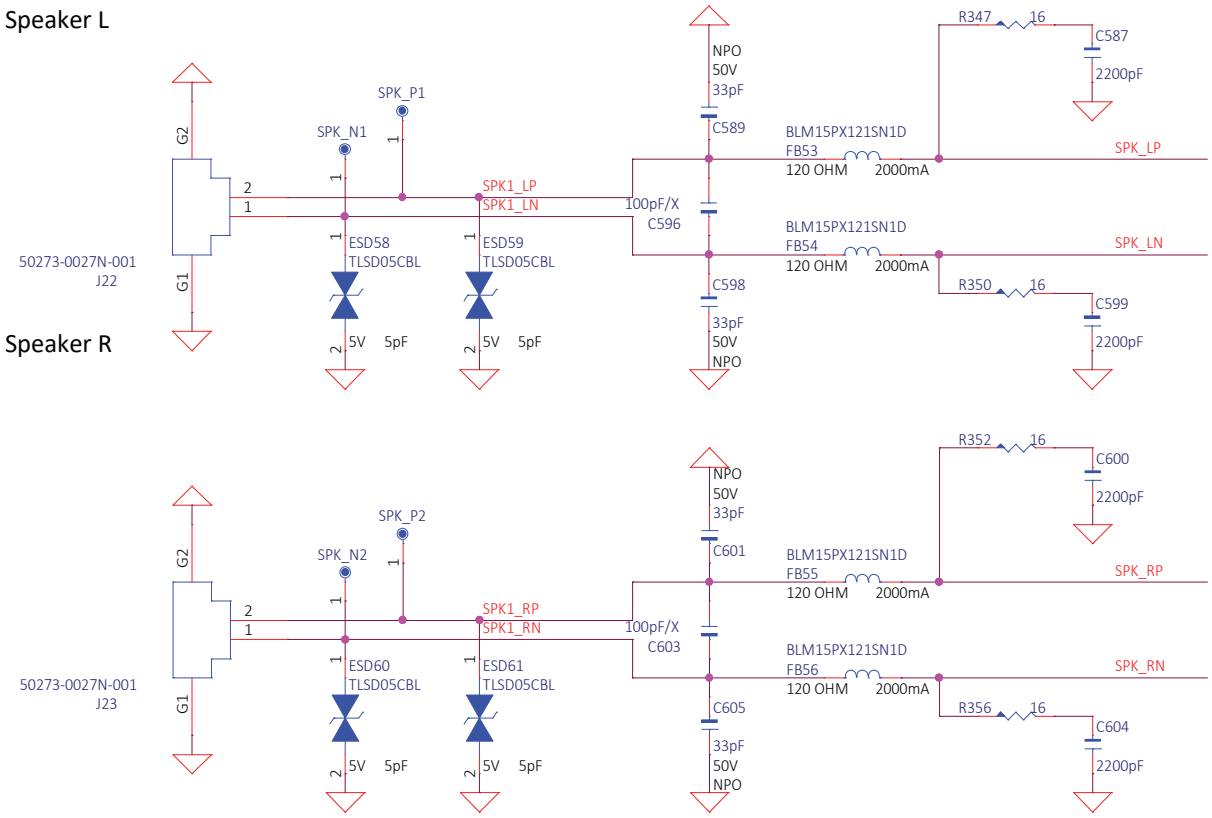


Figure 69: Speaker connector reference circuitry

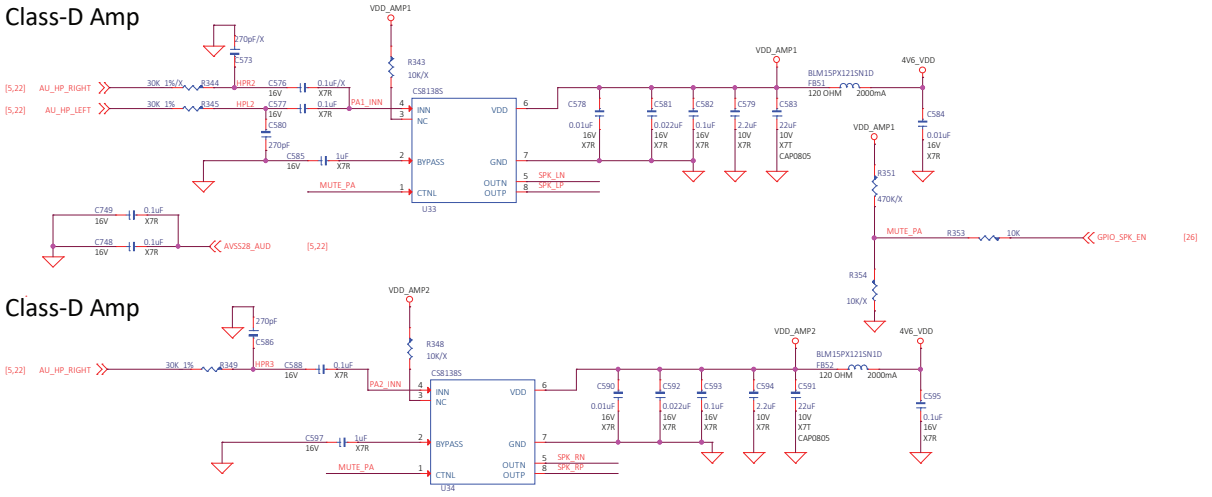


Figure 70: Class-D amplifier reference circuitry

4.8 GPIO Interface

The SOM-3000 module features a General Purpose Input/Output (GPIO) interface.

4.8.1 GPIO Signal Definition

The following table provides the definition of the GPIO signals that are implemented in the M.2 slot. All SOM-3000 GPIOs are 1.8V domain only, all device ports should be the same.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
EXT_INT3	J2.31	GPIO105	1.8V	O, PD	MT8365 EINT105, IO Extender interrupt input, Low active
EXT_INT2	J2.33	GPIO115	1.8V	I, PD	MT8365 EINT115, G-sensor interrupt input, High active
EXT_INT1	J2.35	GPIO67	1.8V	I, PD	MT8365 EINT67, Reserved
EXT_GPIO3	J2.20	GPIO130	1.8V	I, PD	MT8365 GPIO130, default for SPI_BUSY, input, High active
EXT_GPIO2	J2.22	GPIO131	1.8V	I, PD	MT8365 GPIO131, default for NFC_CARD_INT, input, High active
EXT_GPIO1	J2.24	GPIO129	1.8V	I, PD	MT8365 GPIO129, default for NFC_CARD_RESET, output, High active

Table 33: SOM-3000 GPIO signal definition

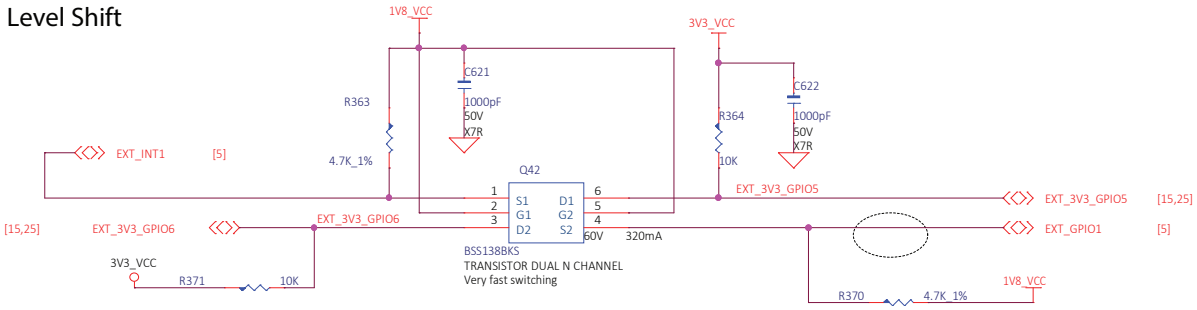


Figure 71: GPIO level shift reference circuitry

4.8.2 GPIO Extender

If the carrier board needs more GPIOs, a GPIO extender is required.

GPIO Expander

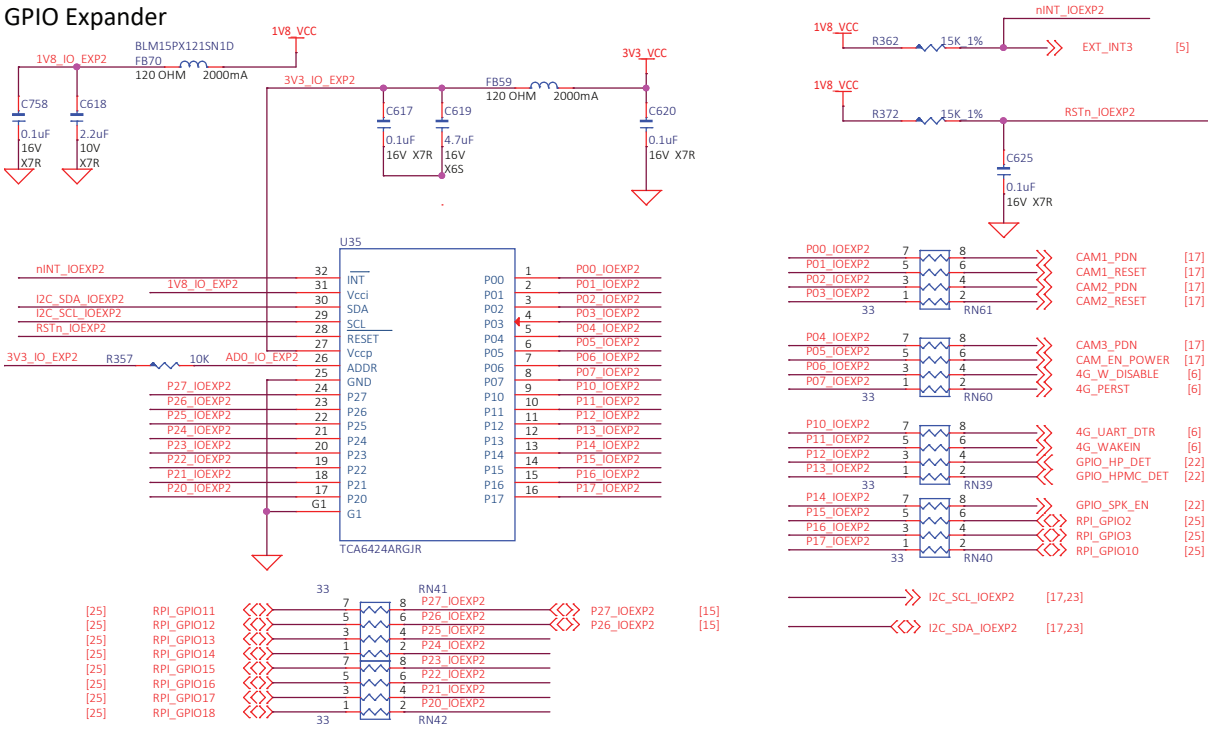


Figure 72: GPIO expander reference circuitry

4.9 ADC Interface

The SOM-3000 module features an ADC interface.

4.9.1 ADC Signal Definition

The following table provides the definition of the ADC signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
ADC_VIN0	J2.67	AUX_IN2	1.8V	AI	MT8365 AUX_IN2

Table 34: SOM-3000 ADC signal definition

4.9.2 ADC Design Notes

- Input range support max. 1.45V.
- 12-bit resolution.
- Connect the J2.67 ADC_VIN0 input pins to the GND when not used.
- In order to prevent power leakage, the AUX_IN2 input signal should not be supplied power while the system is suspended.
- Add a 0.1 uF decouple cap for all AUX_IN2 pins used. The cap should be placed close to the M.2 slot.

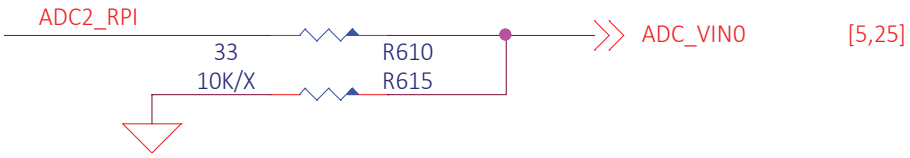


Figure 73: ADC reference circuitry

4.10 System Boot Interface

The SOM-3000 module features a System Boot interface.

4.10.1 System Boot Signal Definition

The following table provides the definition of the System Boot signals that are implemented in the M.2 slot.

Pin	Name	GPIO#	Function	Case	BOOT
J2.25	BATSNS	MT6390/ MT6357 BATSNS	Battery voltage input	3.0V≤V BATSNS≤4.25V	Yes
				V BATSNS<3.0V	No
				V BATSNS>4.25V	No
J1.2	VIN_DC	MT6390/ MT6357 VIN_DC	DC input voltage input, for DC detect	3.4V≤VIN_DC≤12V	Yes
				VIN_DC Low	No
J2.48	SYSRSTB	MT8365 System Reset	System Reset input, Low active	V SYSRSTB High	Yes
				V SYSRSTB Low	No
J2.71 J2.72 J2.75	VSYS		System Power supply	VSYS =3.4~5V	Yes
					No

Table 35: SOM-3000 system boot signal definition

4.10.2 System Boot Design Notes

- The system will auto boot when 3.4~5V power is supplied to the VSYS PIN (J2.71 J2.72 J2.75).
- If the J2.25 V BATSNS<3.0V or V BATSNS>4.25V is used, the PMU MT6390/MT6357 will judge the whether the lithium-ion battery is faulty, and the system will not boot.
- If the J1.2 VIN_DC is pulled Low, the system can't boot.
- Do not pull the SYSRSTB pin (J2.48) pin High on carrier board as it is already pulled High to 1.8V on SOM-3000 module. The system will reboot when the SYSRSTB pin (J2.48) is pulled Low.
- When the system powers off, power to the VSYS pin (J2.71 J2.72 J2.75) will be cut.
- To reduce the power consumption while the system powers off, power to the BATSNS pin (J2.25) and VIN_DC pin (J1.2) should be cut.
- It is highly recommended to use a MCU GPIO to control the power supply of the BATSNS pin (J2.25), VIN_DC pin (J1.2) and VSYS pin (J2.71 J2.72 J2.75)
- When a 2-cell 8.4V lithium-ion battery is used, a 2:1 divider and voltage following amplifier should be added to the BATSNS circuit to avoid loading effect from the internal PMU.
- The maximum power required by the SOM-3000 module during boot may reach up to 2.5W, a maximum current of 0.9A is required for each VSYS pin (J2.71 J2.72 J2.75).

4.10.3 System Boot Reference Schematics

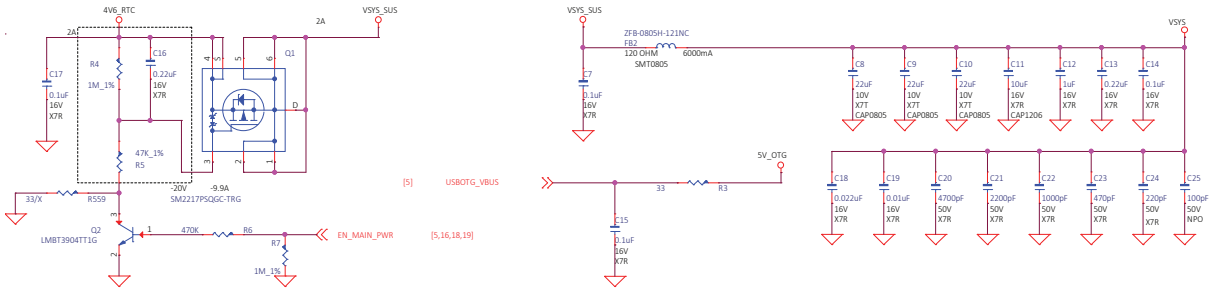


Figure 74: SOM-3000 power switch reference circuitry

2-Cell Battery Wafer

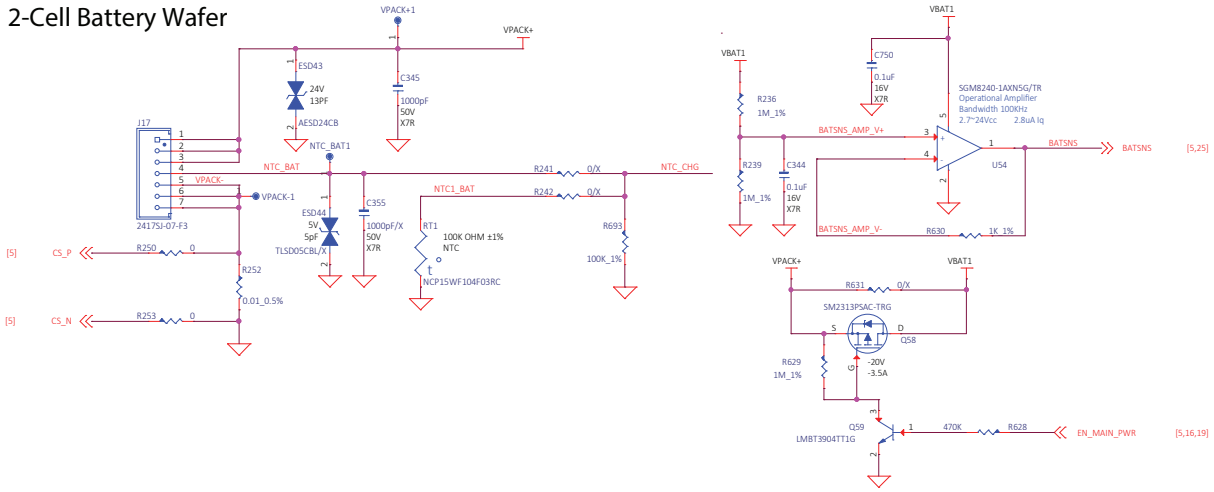


Figure 75: SOM-3000 BATSNS reference circuitry

4.11 PWM Interface

The SOM-3000 module features two PWM interface.

4.11.1 PWM Signal Definition

The following table provides the definition of the PWM signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
PWM_A	J2.58	GPIO114	1.8V	I, PD	PWM_A output, connect to 1st motor PWM
PWM_C	J2.68	GPIO21	1.8V	I, PD	PWM_C output, connect to 2nd motor PWM

Table 36: SOM-3000 PWM signal definition

4.11.2 PWM Design Notes

- PWM output frequency range: 0.04 Hz~ 39MHz.
- PWM output duty: 0~100%.
- PWM I/O level: 1.8V default, a level shift circuit should be added if higher voltage is required (ex. 3.3V).

Note:
An N Channel MOS FET should be a fast-switching type, the Vgs(th) gate-source threshold voltage should be less than 1.65V. In order to prevent power leakage, the PWM output signal should be set to Low when the system is suspended.

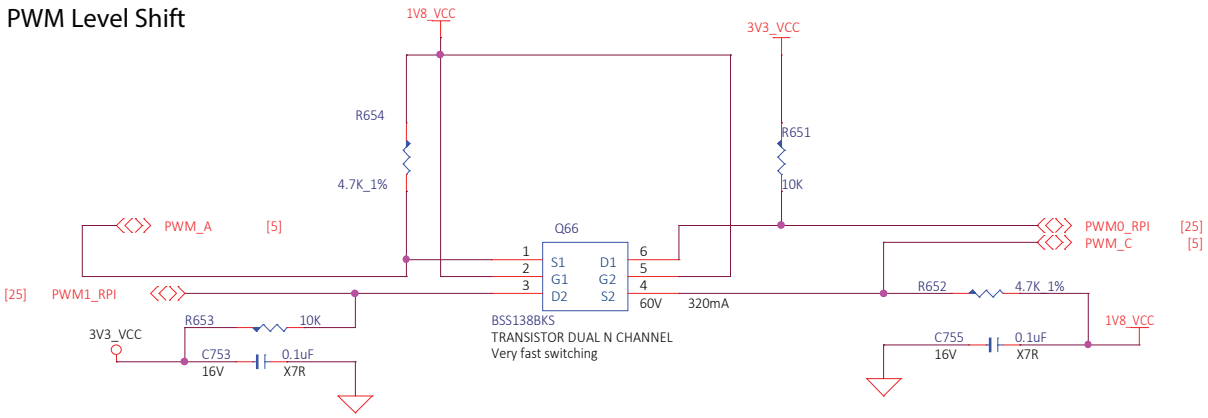


Figure 76: SOM-3000 PWM level shift reference circuitry

4.12 I2C Interface

The SOM-3000 module features three I2C interfaces.

4.12.1 I2C Signal Definition

The following table provides the definition of the I2C signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
SDA2	J1.7	GPIO61	1.8V	I, PU	I2C2 SDA, default connect to front Camera and MCU/IO extender
SCL2	J1.9	GPIO62	1.8V	I, PU	I2C2 SCL, default connect to front Camera and MCU/IO extender
SCL1	J1.24	GPIO60	1.8V	I, PU	I2C1 SCL, default connect to Capacitive Touch Panel and Rear camera
SDA1	J1.26	GPIO59	1.8V	I, PU	I2C1 SDA, default connect to Capacitive Touch Panel and Rear camera
SDA0	J2.27	GPIO57	1.8V	I, PU	I2C0 SDA, default connect to G-sensor and DC/DC
SCL0	J2.29	GPIO58	1.8V	I, PU	I2C0 SCL, default connect to G-sensor and DC/DC

Table 37: SOM-3000 I2C signal definition

4.12.2 I2C Design Notes

- The devices with the same slave address cannot use the same Bus.
- All MT8365 I2C are 1.8V domain only, all the device I2C ports should be the same.
  - Do not pull High the I2C Bus on the carrier board as it is already pulled High to 1.8V on SOM-3000 module.
  - The I2C SDA/SCL Bus is pulled High while the system is suspended, it is pulled Low when the system is powered off.

- The front and rear cameras must use different I2C whether the AF driver/sensor and driver/EEPROM's I2C slave addresses are the same or not.
- Route each I2C SDA/SCL Bus together and do not trace with other critical signals (MIPI or RF trace).
- If the I2C device power domain is 2.5V or 3.3V, a level shift is required. (ex. G-sensor/Touch panel)
- To avoid power leakage on the I2C Bus from the SOM-3000 module to the carrier board, a diode is required for the VDD on the level shift IC (CPU side).

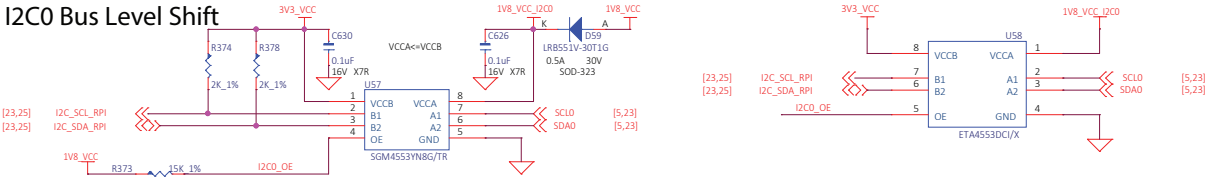


Figure 77: SOM-3000 I2C level shift IC reference circuitry

If an I2C Device & Host power is not present simultaneously when the system is suspended or powered off, a level shift is required.

Note:
The N Channel MOS FET should be a fast switching type, the Vgs(th) gate-source threshold voltage should be less than 1.65V.

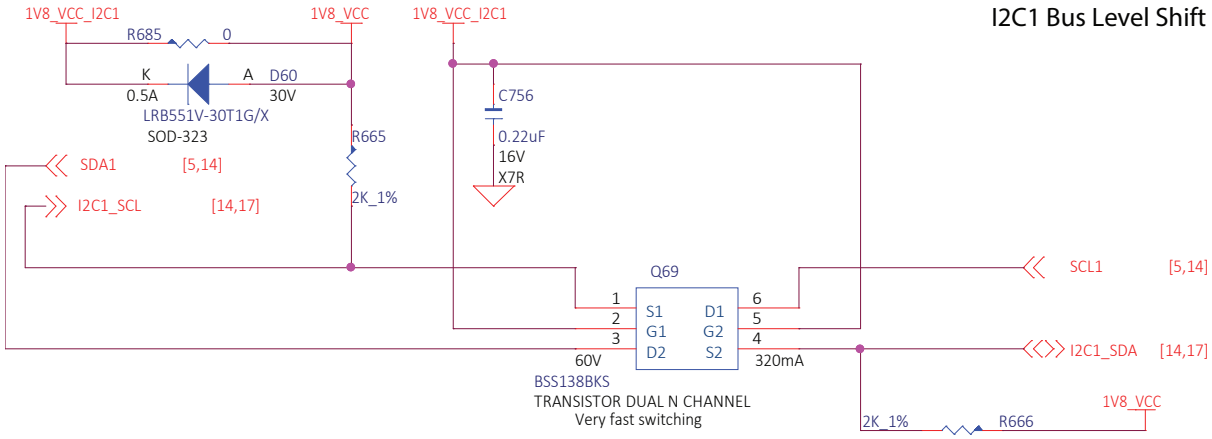


Figure 78: SOM-3000 I2C level shift reference circuitry

4.13 UART & SPI Interface

The SOM-3000 module features a SPI & two UART interfaces.

4.13.1 UART & SPI Signal Definition

The following table provides the definition of the UART & SPI signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
URXD2	J2.36	GPIO39	1.8V	I, PD	UART2 RXD, default for NFC
UTXD2	J2.38	GPIO40	1.8V	I, PD	UART2 TXD, default for NFC
UTXD1	J2.40	GPIO38	1.8V	I, PD	UART1 TXD output, default connect to RS232 transceiver
URXD1	J2.42	GPIO37	1.8V	I, PD	UART1 RXD input, default connect to RS232 transceiver

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
SPI_CS	J2.26	GPIO26	1.8V	I, PD	SPI_CS,SPI Bus chip select output, default for motor driver
SPI_MO	J2.28	GPIO29	1.8V	I, PU	SPI_MO,SPI Bus master data output, default for motor driver
SPI_MI	J2.30	GPIO28	1.8V	I, PD	SPI_MI,SPI Bus master data input, default for motor driver
SPI_CK	J2.32	GPIO27	1.8V	I, PD	SPI_CK,SPI Bus Clock output, default for motor driver

Table 38: SOM-3000 UART & SPI signal definition

4.13.2 UART & SPI Design Notes

- All MT8365 UART & SPI Buses are 1.8V domain only, all the device ports should be the same. Do not pull the UART & SPI Buses High on the carrier board as it is already pulled High to 1.8V on SOM-3000 module.
- The UART bus & SPI Bus is pulled High while the system is suspended and pulled Low when the system is powered off.
- Connect an IR receiver to the MCU GPIO when using the MCU as an IR decoder.
- Route each UART or SPI Bus together and do not trace with other critical signals (MIPI or RF trace).
- If the UART or SPI Buses device power domain is 2.5V or 3.3V, a level shift is required. (ex. motor driver)
- To avoid power leakage from the UART or SPI Buses from the SOM-3000 module to the carrier board, a diode is required for the VDD of the level shift IC (CPU side).

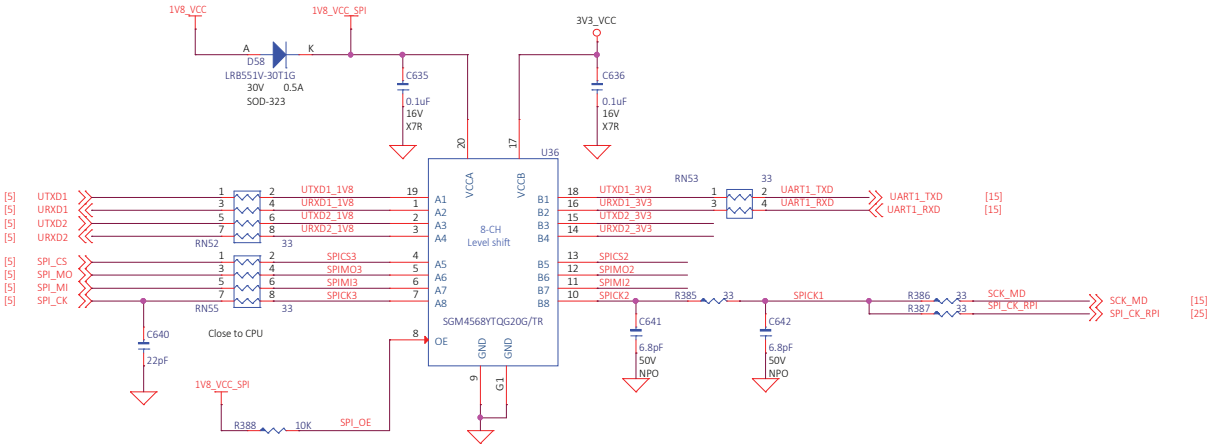


Figure 79: SOM-3000 I2C level shift IC reference circuitry

4.14 MCU Interface

The SOM-3000 module features an MCU interface.

4.14.1 MCU Signal Definition

The following table provides the definition of the MCU signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
MCU_INT	J2.44	GPIO132	1.8V	I, PD	Interrupt input, High active, connect to MCU
MCU_WDI	J2.46	GPIO133	1.8V	I, PD	Watchdog feed output, High active, connect to MCU
MCU_STATUS	J2.50	GPPIO64	1.8V	I, PU	MCU status, Low: MCU upgrading; High: MCU work
SDA2	J1.7	GPIO61	1.8V	I, PU	I2C2 SDA, default connect to front camera and MCU/I/O extender
SCL2	J1.9	GPIO62	1.8V	I, PU	I2C2 SCL, default connect to front camera and MCU/I/O extender

Table 39: SOM-3000 MCU signal definition

4.14.2 MCU Design Notes

It is highly recommended using the MCU to achieve the following functions:

- System power management, watchdog timer, IR decoder, system suspend/wakeup, RTC timer, battery charge status judgement, battery voltage ADC.

4.14.3 MCU Reference Schematics

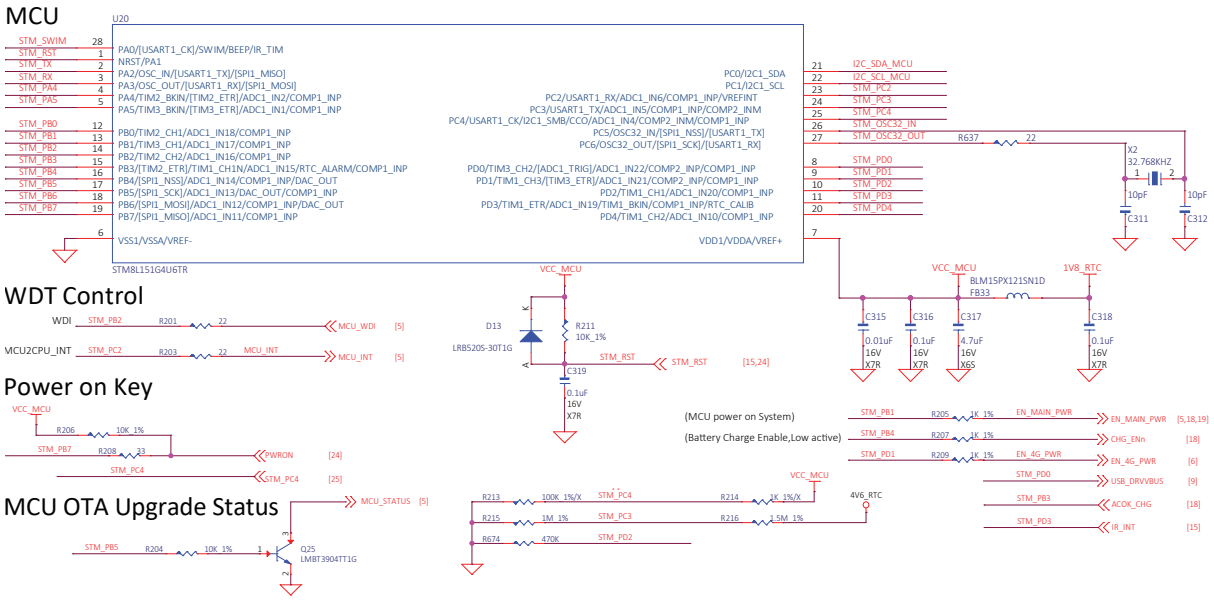


Figure 80: SOM-3000 MCU IC reference circuitry

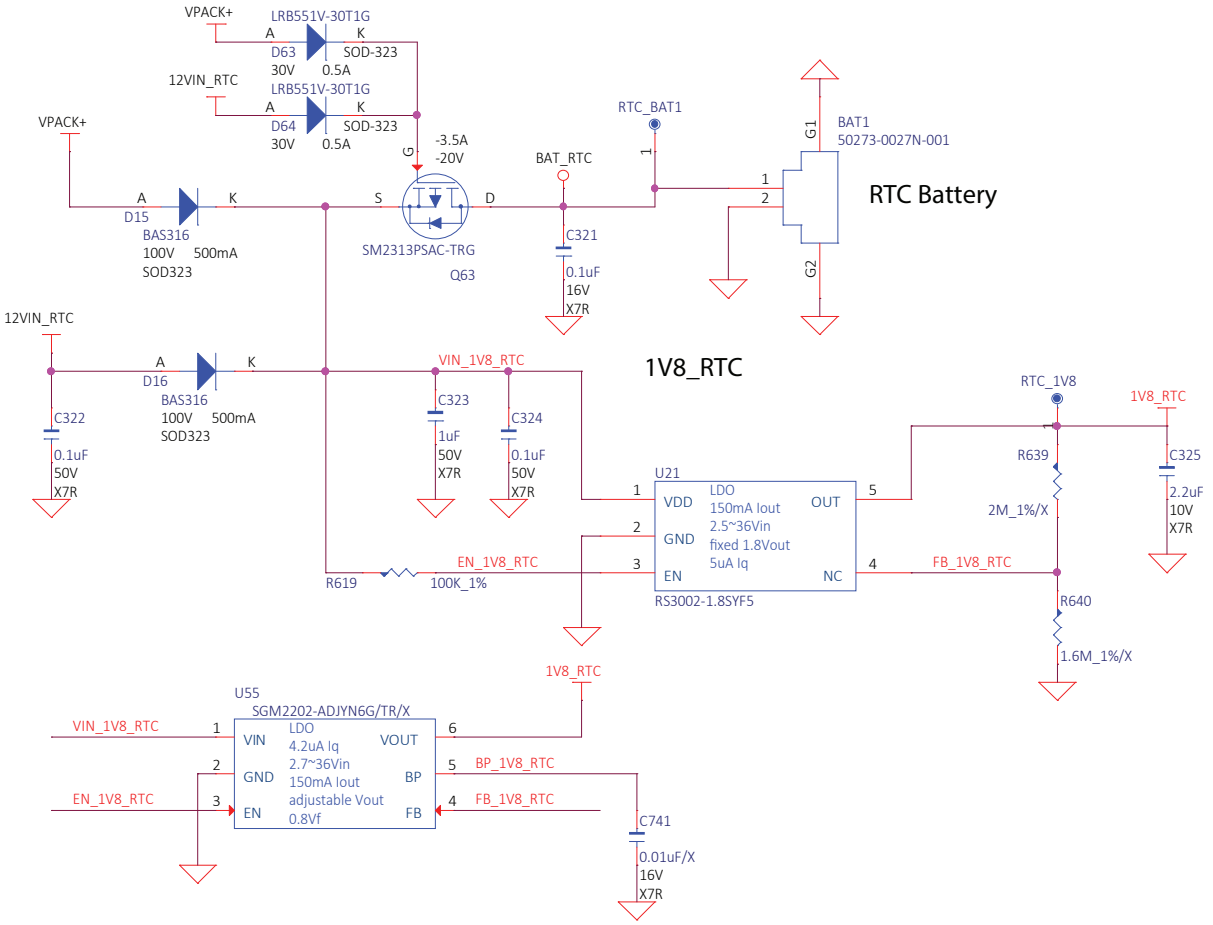


Figure 81: SOM-3000 MCU power supply reference circuitry

MCU Burning

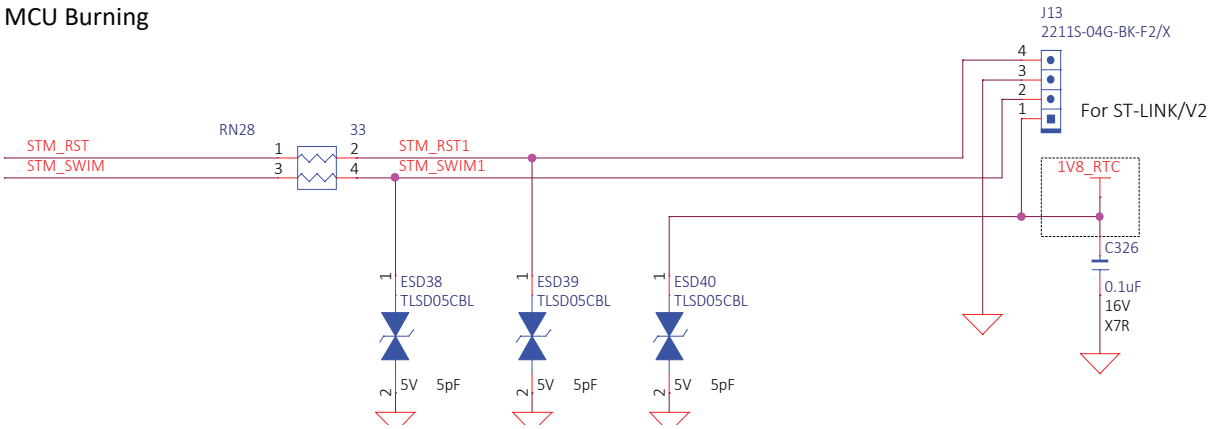


Figure 82: SOM-3000 MCU flash connector reference circuitry

4.14.4 MCU GPIO List

PIN#	GPIO#	I/O	Assignment	Function
28	PA0	I	SWIM	MCU Burning
1	PA1	I	RST	MCU reset, Low active
2	PA2	O	UART_TX	UART TX to 4G, reserved
3	PA3	I	UART_RX	UART RX to 4G, reserved
4	PA4	I	LAN_WAKEUP_SYSTEM	ETHERNET WAKEUP SYSTEM, High pulse active, reserved

PIN#	GPIO#	I/O	Assignment	Function
5	PA5	I	BATGD_CHG	Battery status, Low: Low voltage<6V, High: normal, reserved
12	PB0	I	STATUS_CHG	Battery charge status, Low: Charging; High: Charge OK
13	PB1	O	EN_Main_PWR	System main power enable output, High active
14	PB2	I	MCU2CPU_INT1	WDI, CPU watch dog feed, High pulse active
15	PB3	I	ACOK_CHG	DC Input detect, High active
16	PB4	O	CHG_ENn	Battery charge enable, Low active (Reset Pull up), reserved
17	PB5	O	MCU_STATUS	MCU OTA upgrade STATUS output High: MCU upgrading; Low: MCU normal work
18	PB6	I	4G_WAKE2MCU	4G module sleep instructions; 4G wake up host: reserved
19	PB7	I	PWRON	Power on key, Low pulse active
21	PC0	IO	I2C_SDA	I2C_SDA, connect to CPU
22	PC1	I	I2C_SCL	I2C_SCL, connect to CPU
23	PC2	O	MCU2CPU_INT2	MCU to CPU Interrupt: High active
24	PC3	I	POWER DETECT	Power supply detect: MCU enter low power mode when detect Low. High: power supply Low: Power remove
25	PC4	I	ADC	BATTERY VOLTAGE ADC INPUT
26	PC5	I	OSC32_IN	OSC32_IN
27	PC6	O	OSC32_OUT	OSC32_OUT
8	PD0	O	USB_DRVVBUS	USB Host 5V output enable: High active
9	PD1	O	EN_4G_PWR	4G module power enable output: High active
10	PD2	O	MCU suspend status	MCU work: High MCU suspend: Low
11	PD3	I	IR_INT	IR input, connect to IR receiver
12	PD4	I	4G_RI2MCU	4G output signal to wake up the host, reserved

Table 40: SOM-3000 MCU GPIO list

4.15 Button Interface

The SOM-3000 module features three buttons interface.

4.15.1 Button Signal Definition

The following table provides the definition of the Button signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
System Reset	J2.48	SYSRSTB	1.8V	I, PU	System Reset input, Low active
KPCOL0	J2.52	GPIO24	1.8V	I, PU	Connect to firmware download key, input, Low active
PWRON	MCU pin 19	PB7	1.8V	I, PU	Power on key, Low pulse active

Table 41: SOM-3000 button signal definition

4.15.2 Button Design Notes

- Do not pull the SYSRSTB J2.48 pin High on the carrier board as it is already pulled High to 1.8V on SOM-3000 module.

Reset Key

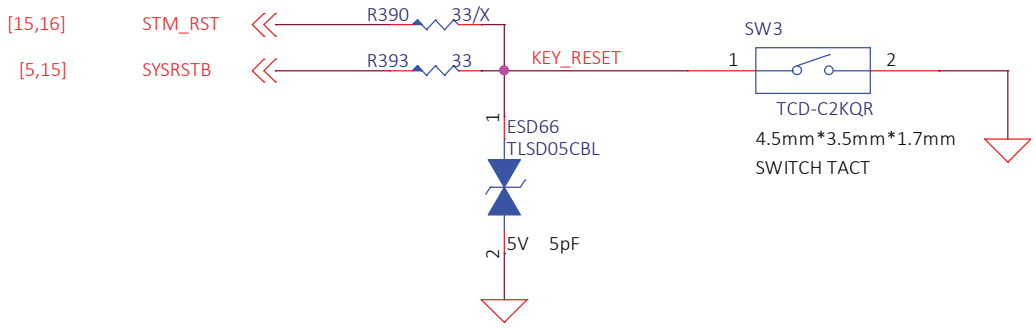


Figure 83: SOM-3000 reset button reference circuitry

- Do not pull the KPCOL0 J2.52 pin High on the carrier board as it is already pulled High to 1.8V on SOM-3000 module.

Download Button

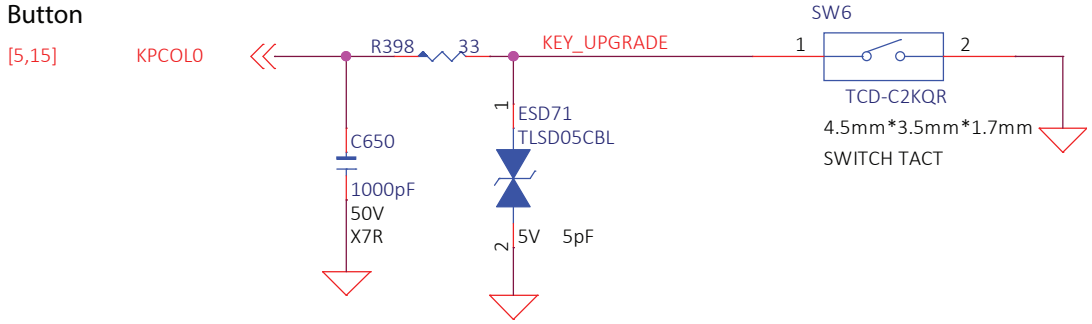


Figure 84: SOM-3000 download button reference circuitry

Power Key

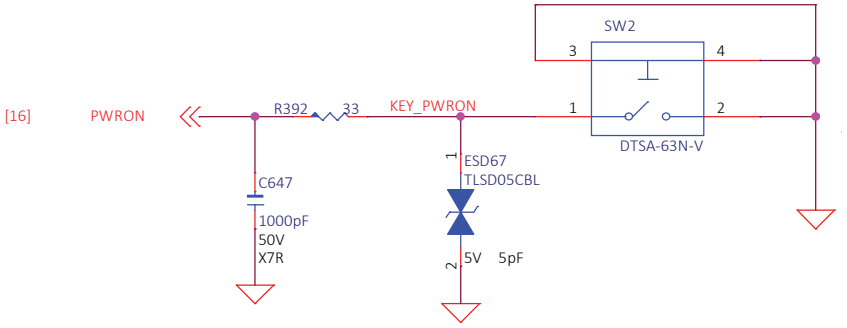


Figure 85: SOM-3000 power button reference circuitry

4.16 Power Manage Interface

The SOM-3000 module features two power management interfaces to control the carrier board power.

4.16.1 Power Manage Signal Definition

The following table provides the definition of the power management signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
EXT_3V3_ENABLE	J2.54	GPIO70	1.8V	I, PD	Carrier board power enable, output, High active, suspend off,
EXT_PMIC_EN1	J2.56	EXT_ PMIC_EN1	1.8V	O, PD	Carrier board power enable, output, High active, suspend on

Table 42: SOM-3000 power management signal definition

4.16.2 Power Manage Design Notes

The following table describes the carrier board power control pin status.

Pin#	Name	Power off	System Work	System Suspend
J2.54	EXT_3V3_ENABLE	Low	High	Low
J2.56	EXT_PMIC_EN1	Low	High	High

Table 43: SOM-3000 power management status

- The EXT_PMIC_EN1 J2.56 pin is used to keep power to devices while the SOM-3000 module is suspended, such as USB Hub, USB to Ethernet Bridge.
- The EXT_3V3_ENABLE J2.54 pin is used to turn off power to devices when the SOM-3000 module is suspended, such as LCD, speakers, etc.

4.17 Gas Gauge Interface

The SOM-3000 module features a Gas Gauge interface to monitor the lithium polymer battery capacity.

4.17.1 Gas Gauge Signal Definition

The following table provides the definition of the gas gauge signals that are implemented in the M.2 slot.

Signal Name	Pin #	I/O	Pad Characteristics		Description
			Voltage	Type	
BATSNS	J2.25		4.2V	AI	1-cell Battery voltage input
CS_P	J2.23		4.2V	AI	Battery Gas Gauge CS_P
CS_N	J2.21		4.2V	AI	Battery Gas Gauge CS_N

Table 44: SOM-3000 gas gauge signal definition

4.17.2 Gas Gauge Design Notes

- The Gas gauge sensor and calculation circuit is already included by the PMU on the SOM-3000 module. If using a lithium-ion battery, an external circuit must be reserved for the battery current sensor and single battery voltage circuit. The battery voltage must be isolated by the P Channel MOS FET to prevent power leakage.

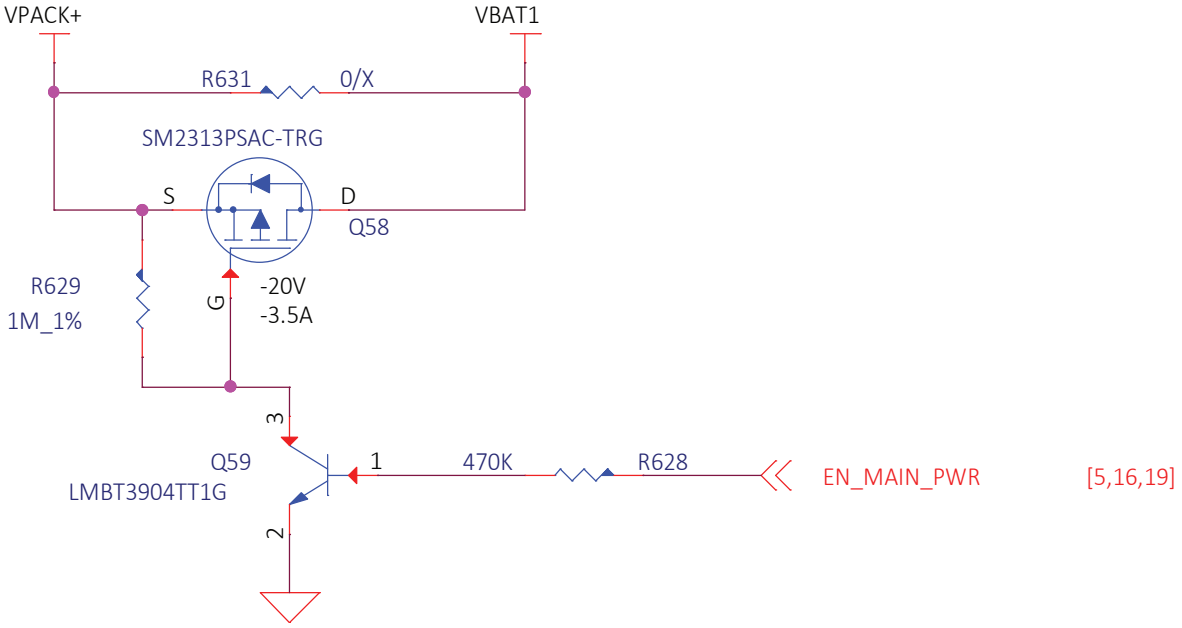


Figure 86: SOM-3000 battery leakage protect reference circuitry

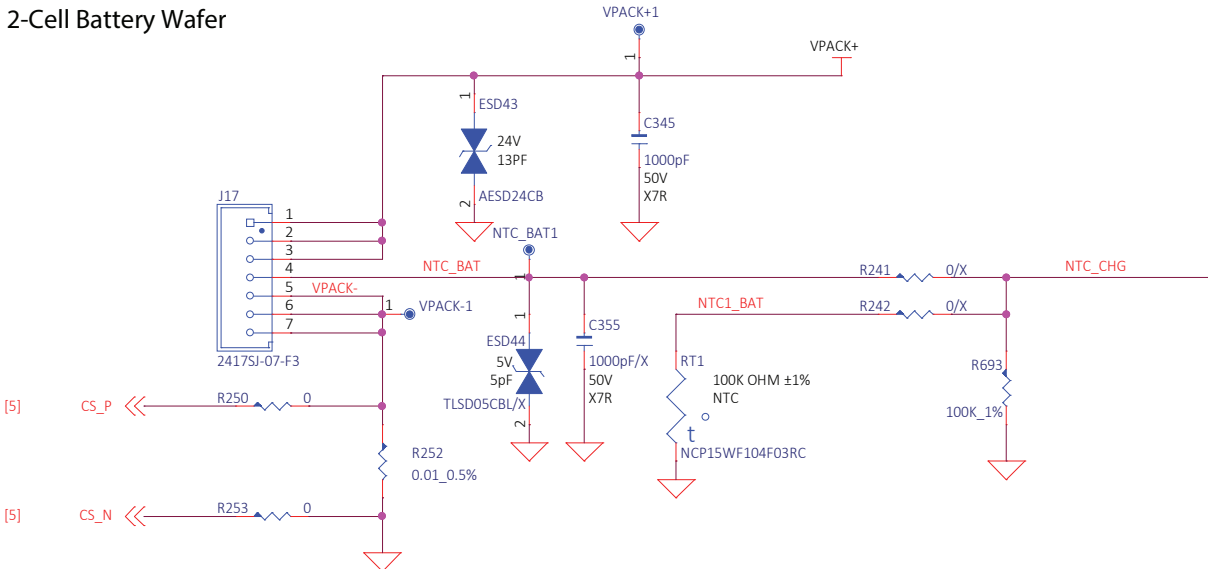


Figure 87: SOM-3000 gas gauge current sense reference circuitry

- When a dual-cell battery is used to supply power to the carrier board, a 2:1 voltage divided circuit & voltage following circuit is required.

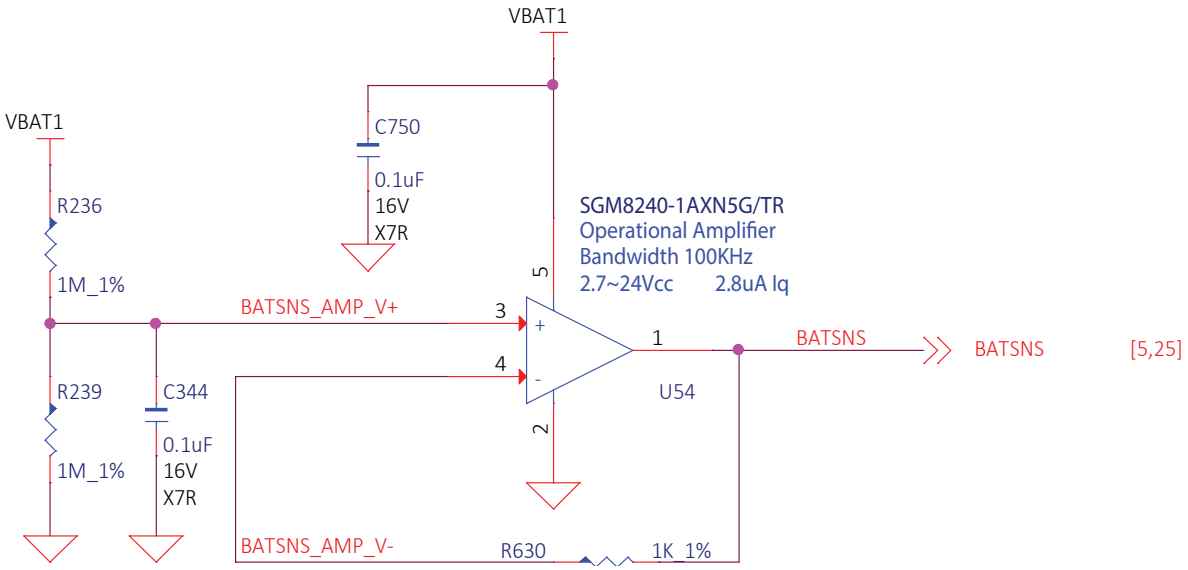


Figure 88: 2:1 voltage divided voltage following reference circuitry

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